MAX 3543 Layout Guide

This application note shows the critical design/layout features of MAX3543 on 234RD1 Hybrid TV (DTV + ATV) reference design. Specific discussion topics include MAX3543's schematic review, critical design features, critical layout features and general considerations on components placement.

Introduction

The MAX3543 hybrid broadband single-conversion television tuner is designed for use in analog (PAL, SECAM) + digital (DVB-T, GB20600) television sets and terrestrial receivers. It receives all television bands from 47MHz to 862MHz and converts the selected channel to an industry-standard 36MHz IF.

The MAX3543 is available in a small, 6mm x 6mm, thin QFN package, and the application circuit fits in 20mm x 25mm on a two-layer board with single-sided component mounting.

Some designs have proven it can be used in TV, STB, and USB device. In order to design MAX3543 easily in customers' devices, this application note introduces the critical design and layout features of MAX3543. An example used in this note is 234RD1 DVB-T/PAL reference design.

Layer Stack:

Figure 1 shows the layer stack-up used on 234RD1 reference design boards. Layers definitions are shown as following:

Layer count: 2
Top layer ---- Components side and critical signal layer
Bottom layer ---- Ground and other signals

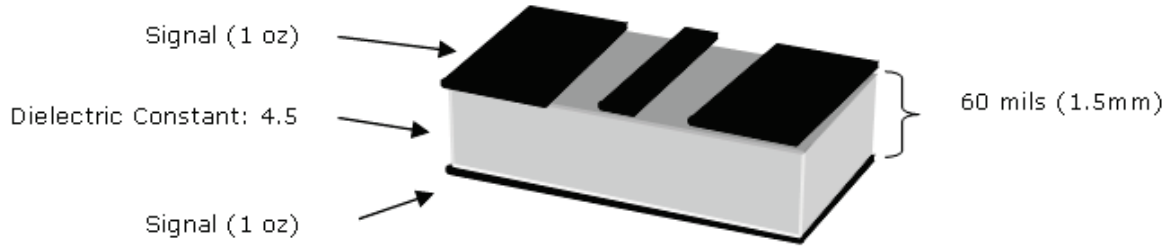

Figure 1 Layers Stack-up in 234RD1

Layout, Schematic Overview:

The overview of MAX3543's schematic and layout is shows as Figure 2, 3 and 4. Please see Figure 2 for locations guide refers to.

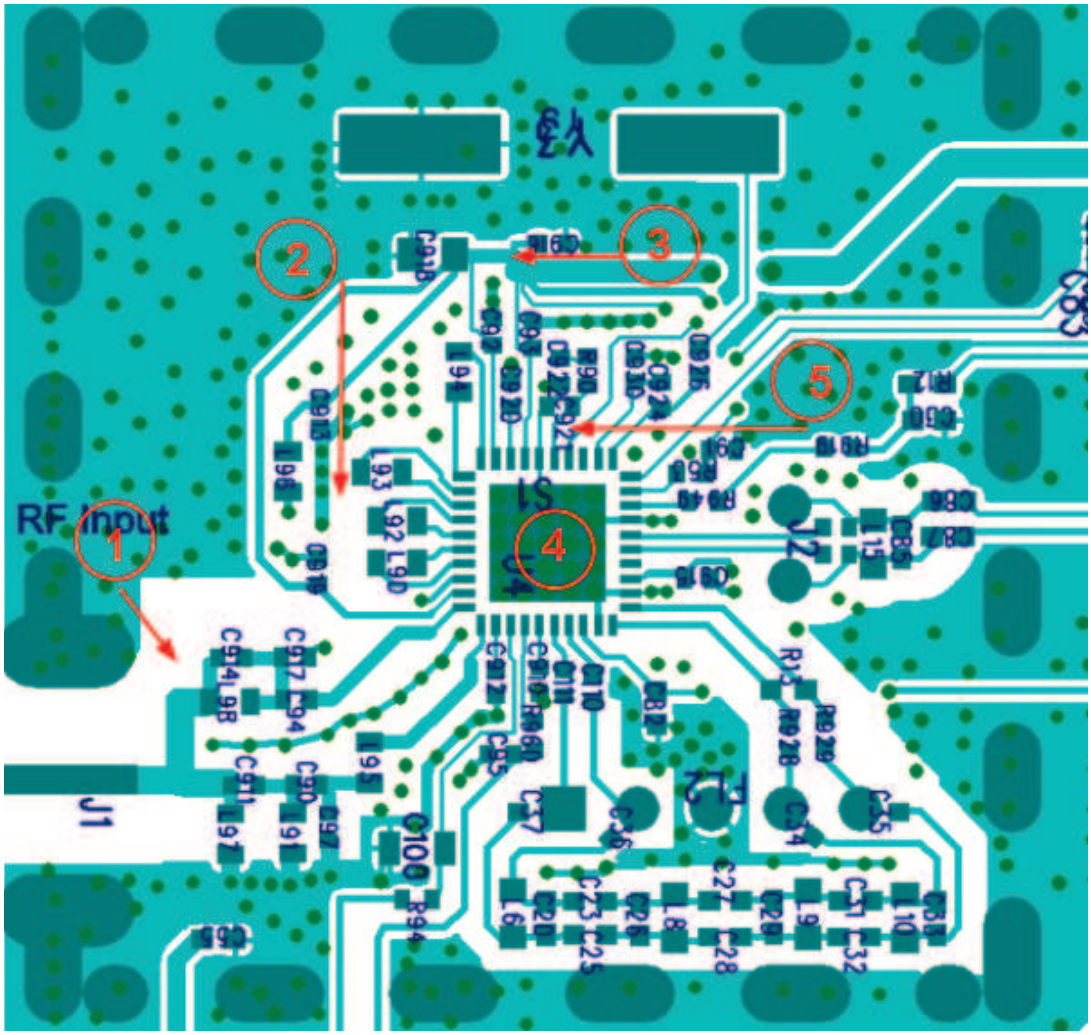

Figure 2 Top layer Layout of 234RD1

All components and most traces are in top layer

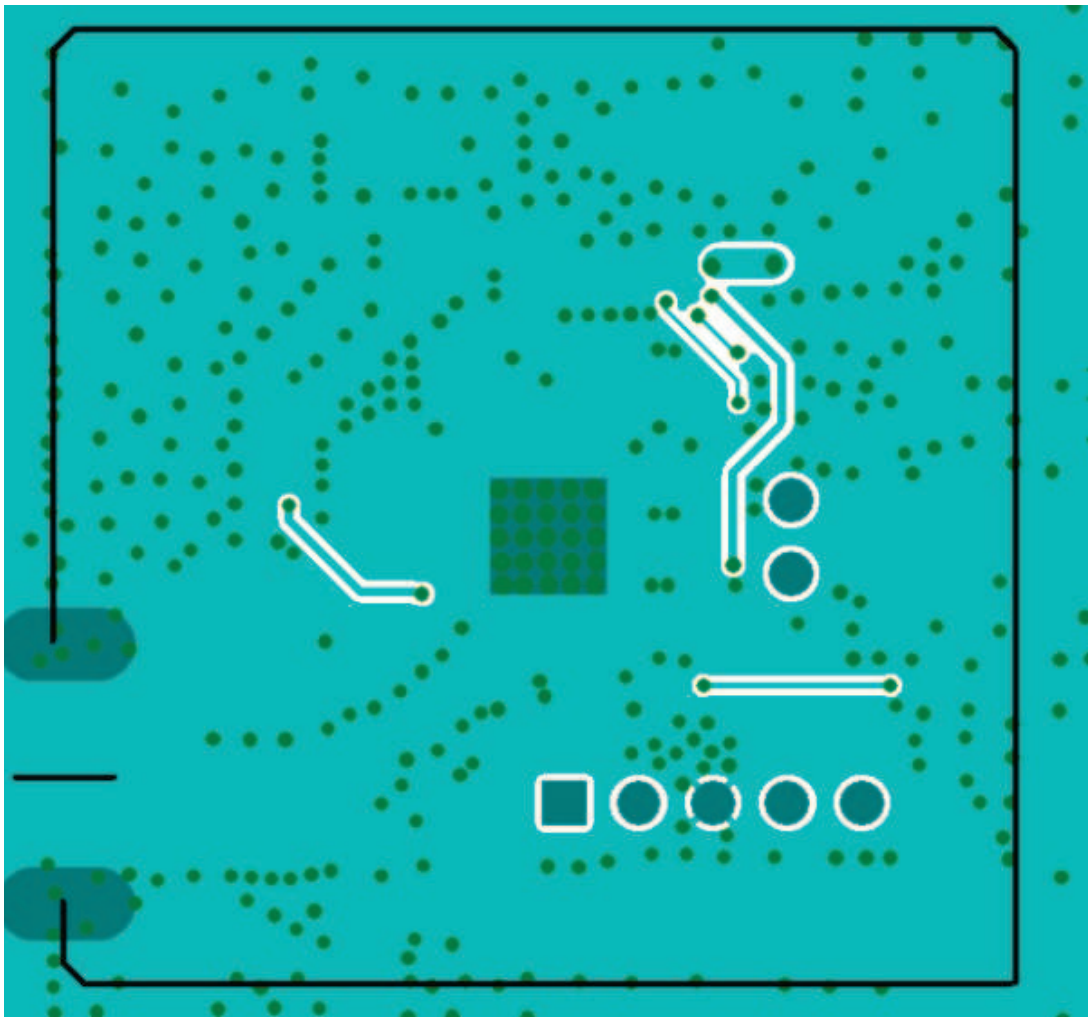

Figure 3 Bottom layer Layout of 234RD1

For optimized RF/ thermal performance, minimize the trace at bottom as much as possible to make bottom layer as a whole piece of copper.

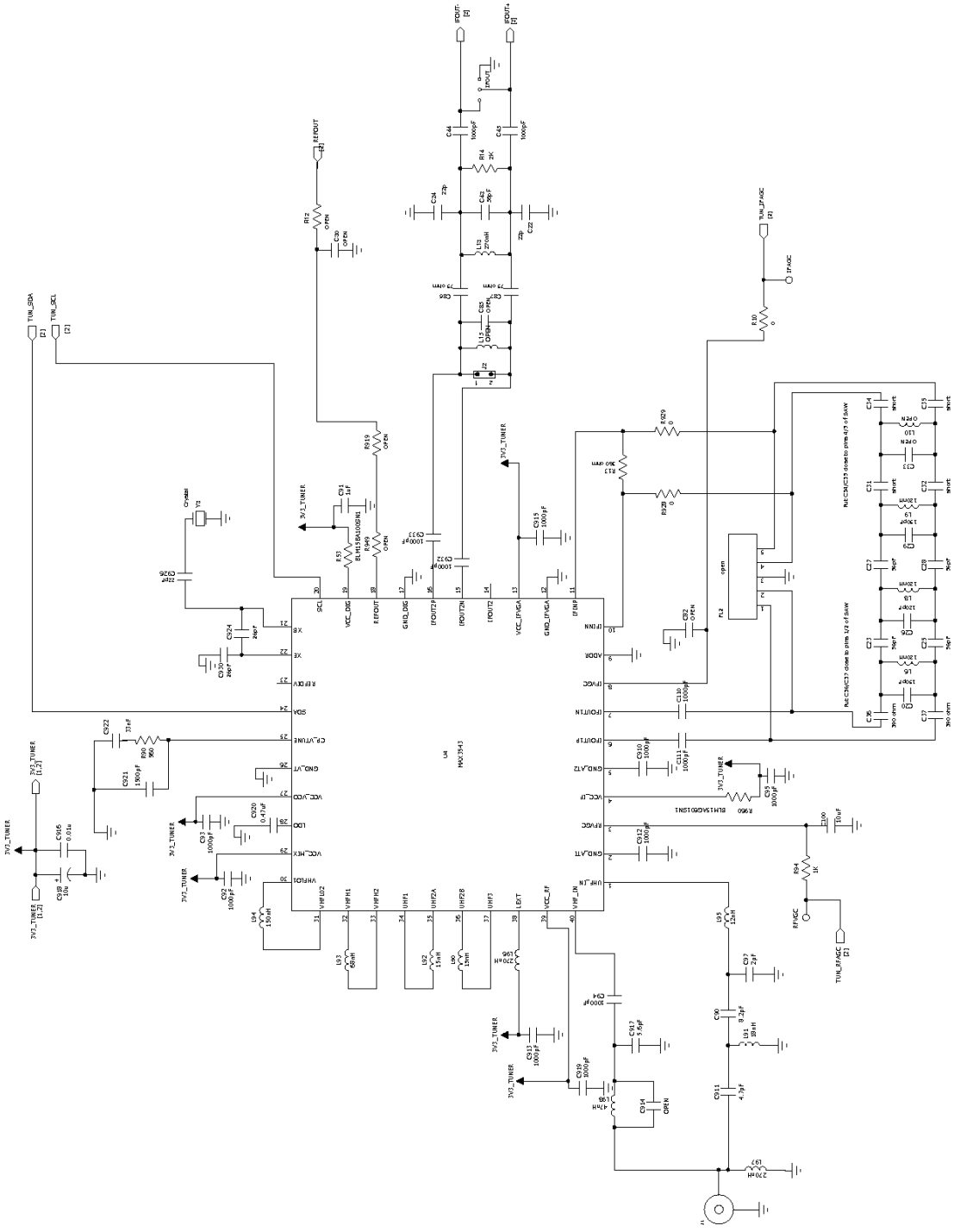

Figure 4 Schematic of 234RD1

Guide:

1. RF input and Diplex filter

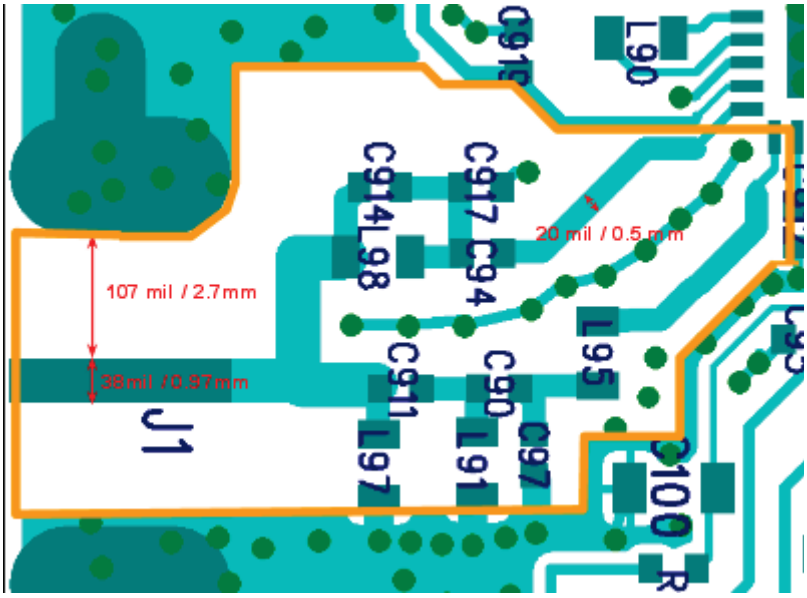

Figure 5 RF input and Diplex filter

For DVB-T receiver, 75Ω characteristic impedance and F-type, female, 75Ω connector are suggested by Nordig.

- RF traces should be as short as possible to minimize the losses and radiations
- It is important for the layout with 75Ω controlled impedance lines and solid ground plane under RF traces. On the example layout as Figure 5 shown, RF input pad width=38mil (0.97mm) and trace to ground gap=107mil (2.7mm) are used. The RF input width is choose to have similar size of RF connector.
- For better VHF/UHF isolation, a diplex filter (L98/C94/C917, L97/C911/L91/C90/ L95) is used at RF input. Please use the exactly same placement as above figure shown for optimized performance
- the RF trace width used after deplex filter is 20mil (0.5mm), this size to choose to have similar size of 0402 component pad to minimize the discontinuity of the RF trace.
- To avoid unwanted parasitic and coupling, a top layer ground keep out should be placed, as orange outline shown at Figure
- Abundant vias should be placed along the RF traces on the edges of ground to improve the performance of RF traces and keep from undesired coupling

2. Tracking filter

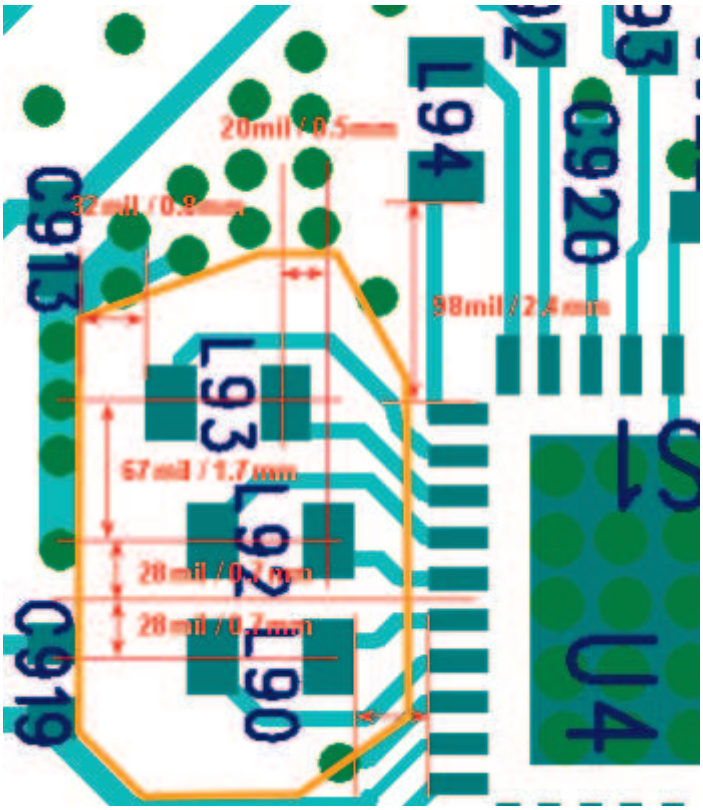

Figure 6 Tracking filter

Tracking filter is very important for Gain/Noise/Image Rejection. For optimazied performance please use EXACTLY same layout as Figure shown:

- Place L92 and L90 symmery to center of pin 35 and 36
- Center of Pin 35/36 to center of L92 = 28 mil / 0.7mm
- Center of Pin 35/36 to center of L90 = 28 mil / 0.7mm
- L93 and L92 offset at X direction = 20 mil / 0.5mm
- L93 and L92 offset at Y direction = 67 mil / 1.7mm
- L93 right pad edge to ground edge = 32 mil / 0.8mm
- L94 bottom edge to pin =98mil /2.4mm
- To avoid unwanted parasitic and coupling, a top layer ground keep out should be placed, as orange outline shown at above figure

3. Power Lines

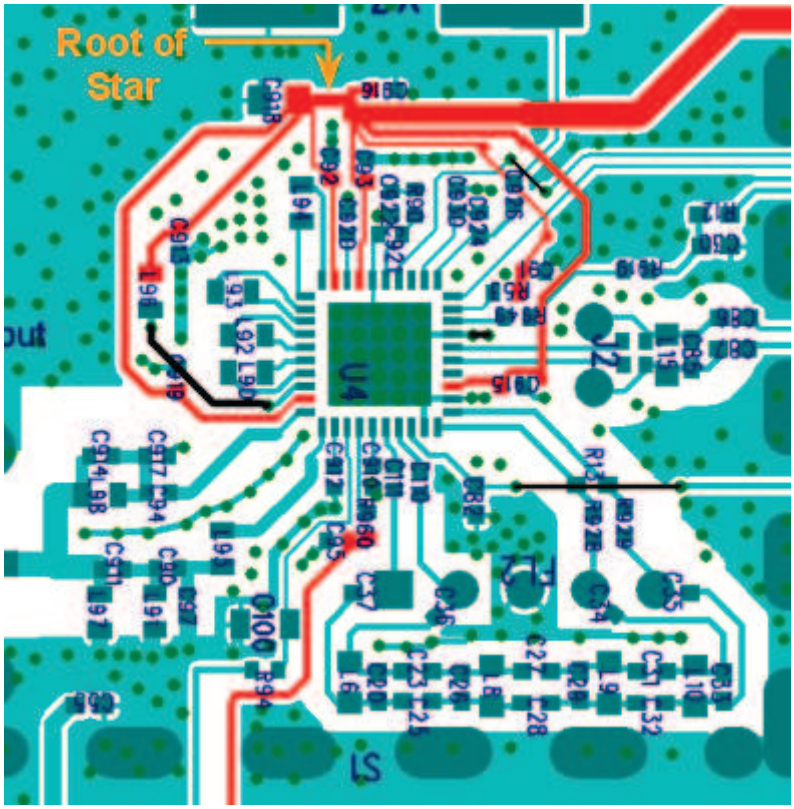

Figure 7 Power Line

- As above figure shown, the layout uses a star configuration on (mostly on top layer) whenever possible for DC voltage distribution from a common point near LDO. Several different lines fan out from this point,which was done for isolation and is highly recommended
- Place 2 capacitor (C918 & C916, 10u & 0.01uF) at the root of the star
- Bypass capacitors are located as close as possible to each voltage connection point. Use at least one via per bypass capacitor for a low-impedance ground connection.
- When connecting bypass capacitor to ground, avoid to share same vias/small piece of ground copper at top layer, which could cause un-wanted coupling

4. Exposed Paddle of Ground

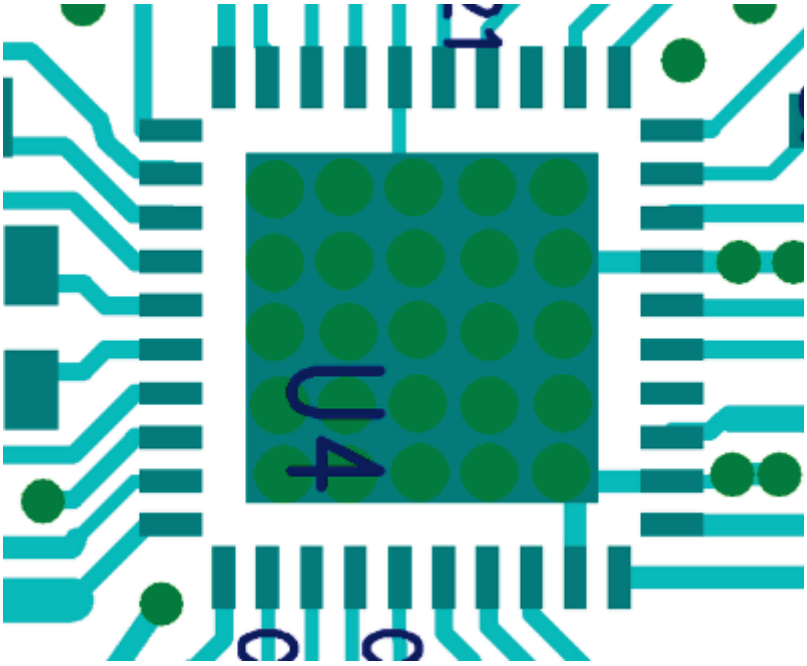

Figure 8 exposed paddle

- The exposed paddle of MAX3543 should be soldered to board evenly and use abundant vias beneath the exposed paddle for maximum heat dissipation. In this design 25 vias is used. Vias diameter =26 mil
- Solder masking oping for exposed paddle at both top and bottom layer, which allow the solder flow though thermal vias to improve thermal performance
- Connect ground pin (#12,#17 & #26) to the ground paddle

5. PLL

C921, C922 and R90 constitute the loop filter of PLL. For optimized PLL phase noise performance, please follow:

- The loop filter should be placed as close as possible to the MAX3543.
- Ground pads of two capacitors and Pin26 GND of MAX3543 should be tied together and then connected to ground plane through one separated via.
- Connect Pin26 GND to exposed paddle

Figure 9 PLL

6. Other Consideration Of the Layout

- To avoid unwanted parasitic and coupling, do NOT place ground copper too close to IF LC filter (L6, C20.... C29,L9). In this design, about 30 mil keep-out is used
- Make sure IFOUT+/- (pin # 15 & 16) differential lines close to each other, place top layer ground copper along those lines.
- Pay attention to I2C line, Xtal line. They carry high voltage digital signal, keep them away from sensitive analog trace.
- Make bottom layer ground a whole piece copper as much as possible.
- Use abundant vias on top layer ground plane, NO floating copper piece.
- Use shield for EMC protection