ECE 464

Project 3 - Combinational Circuit Study Report

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1.Introduction

Theory:

Combinational logic circuit combines logical functions, which are implementing Boolean functions, where output depends on current input values combination only.

Combinational Logic circuit consists of logic gates (**AND, NAND, OR, NOR, XOR, XNOR, NOT**), which have different different combinational logic, thus different output of each gate, which affects overall output. Each of the gate can be distinguished by different logic table. To obtain the output (result) we are using: truth table, Karnaugh Map and circuit diagram.

a) Goal of the investigation:

In this part of the project we are examining the fault coverage of pseudo random Test Vectors in combinational circuit. The goal of the experiment is to:

1. Generate Pseudo Random Test Vectors.
2. Implement Test Vectors into combinational circuit simulator
3. Detect if size of the circuit, and the way of the generation of the Test Vector have any influence on the fault coverage of the circuit, and how it changes at each size.

The experiment will challenge our main question - **How test vector coverage changes with the size of the circuit, and is it becoming more or less effective?**

2. Experiment Procedure

For this experiment you will need:

1. Small/Medium/Large .bench type files.

   Bench files/circuits used in this experiment - **c17,c432,c2670**
2. Full Fault list generator, which will generate .txt file of all possible faults in the circuit.
3. Test Vector Generator that will create 5 different Test Vectors (refer to Table 1)
4. Simulator, that will show fault coverage of each Test Vector.

a) Generating the full fault list:

At the beginning of the experiment we have to create full fault list of the given circuits. For circuits used in this experiment the amount of the faults detected for each circuit is:

1. **c17:** 46 faults
2. **c432:** 1064 faults
3. **c2670:** 7004 faults

b) Generation of the test vectors:

In part **b)** of the experiment we will create 5 different Test Vectors. To Generate them, we will use different techniques described in the Table 1.

Test Vector	Generator	Seeding mechanism
TV_A	Single N-bit counter	one seed (s0 by user)
TV_B	Multiple 8-bit counters	oneseed (s0 by user) for all
TV_C	Multiple 8-bit counters	different seeds (... s2, s1, s0) where s0 is set by user, and s[i+1] is the next vector in the sequence after s[i]
TV_D	Multiple 8-bit LFSRs (taps at 2, 3, 4)	one seed (s0 by user) for all
TV_E	Multiple 8-bit LFSRs (taps at 2, 3, 4)	different seeds (... s2, s1, s0) where s0 is set by user, and s[i+1] is the next vector in the sequence after s[i]

Table 1: Test Vectors

c) Implementing Test Vectors into the simulator:

In this part we are implementing our generated test vectors into the simulator. We are using simulator that checks how much TVs are covering after each batch. For this particular experiment we picked seed = 1 and batch size = 1 for all circuit sizes.

d) Results:

As the simulator ended testing all of the Test Vectors coverage for all 3 circuits we can begin to look at the outcome of the experiment:

1. **c17:**

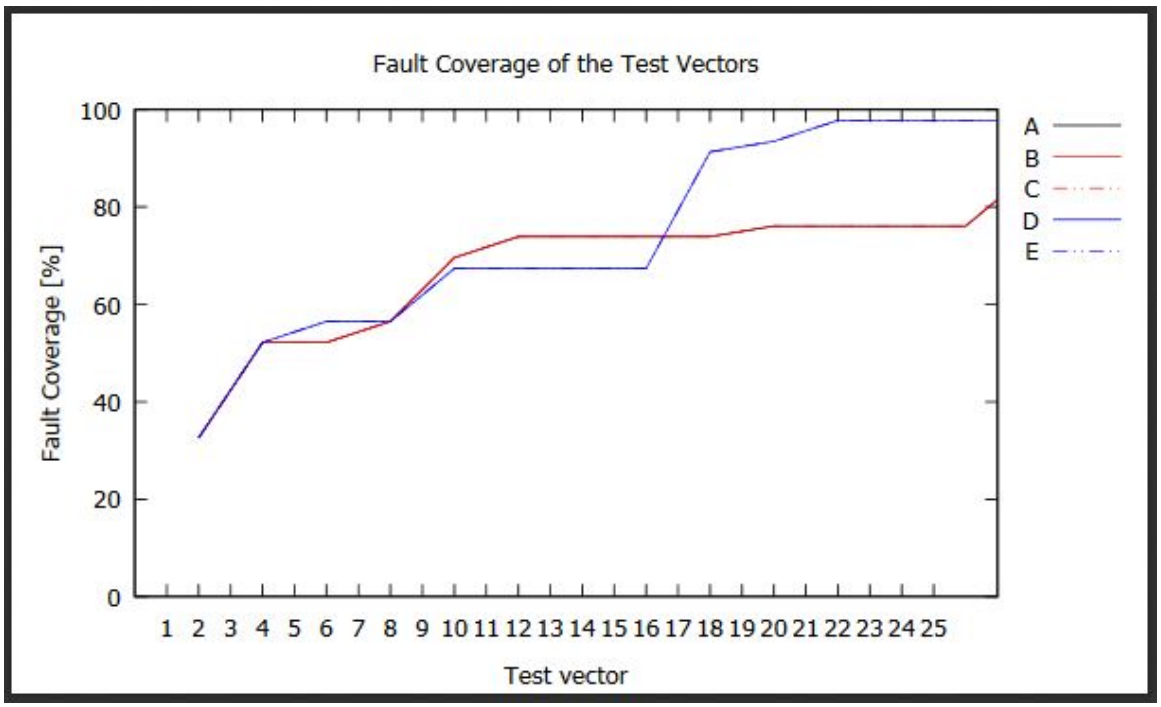

Figure 1: C17 fault coverage

2. **c432:**

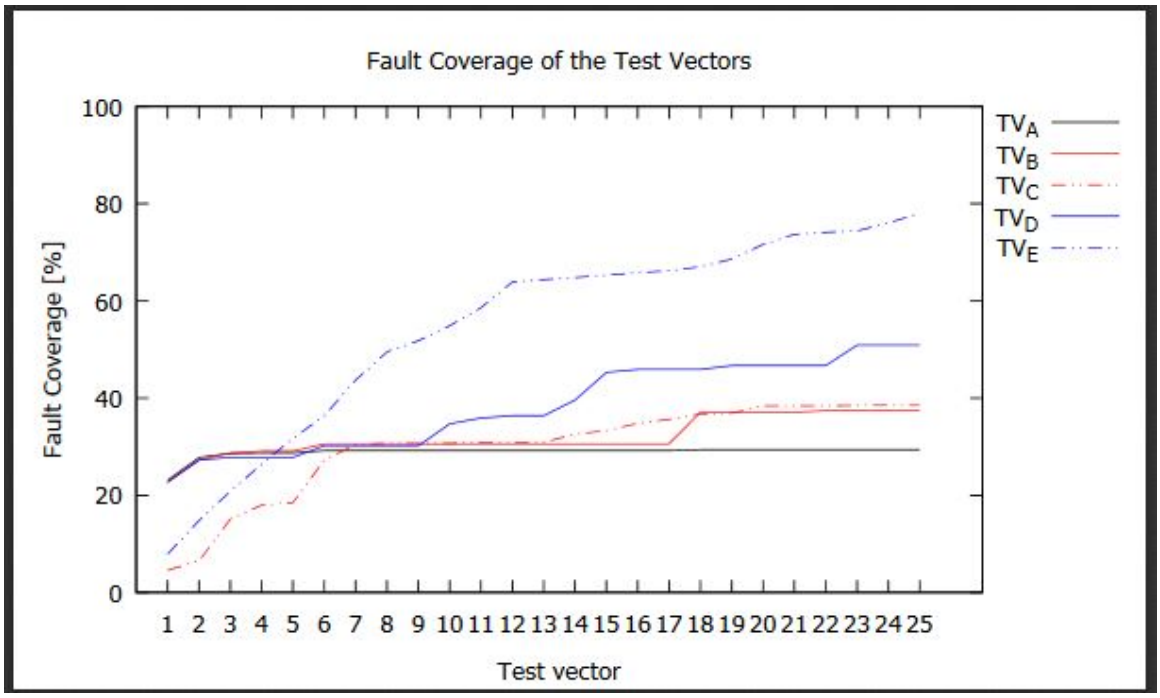

Figure 2: C432 fault coverage

3. **c2670:**

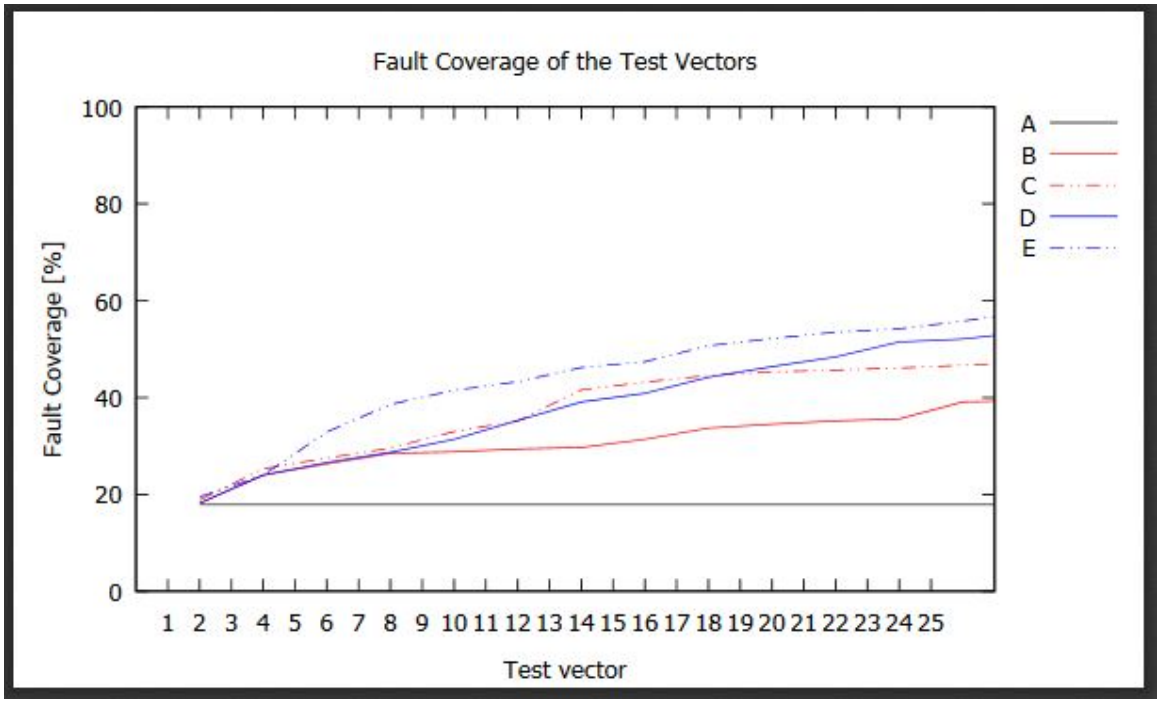

Figure 3: C2670 fault coverage

3. Experiment Results

In conclusion we can notice that the best method to cover all the faults is **TV E**, while the pseudo random generated test vectors covers the best at the **smallest size** of the circuit. The least effective method was **TV A**.

4. Explanation of the result

As we can notice the bigger the circuit becomes, the worse the fault coverage of the test vector becomes. The biggest change starts for the most effective TV - **TV E**, as we can see with the size of the circuit, the coverage drops down much faster than the other methods.

5. Was this expected to happen?

Well assuming the circuit size increases, the probability of finding particular fault using one of the methods in **Table 1** decreases. Experiment shown that for instance **TV C** and **TV D** had small incrementation of the coverage at the experiment, but if we generated much bigger circuits the decrementation of coverage would be even more noticable.

6. How it applies to 464 material?

During the last projects everything has been revolving around finding the best test vectors, applying them to the simulator and coming out with as efficient solution as possible. We came out with this simple experiment to wrap up 464 material and decide how size of the circuit and design of the test vector affects overall testability, and if it is easier to cover small, simple circuits, or is it easier to do so on large circuits - assuming of course we are not counting in factors such as run time. The answer was unclear for our group as we were usually working with medium and small circuits only.

7. references

Lala, P. K. (2009). An introduction to logic circuit testing. San Rafael, CA: Morgan and Claypool Publishers.