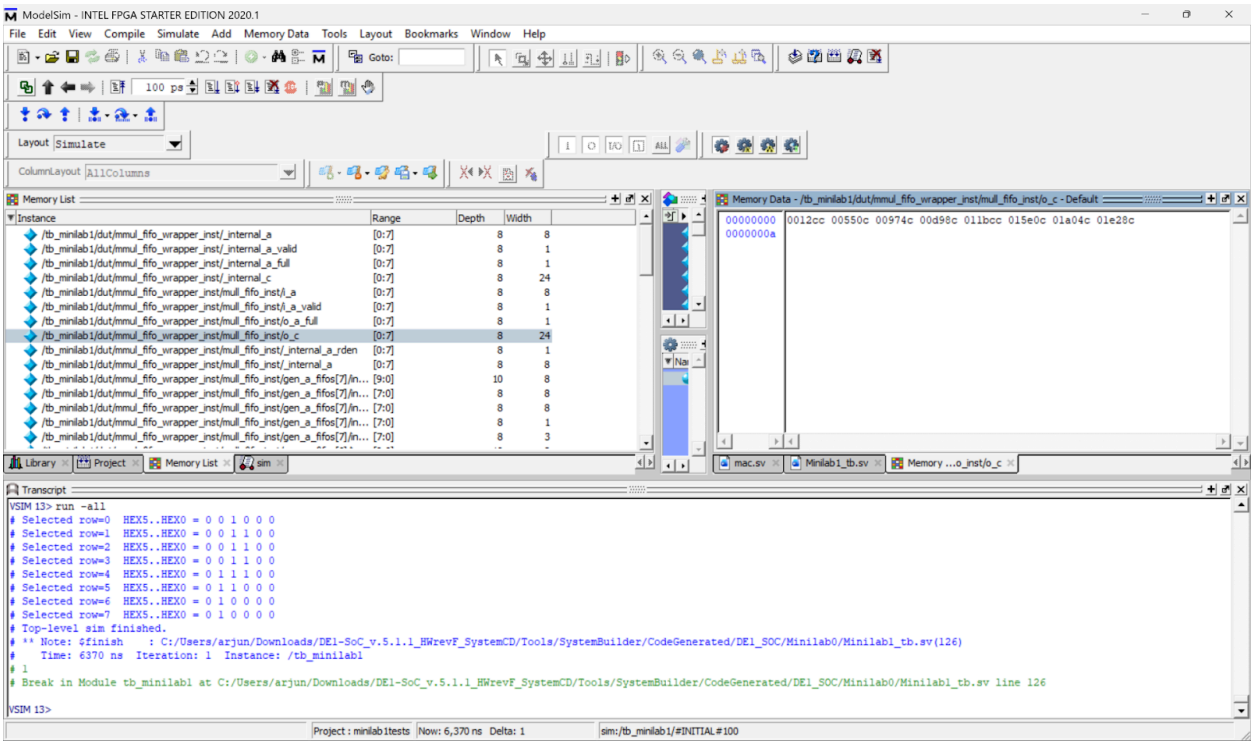
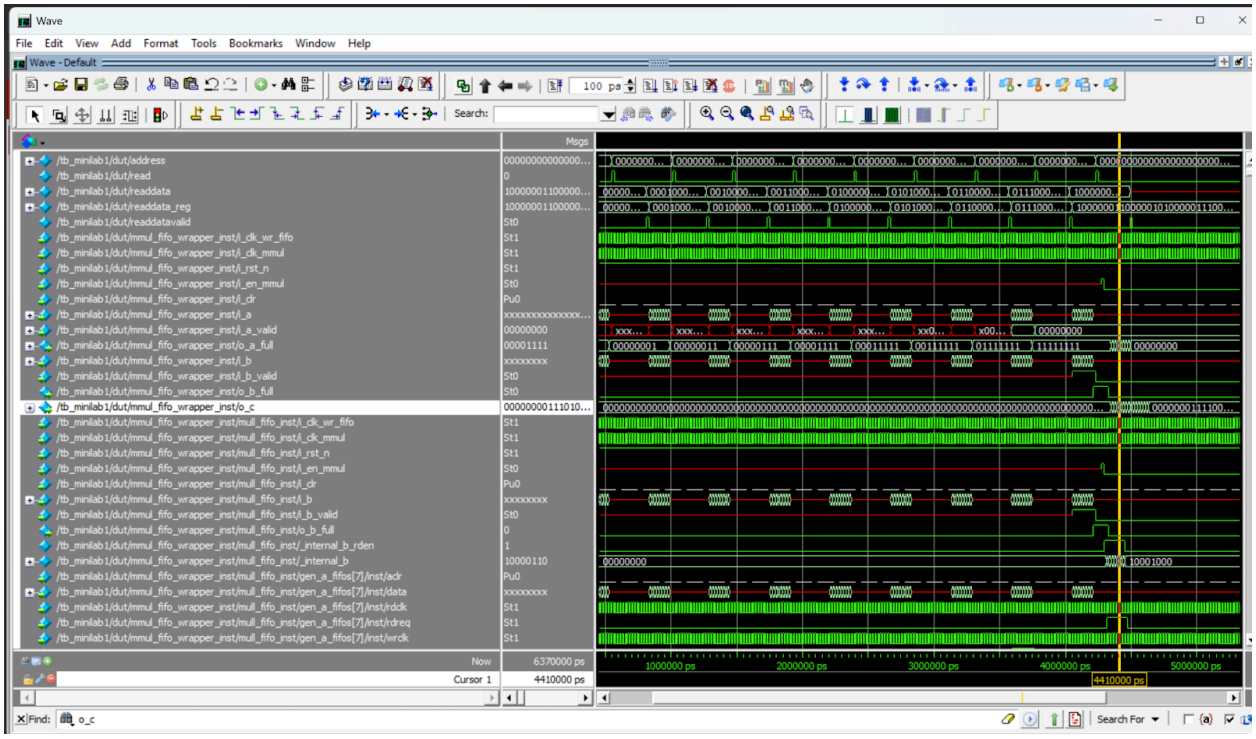
- How I created this repository

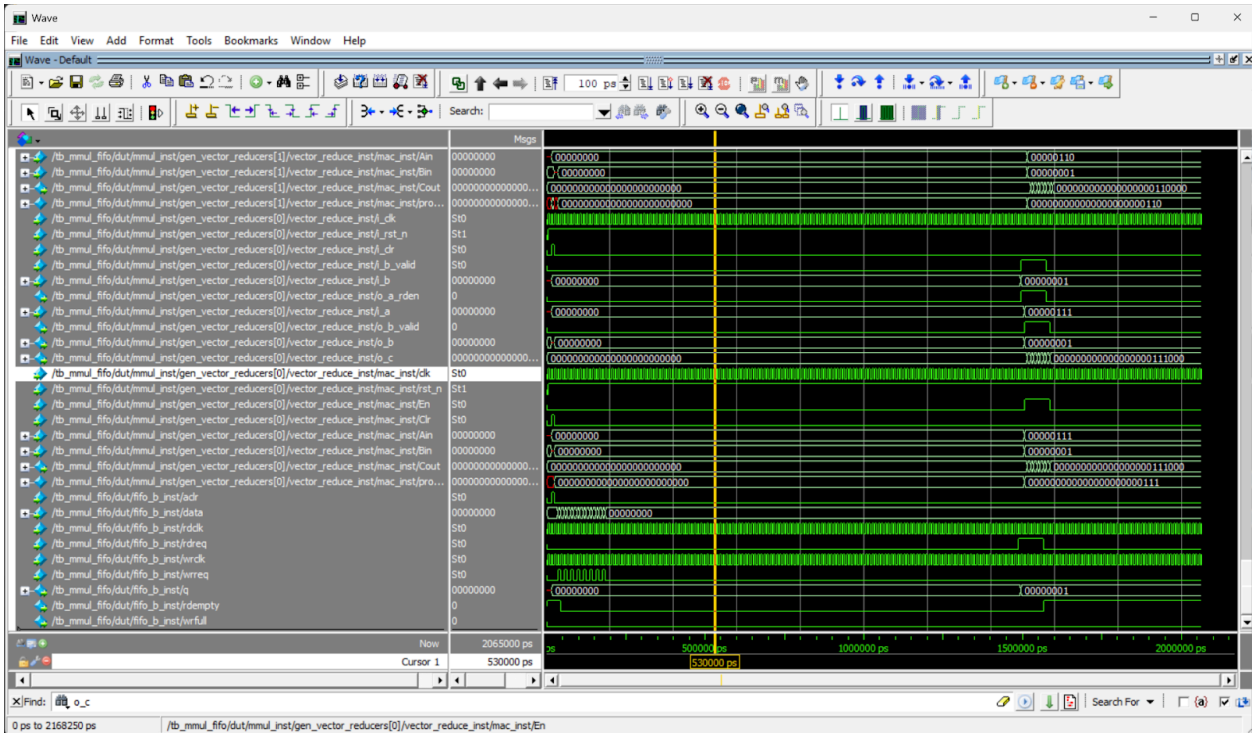
Github → create new → SSH key → connected to it on personal computer → added important files from other folder (organized to be near eachother on personal computer) → and finished

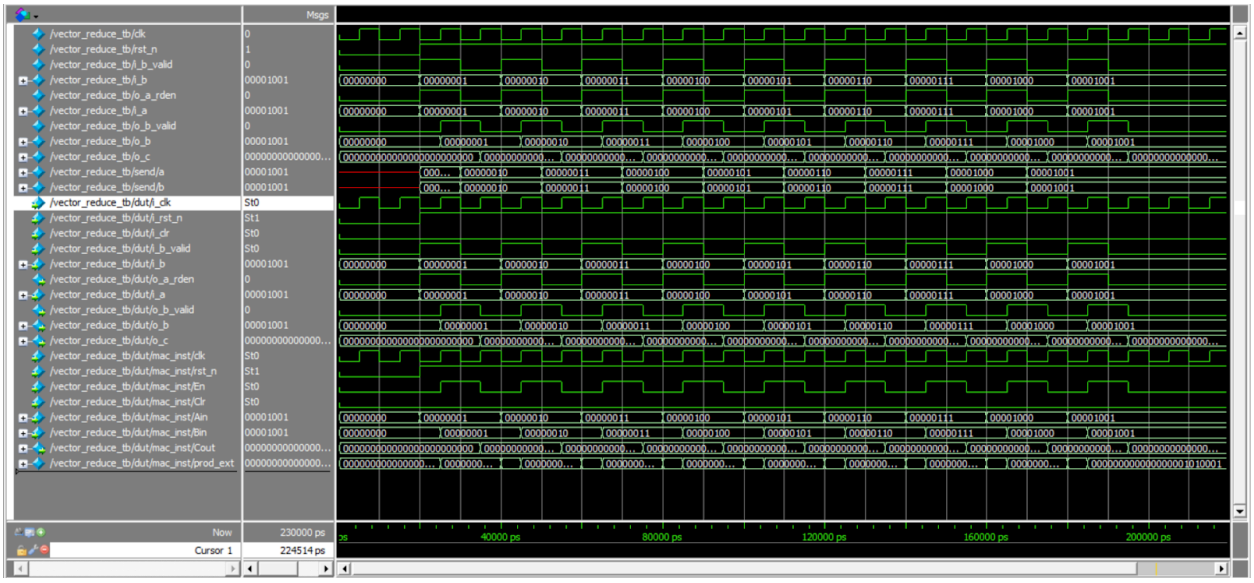
- How you tested the design via simulation (screenshot of waveform)

We did 3 waves of testbenching for this project. The first testbench tested the matrix multiplication with simple inputs (1,1; 2,2 … etc). After that, we tested adding given values to the FIFOs and performing matrix multiplication and accumulation with the FIFOs involved. When that worked, we finally tested everything together: memory module → FIFO → mmul + accumulate. The two biggest issues we dealt with were an off-by-one issue in the 2nd test (we realized that requesting and sending from with the “B FIFO” was flawed) and a truncating issue in the 3rd testbench (this took forever to figure out)




Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
/tb_minilab1/dut/address
/tb_minilab1/dut/read
/tb_minilab1/dut/readdata
/tb_minilab1/dut/readdata_reg
/tb_minilab1/dut/readdatavalid
/tb_minilab1/dut/mmul_fifo_wrapper_inst/i_clk_wr_fifo
/tb_minilab1/dut/mmul_fifo_wrapper_inst/i_clk_mmul
/tb_minilab1/dut/mmul_fifo_wrapper_inst/i_rst_n
/tb_minilab1/dut/mmul_fifo_wrapper_inst/i_en_mmul
/tb_minilab1/dut/mmul_fifo_wrapper_inst/i_clr
/tb_minilab1/dut/mmul_fifo_wrapper_inst/i_a
/tb_minilab1/dut/mmul_fifo_wrapper_inst/i_a_valid
/tb_minilab1/dut/mmul_fifo_wrapper_inst/o_a_full
/tb_minilab1/dut/mmul_fifo_wrapper_inst/i_b
/tb_minilab1/dut/mmul_fifo_wrapper_inst/i_b_valid
/tb_minilab1/dut/mmul_fifo_wrapper_inst/o_b_full
/tb_minilab1/dut/mmul_fifo_wrapper_inst/o_c
/tb_minilab1/dut/mmul_fifo_wrapper_inst/mull_fifo_inst/i_clk_wr_fifo
/tb_minilab1/dut/mmul_fifo_wrapper_inst/mull_fifo_inst/i_clk_mmul
/tb_minilab1/dut/mmul_fifo_wrapper_inst/mull_fifo_inst/i_rst_n
/tb_minilab1/dut/mmul_fifo_wrapper_inst/mull_fifo_inst/i_en_mmul
/tb_minilab1/dut/mmul_fifo_wrapper_inst/mull_fifo_inst/i_clr
/tb_minilab1/dut/mmul_fifo_wrapper_inst/mull_fifo_inst/i_b
/tb_minilab1/dut/mmul_fifo_wrapper_inst/mull_fifo_inst/i_b_valid
/tb_minilab1/dut/mmul_fifo_wrapper_inst/mull_fifo_inst/o_b_full
/tb_minilab1/dut/mmul_fifo_wrapper_inst/mull_fifo_inst/_internal_b_rden
/tb_minilab1/dut/mmul_fifo_wrapper_inst/mull_fifo_inst/_internal_b
/tb_minilab1/dut/mmul_fifo_wrapper_inst/mull_fifo_inst/gen_a_fifos[7]/inst/adr
/tb_minilab1/dut/mmul_fifo_wrapper_inst/mull_fifo_inst/gen_a_fifos[7]/inst/data
/tb_minilab1/dut/mmul_fifo_wrapper_inst/mull_fifo_inst/gen_a_fifos[7]/inst/rdclk
/tb_minilab1/dut/mmul_fifo_wrapper_inst/mull_fifo_inst/gen_a_fifos[7]/inst/rdreq
/tb_minilab1/dut/mmul_fifo_wrapper_inst/mull_fifo_inst/gen_a_fifos[7]/inst/wrclk
Now
6370000 ps
Cursor 1
4410000 ps
1000000 ps
2000000 ps
3000000 ps
4000000 ps
5000000 ps
4410000 ps
Find: o_c
Search For


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
/tb_mmul_fifo/dut/mmul_inst/gen_vector_reducers[1]/vector_reduce_inst/mac_inst/Ain
/tb_mmul_fifo/dut/mmul_inst/gen_vector_reducers[1]/vector_reduce_inst/mac_inst/Bin
/tb_mmul_fifo/dut/mmul_inst/gen_vector_reducers[1]/vector_reduce_inst/mac_inst/Cout
/tb_mmul_fifo/dut/mmul_inst/gen_vector_reducers[1]/vector_reduce_inst/mac_inst/pro...
/tb_mmul_fifo/dut/mmul_inst/gen_vector_reducers[0]/vector_reduce_inst/i_clk
/tb_mmul_fifo/dut/mmul_inst/gen_vector_reducers[0]/vector_reduce_inst/i_rst_n
/tb_mmul_fifo/dut/mmul_inst/gen_vector_reducers[0]/vector_reduce_inst/i_clr
/tb_mmul_fifo/dut/mmul_inst/gen_vector_reducers[0]/vector_reduce_inst/i_b_valid
/tb_mmul_fifo/dut/mmul_inst/gen_vector_reducers[0]/vector_reduce_inst/i_b
/tb_mmul_fifo/dut/mmul_inst/gen_vector_reducers[0]/vector_reduce_inst/o_a_rden
/tb_mmul_fifo/dut/mmul_inst/gen_vector_reducers[0]/vector_reduce_inst/i_a
/tb_mmul_fifo/dut/mmul_inst/gen_vector_reducers[0]/vector_reduce_inst/o_b_valid
/tb_mmul_fifo/dut/mmul_inst/gen_vector_reducers[0]/vector_reduce_inst/o_b
/tb_mmul_fifo/dut/mmul_inst/gen_vector_reducers[0]/vector_reduce_inst/o_c
/tb_mmul_fifo/dut/mmul_inst/gen_vector_reducers[0]/vector_reduce_inst/mac_inst/clk
/tb_mmul_fifo/dut/mmul_inst/gen_vector_reducers[0]/vector_reduce_inst/mac_inst/rst_n
/tb_mmul_fifo/dut/mmul_inst/gen_vector_reducers[0]/vector_reduce_inst/mac_inst/En
/tb_mmul_fifo/dut/mmul_inst/gen_vector_reducers[0]/vector_reduce_inst/mac_inst/Clr
/tb_mmul_fifo/dut/mmul_inst/gen_vector_reducers[0]/vector_reduce_inst/mac_inst/Ain
/tb_mmul_fifo/dut/mmul_inst/gen_vector_reducers[0]/vector_reduce_inst/mac_inst/Bin
/tb_mmul_fifo/dut/mmul_inst/gen_vector_reducers[0]/vector_reduce_inst/mac_inst/Cout
/tb_mmul_fifo/dut/mmul_inst/gen_vector_reducers[0]/vector_reduce_inst/mac_inst/pro...
/tb_mmul_fifo/dut/fifo_b_inst/adr
/tb_mmul_fifo/dut/fifo_b_inst/data
/tb_mmul_fifo/dut/fifo_b_inst/rdclk
/tb_mmul_fifo/dut/fifo_b_inst/rdreq
/tb_mmul_fifo/dut/fifo_b_inst/wrclk
/tb_mmul_fifo/dut/fifo_b_inst/wrreq
/tb_mmul_fifo/dut/fifo_b_inst/q
/tb_mmul_fifo/dut/fifo_b_inst/rdempty
/tb_mmul_fifo/dut/fifo_b_inst/wrfull
Now
2065000 ps
Cursor 1
530000 ps
500000 ps
1000000 ps
1500000 ps
2000000 ps
530000 ps
Find: o_c
Search For
0 ps to 2168250 ps
/tb_mmul_fifo/dut/mmul_inst/gen_vector_reducers[0]/vector_reduce_inst/mac_inst/En



- How you fixed the design to meet the timing constraint

We fixed the design to meet the timing constraint by pipelining the multipliplier as it contained the critical path (which was the only path above 5ns which was required for 200MHz). The path was reduced from 6.9ns to below 5.

Slow 1100mV 85C Model Fmax Summary

<<Filter>>

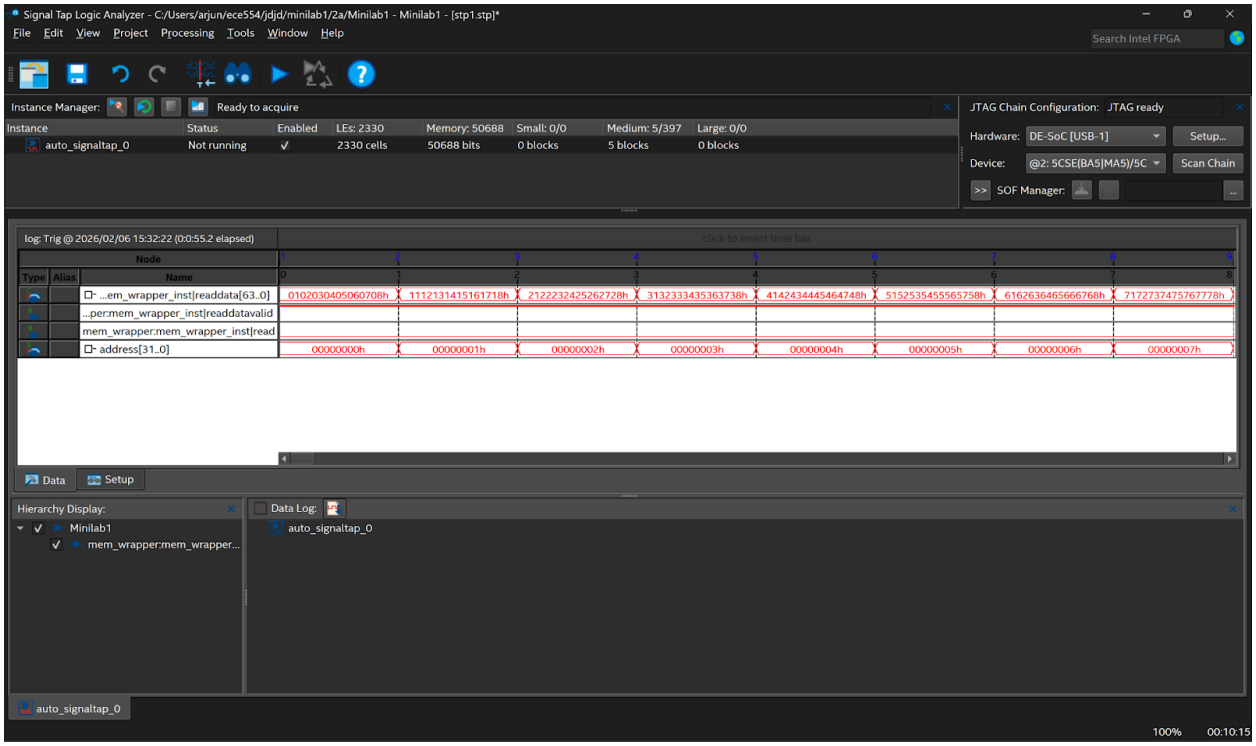
	Fmax	Restricted Fmax	Clock Name	Note
1	51.55 MHz	51.55 MHz	altera...ed_tck	
2	90.49 MHz	90.49 MHz	CLOCK_50	
3	256.41 MHz	256.41 MHz	CLOCK2_50	

- How you tested the design on board using an example and snapshot of the board that shows it

We tested the design on the board by just creating a top level module that connected the necessary ports → read form the memory module and used the information to perform the matri multiplicaiton

- How you tested the design using SignalTap (screenshot of waveform around the trigger condition)

We just followed the video for setup: Tools → SignalTAP → clk → signals → triggers+storage recompile → check values. Specifically we checked the signals of the addresses requested and checked that they matched with the values received to see if the proper requests were being sent in order



- Explain any difficulties that you faced during the whole process and how you overcame it

The main difficulty we dealt with was learning how ModelSim does indexing with arrays (I still don't fully get it but I had an issue with the test bench that resulted with model sim incrementing in an opposite direction than I designed)
Also, debugging the last version of the design was a pain (there was an overflow issue and it took FOREVER to find it)
Both of these issues were dealt with by working together to analyze the waveforms and effects of signals on others. Also syntax searching and Google/Stack overflow helped.
Oh yeah another difficulty was finding time to meet one another → We just communicated via text