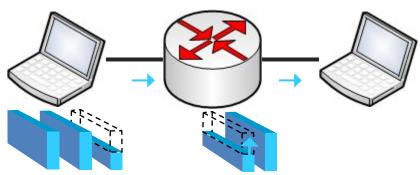


# Forwarding methods

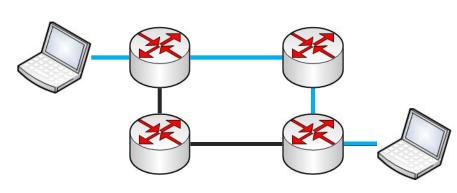


Packet switching

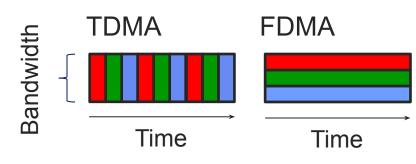


• Store and forward: entire packet must arrive at router before it can be transmitted on next link

Circuit switching



 End-to-end resources reserved for the duration of transmission



# Packet vs. Circuit switching



Which gives better performance in terms of:

- End-to-end delay?
- Flow throughput?
- Network throughput?

#### Packet switching

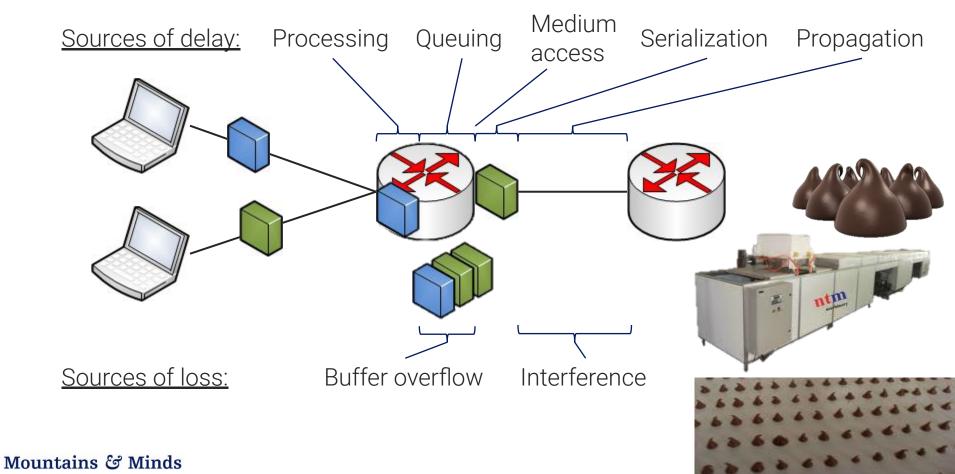
- + More efficient with bursty data
- + Simpler no call setup
- Variable delay
- Need protocols for reliability and congestion control

### Circuit switching

- + Lower end-to-end delay
- Wastes resources during quiet periods
- Need protocols for resource reservation

### Network performance





### Definitions of delay



- Processing delay
  - The time it takes to read an incoming packet, determine on which link to transmit the packet, and to form packet headers.
  - Analogy: The time to set up the chocolate chip making machine.
- Queueing delay
  - The time it takes for the packet to get to the front of the queue.
  - Analogy: The time to finish a run of white chocolate chips to start the regular chips.
- Medium access delay
  - The time a packet has to wait at the front of the queue for the transmission medium to be free.
  - Analogy: Wait for the conveyor to reach the correct speed.
- Serialization delay
  - The time it takes to put all the packet's bits onto the transmission medium.
  - Analogy: The time to drip down a batch of chocolate chips.
- Propagation delay
  - The time it takes for the first bit of a packet to traverse a link
  - Analogy: The time it takes for the first line of chocolate chips to cool before they are packed at the end of the conveyor.

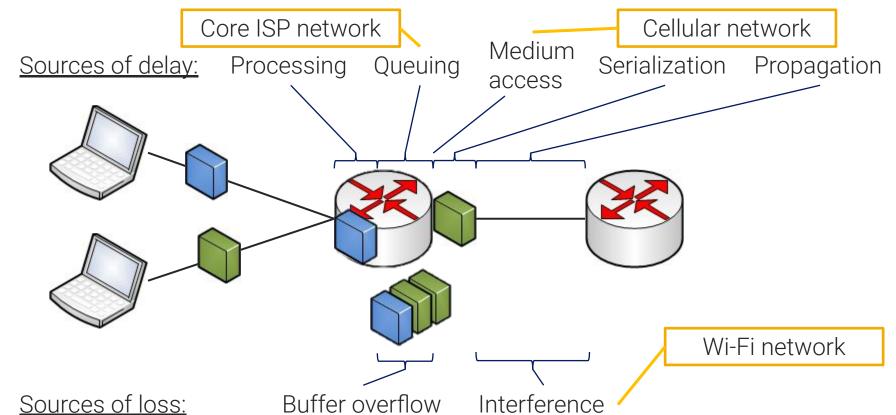
### **Definitions of loss**



- Buffer overflow
  - When the rate of arriving packets exceeds sending rate packets queue up. Eventually the number of queued packets exceeds queue size in router memory and newly arriving packets are dropped.
  - Analogy: The box collecting chips at the end of the conveyor fills up and new chips are dropped on the floor. (No three seconds rule!)
- Interference
  - When a transmitted packet collides with another packet on the transmission medium and neither one can be decoded.
  - Analogy: Someone snags a chip of the conveyor belt.

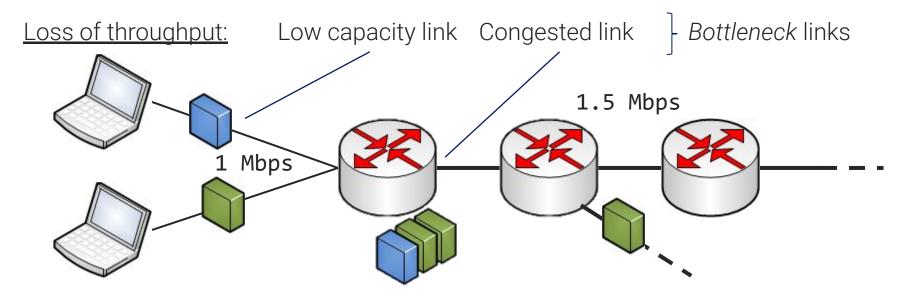
### Likely sources of delay





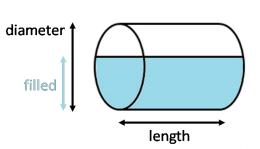
### Network performance





#### Metrics of delivery rate:

- Capacity bandwidth, serialization rate, thickness of the pipe
- Available bandwidth unutilized bandwidth
- Achievable throughput share of capacity achieved by a flow
- Goodput rate of delivered application payload data



# Illustration of queuing delay



B: link bandwidth (bps)

L: packet length (bits)

A: average packet arrival rate

 $LA/B \sim 0$ :

- Small queuing delay

 $LA/B \rightarrow 1$ :

Large queuing delay

LA/B > 1:

- More "work" arriving than can be serviced
- Queuing delay infinite!

average queueing delay Assuming bursty arrival rate, would large router buffers improve, or degrade network performance?

