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Cellular neural network formed by simplified processing elements composed of thin-film transistors

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ABSTRACT

We have developed a cellular neural network formed by simplified processing elements composed of thin-film transistors. First, we simplified the neuron circuit into a two-inverter two-switch circuit and the synapse device into only a transistor. Next, we composed the processing elements of thin-film transistors, which are promising for giant microelectronics applications, and formed a cellular neural network by the processing elements. Finally, we confirmed that the cellular neural network can learn multiple logics even in a small-scale neural network. Moreover, we verified that the cellular neural network can simultaneously recognize multiple simple alphabet letters. These results should serve as the theoretical bases to realize ultra-large scale integration for brain-type integrated circuits.

1. Introduction

Cellular neural networks are neural networks where a neuron is connected only to its neighboring neurons [1,2], which are suitable for integration of electron devices. Until now, the fundamental theory, operation principle, and potential applications, such as signal processing [3], image processing [4], pattern recognition [5], and edge detection [6], have been actively investigated using formal models and numerical simulations. Compared to multi-layer perceptrons [7] or neural networks with a radial basis function [8], one advantage of cellular neural networks is that they are suitable for integration of electron devices. This is because when we assume that neurons are integrated like an array on a wafer, it is convenient that a neuron is connected only to neighboring neurons and not all neurons such as those far from the neuron. However, there are few reports on the actual hardware of cellular neural networks [9,10] likely because conventional circuits of the processing elements, such as neurons and synapses, are complicated, although the network architecture is remarkably simple. For example, more than ten transistors are used in the conventional elements. Therefore, the first objective of this study is to simplify the processing elements.

On the other hand, thin-film technologies are promising for giant microelectronics applications, which may realize three-dimensionally stacked large-area integrated circuits [11]. Although thin-film transistors (TFTs) have been widely utilized for flatpanel displays [12,13], novel killer applications are greatly desired [14]. Therefore, the second objective of this study is to compose cellular neural networks of TFTs as a novel application.

We have developed a cellular neural network formed by simplified processing elements composed of TFTs [15-18]. First, we simplified the neuron circuit into a "two-inverter two-switch circuit" and simplified the synapse device into only a transistor. The network architecture of the cellular neural network and learning principle were also modified to simplify the processing elements. Next, we composed the processing elements of TFTs, which are promising for giant microelectronics applications, and formed a cellular neural network by the processing elements. The fabrication processes of the TFTs were the conventional processes for poly-Si TFTs using excimer laser crystallization [19-21]. Finally, we confirmed that the cellular neural network can learn multiple logics of AND and OR even in a small-scale neural network of 5×5 [17]. Moreover, particularly in this paper, we verify that the cellular neural network can simultaneously recognize multiple simple alphabet letters of "T" and "L" in a slightly larger-scale neural network of 7×7. We also explain the neuron circuit, synapse device, network architecture, learning principle, actual hardware, experimental methods, and results in detail. Although these results are

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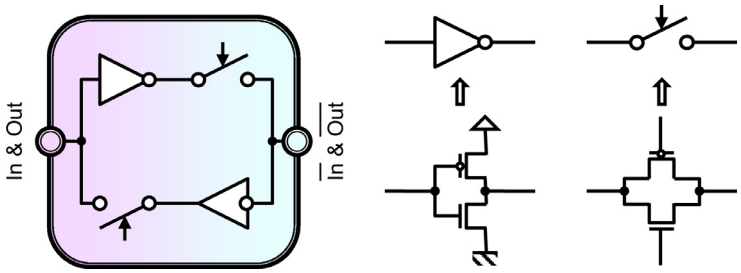

Fig. 1. Neuron circuit.

presently very primitive, we think that they should serve as the theoretical bases to realize ultra-large scale integration for brain-type integrated circuits.

2. Neuron circuit

First, we considered the requisite minimum functions for the neuron element and invented a neuron circuit. The neuron circuit is shown in Fig. 1. The neuron circuit is simplified to a two-inverter two-switch circuit, which is literally a circuit where the two inverters and the two switches are circularly connected. The two terminals are bi-directional, that is, they simultaneously work as both input and output terminals. One terminal is for the positive logic, whereas the other terminal is for the negative logic. The two-inverter two-switch circuit has the requisite minimum functions for the neuron element to: (1) generate and maintain a binary state called the fire and stable states and (2) alternate the binary state according to the input signal. The two inverters generate a binary state. The fire state is defined as the state where the terminal voltages for the positive and negative logics are high and complementarily low, respectively, whereas the stable state is defined as the opposite state. The two inverters are called a latch circuit, which is a well-known circuit for generating and maintaining a binary state. However, it should be noted that the characteristic of a latch circuit is similar to a sigmoid function, which is a typical function used to provide a favorable soft threshold for neural networks. The two switches maintain or alternate the binary state according to the input signal. The binary state is maintained when the two switches are on, whereas the binary state is alternated when the two switches are off and an opposite input signal is received. Because the neuron circuits are made using a complementary transistor circuit, an inverter consists of a pair of n-type and p-type transistors. The switch also consists of a pair of the transistors. Consequently, this neuron circuit consists of eight transistors. On the other hand, the number of the synapses per connected neighboring neuron is two, namely, the synapses for the concordant and discordant connections, as mentioned later.

3. Synapse device

Next, we considered the requisite minimum functions for the synapse element and invented a synapse device. The synapse device is shown in Fig. 2. The synapse device is simplified to only a transistor. The design parameters are optimized to induce the characteristic shift properly. The gate voltage is used as a control voltage to induce or not induce the characteristic shift, and the source and drain terminals are connected to the neurons. The transistor has the requisite minimum functions for the synapse element to: (1) transfer the state signal from a neuron to the neighboring neuron, (2) merge the state signals from multiple neurons for the neuron to alternate the binary state following the majority rule, and (3) control the synaptic connection strength, namely, how the state signal is effectively transferred, on demand. The transistor transfers the state signal as an electric current. The transistor conductance corresponds to the synaptic connection strength. The electric currents are easily added by bundling multiple transistors in parallel, which corresponds to merging the state signals. The characteristic shift depends on the history of the electric current, which corresponds to controlling the synaptic connection strength.

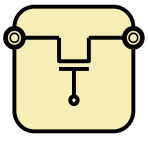

Fig. 2. Synapse device.

4. Network architecture

The network architecture is shown in Fig. 3. The entire architecture is shown in the left figure, and the local connections are shown in the right figure. The cellular neural networks are neural networks where a neuron is connected only to its neighboring neurons. Thus, each neuron is connected through synapses to four neighboring neurons, namely, the upper, lower, left, and right neurons. There are two types of synapse connections, that is, concordant and discordant connections. A concordant connection connects two terminals for the same logics in two neurons, namely, positive and positive logics or negative and negative logics, and tends to make the same binary states in the two neurons. On the other hand, a discordant connection connects two terminals for the different logics in two neurons, namely, positive and negative logics, and tends to make the different binary states in the two neurons. In other words, only by changing the connection, the synapses of the same simplified structure can be either a concordant or discordant connection. The two types of synapse connections are prepared to induce a practical effect that the relative synaptic connection strength becomes both stronger and weaker even if the actual synaptic connection strength becomes either stronger or weaker. For example, the relative synaptic connection strength becomes stronger if the discordant connection becomes weaker.

The electric currents from the neighboring neurons are weighted by the transistor conductance as the synaptic connection strength. The electric currents from the four neighboring neurons, namely, the upper, lower, left, and right neurons, through the two types of synapse connections, namely, the concordant and discordant connections, are summed and sent to the target neuron. The target neuron maintains or alternates the binary state according to the electric current, that is, the target neuron is subject to the majority rule of multiple signals with weighted strengths. Moreover, it should be noted that this neural network is a kind of interconnective neural network where a synapse connection simultaneously transfers a signal from one neuron to another neuron and from the latter neuron to the former neuron, which may correspond to the function of two synapse connections and compensate for the small number of the synapse connections. In any case, we successfully

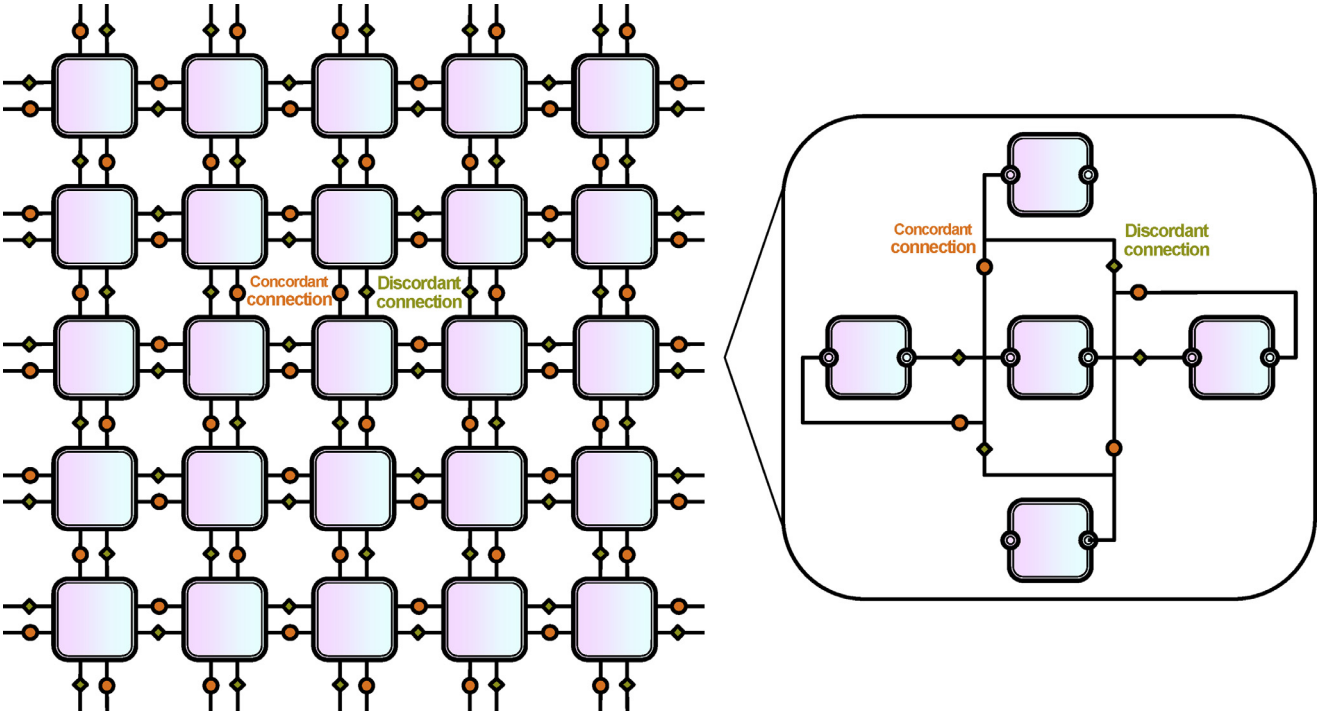

Fig. 3. Network architecture.

created an interconnective neural network where each neuron is connected only to four neighboring neurons, which is exceedingly suitable for integration of electron devices.

5. Learning principle

Hebbian learning is a typical learning procedure in biological and artificial neural networks [22]. The synaptic connection strength is enhanced when both neurons connected to the synapse connection are in the fire state but impaired otherwise. Since the processing elements, such as a neuron and a synapse, are dramatically simplified, the leaning principle is also modified. Modified Hebbian learning is shown in Fig. 4. "F" means the fire state, while "S" means the stable state. As an example, consider the NOT logic. The left and right neurons are assigned to the input and output elements, respectively. Initially, in the initial recalling stage, a stable state is applied to the input element, and a stable state arises from the output element, and vice versa because the synaptic connection strength of the concordant connection is accidentally slightly stronger than that of the discordant connection, which is not the NOT logic. Next, in the first learning stage, a stable state is applied to the input element, and a fire state is applied to the output element. Since the concordant connection connects the two terminals for the same logic in the two neurons and the binary states at both terminals in the two neurons are different, the electric current flows through the concordant connection due to the voltage difference, but the electric current does not flow through the discordant connection. Consequently, the characteristic shift gradually occurs only in the concordant connection, which is a necessary property of our synapses [23-25], the transistor conductance gradually decreases, and only the synaptic connection strength of the concordant connection gradually weakens. In the second learning stage, a fire state is applied to the input element, and a stable state is applied to the output element. Similarly, only the synaptic connection strength of the concordant connection gradually weakens. Finally, in the final recalling stage, a stable state is applied to the

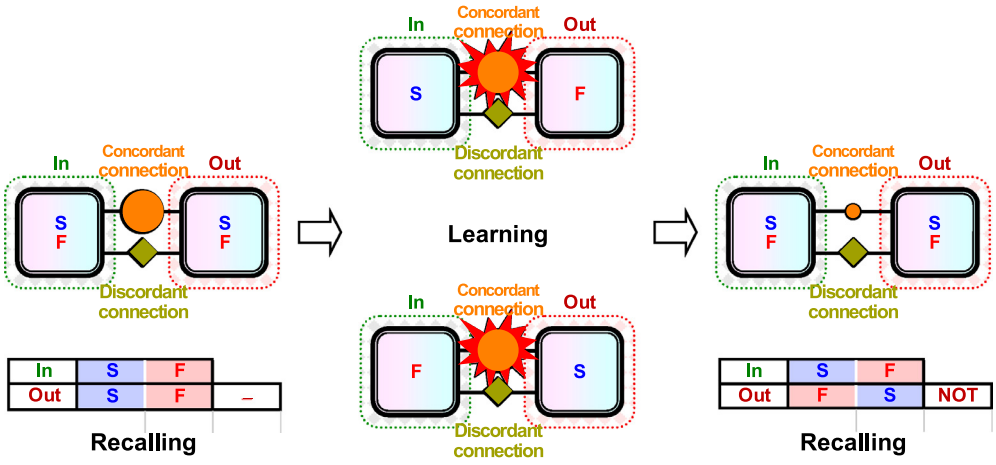

Fig. 4. Modified Hebbian learning.

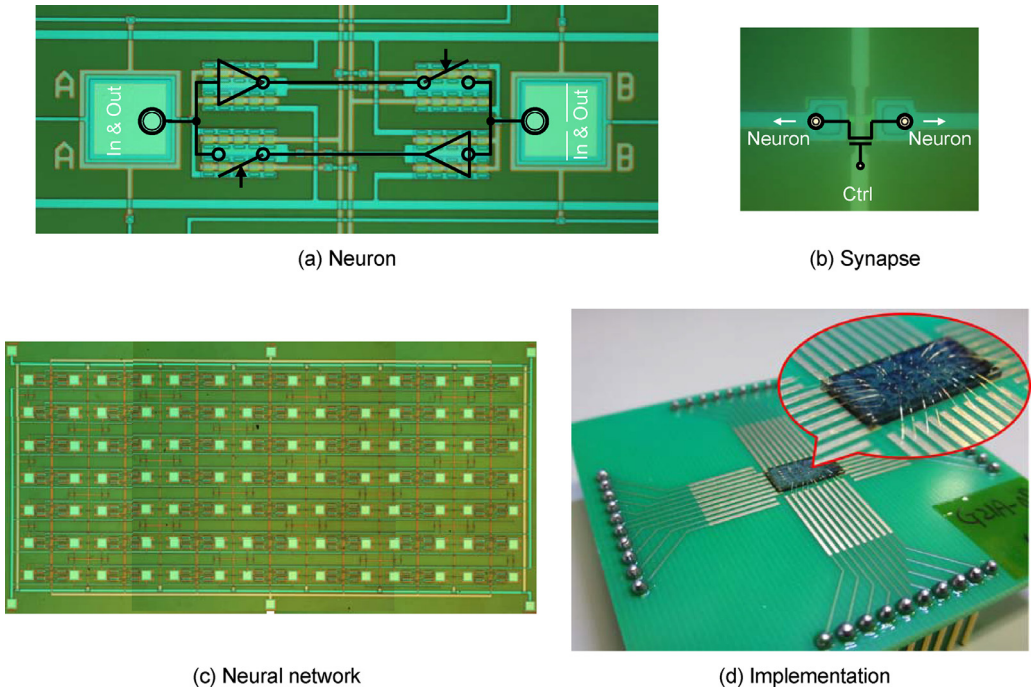

Fig. 5. Actual hardware.

input element, and a fire state arises from the output element, and vice versa because the synaptic connection strength of the concordant connection becomes slightly weaker than that of the discordant connection, which is the NOT logic. It should be noted that because the characteristic shift usually occurs in the direction of the characteristic degradation in the transistors, the absolute value of the synaptic connection strength cannot be enhanced even if both neurons connected to the synapse connection are in the fire state, but the relative values of the synaptic connection strength can be enhanced. This is why we refer to it as modified Hebbian learning. In any case, by employing modified Hebbian learning and the characteristic shift of the transistor, we successfully create a synapse device that consists of just one transistor.

6. Actual hardware

We compose the processing elements of TFTs, which are promising for giant microelectronics applications, and form a cellular neural network by the processing elements. Thin-film devices, including TFTs, are expected to be key technologies for giant microelectronics, because micro-size electron devices can be fabricated on large and inexpensive substrates. Although the device dimensions are on the μm order in this development, they can be on the nm order [26]. In this development, the thin-film devices are fabricated on a glass substrate, but they can also be fabricated on plastic films [27], which can be folded down to a compact size similar to a human brain. Therefore, we believe that thin-film devices are the most promising electron devices for cellular neural networks.

The fabrication processes of the TFTs are the conventional processes for poly-Si TFTs using excimer laser crystallization [19-21]. First, an amorphous-Si film is deposited using low-pressure chemical vapor deposition (LPCVD) of Si_2H_6, crystallized using a XeCl excimer pulse laser, and patterned to form 50-nm-thick poly-Si films, which are used as the channels for the transistors. Next, a SiO_2 film is deposited using plasma-enhanced chemical vapor deposition (PECVD) of tetraethyl orthosilicate (TEOS) to form a 75-nm-thick insulator film, which is used as the gate-insulator films for the transistors. Afterward, a first metal film is deposited and patterned, which is used as both the gate terminals for the transistors and the first electrode wires. Subsequently, phosphorous and boron are implanted into the poly-Si films and thermally activated to form doping regions, which are used as the source and drain regions for the transistors. Next, a SiO_2 film is deposited to form an insulator film, which is used as the interlayer-insulator film. After that, a second metal film is deposited and patterned, which is used as both the source and drain terminals for the transistors and the second electrode wires. Finally, a water-vapor heat treatment is performed to improve the poly-Si films, the SiO_2 film, and their interfaces. The field effect mobility and threshold voltage of the n-type transistors are 93 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and 3.6 V, respectively, while those of the p-type transistors are 47 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and −2.9 V, respectively. These parameters are sufficient for the circuits in the cellular neural network.

The actual hardware is shown in Fig. 5. Microscope photographs of the neuron, synapse, and neural network composed of TFTs and the implementation overview are shown. The n-type transistors in the neuron circuits have a gate width (W) = 100 μm, gate length (L) = 7.5 μm, and lightly-doped drain length (LDD) = 0.75 μm, whereas the p-type transistors have the same W, L = 5 μm, and a single drain structure. The LDD structure is employed to avoid the characteristic shift. On the other hand, the n-type transistor as the synapse device has W = 5 μm, L = 7.5 μm, and a single drain structure. The single drain structure is employed to induce the characteristic shift. The actual chip is die-bonded on a printed circuit board and wire-bonded to metal contacts.

Modified Hebbian learning can be realized using the characteristic shift of the TFTs as synapses. The transistor conductance of the concordant connection is kept the same when both neurons connected to the synapse connection are in the same binary states but impaired otherwise. In contrast, the transistor conductance of the discordant connection is kept the same when both neurons are in different binary states but impaired otherwise. This is because electric current flows between the source and drain terminals owing to the voltage difference in the TFT for the concordant connection when both neurons are in different binary states

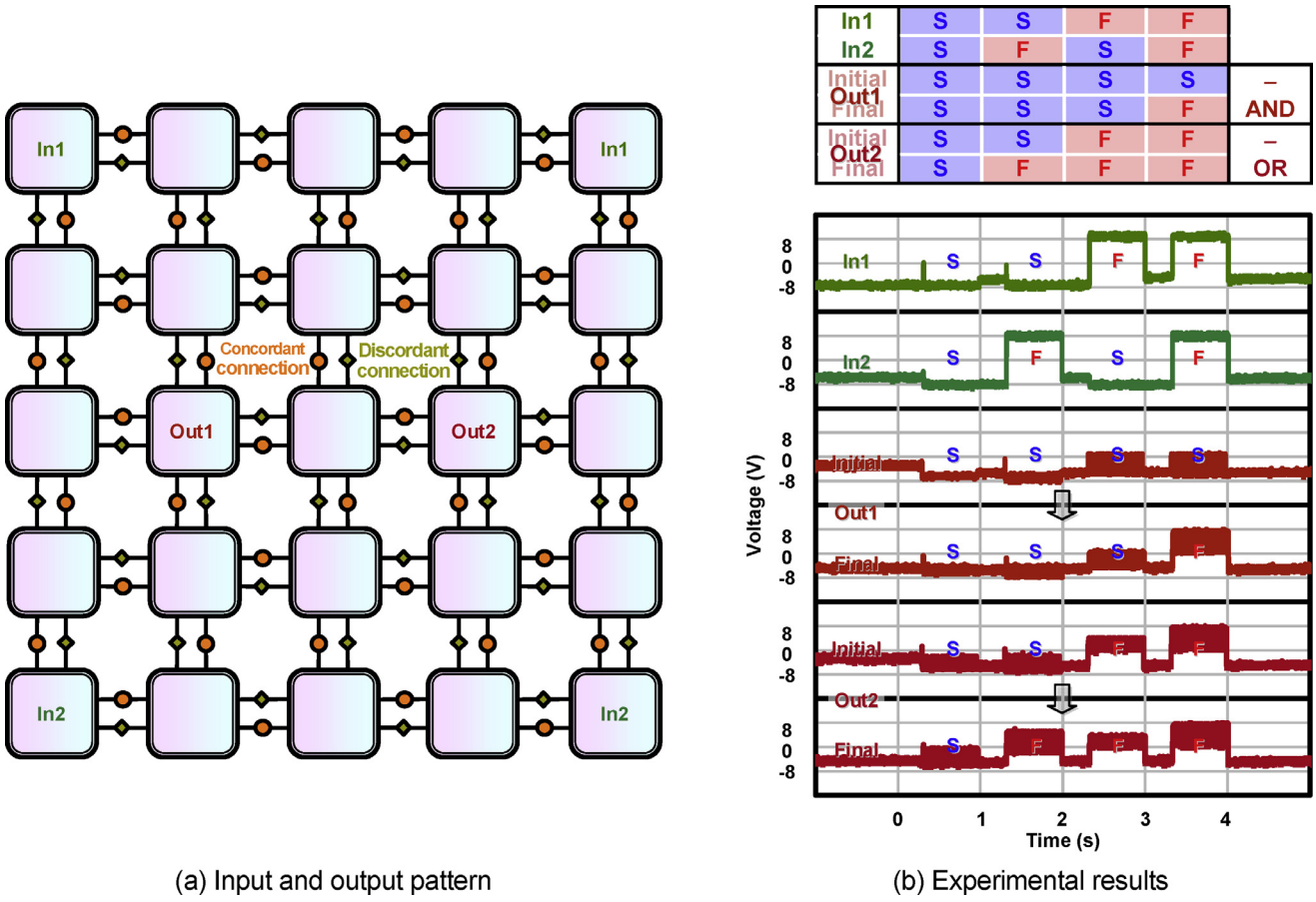

Fig. 6. Logic learning.

and for the discordant connection when both neurons are in the same binary states. The characteristic shift is induced owing to the Joule-heating and hot-carrier degradations by the electric currents [23-25].

7. Logic learning

We confirmed that the cellular neural network can learn multiple logics of AND and OR even in a small-scale neural network of 5×5 [17]. The input and output pattern for the logic learning is shown in Fig. 6(a). The cellular neural network has 5×5 neurons, including four input neurons, to which the input signals are inputted, and two output neurons, from which the output signals are outputted. The four input neurons are assigned to two pairs of In1 and In2, and the two output neurons are assigned to Out1 and Out2. The learning procedure is as follows. VDD = ±8 V and VSS = −8 V are applied as voltage sources for the inverters in the neuron circuits. Therefore, either ± 8 V is inputted to and outputted from the terminals. First, in the learning stage, a high control voltage of 15 V is applied to the synapse TFTs to induce the characteristic shift. Four combinations of the input patterns of the high (H) and low (L) voltages for the two input logic are inputted to In1 and In2, and the corresponding outputs of AND and OR are inputted to Out1 and Out2. Next, switching pulses are periodically applied to repeat the switch on and off of the two switches in the neuron circuits. A steady pattern of the binary states is generated in all neurons based on the normal theory of dynamics of neural networks. After that, the synaptic connection strengths are changed, obeying modified Hebbian learning. Finally, in the recalling stage, a low control voltage of 10 V is applied to avoid the characteristic shift. Four combinations of the input patterns are inputted to In1 and In2, and the output voltages generated from the neural network are measured at Out1 and Out2. Because all the neurons and synapses simultaneously work, it can be said that full parallel processing of neural network is achieved.

The experimental results of the logic learning is shown in Fig. 6(b). It is found that at the initial recalling stage, the wrong output signals are generated from Out1 and Out2. On the other hand, at the final recalling stage, the correct output signals corresponding outputs of AND and OR are generated from Out1 and Out2, respectively. In addition to this example, it is confirmed that the learning is successful in most cases although the times until the correct output signals are generated is widely distributed, namely, ranging from several to several hundred times. Incidentally, as shown in Fig. 6(b), the response time, that is, the rising and falling time, is very quick and sufficient for most anticipated applications of cellular neural networks.

8. Letter recognition

We verified that the cellular neural network can simultaneously recognize multiple simple alphabet letters of “T” and “L” in a slightly larger-scale neural network of 7×7. The input and output pattern for the letter recognition is shown in Fig. 7(a). The cellular neural networks has 7×7 neurons, including 3×3 input/output (I/O) neurons, to which the letter pattern is inputted and from which the generated pattern is outputted, and hidden neurons between them. The learning procedure is as follows. VDD = ±8 V and VSS = −8 V are applied as voltage sources for the inverters in the neuron circuits. Therefore, either ± 8 V is inputted to and out-

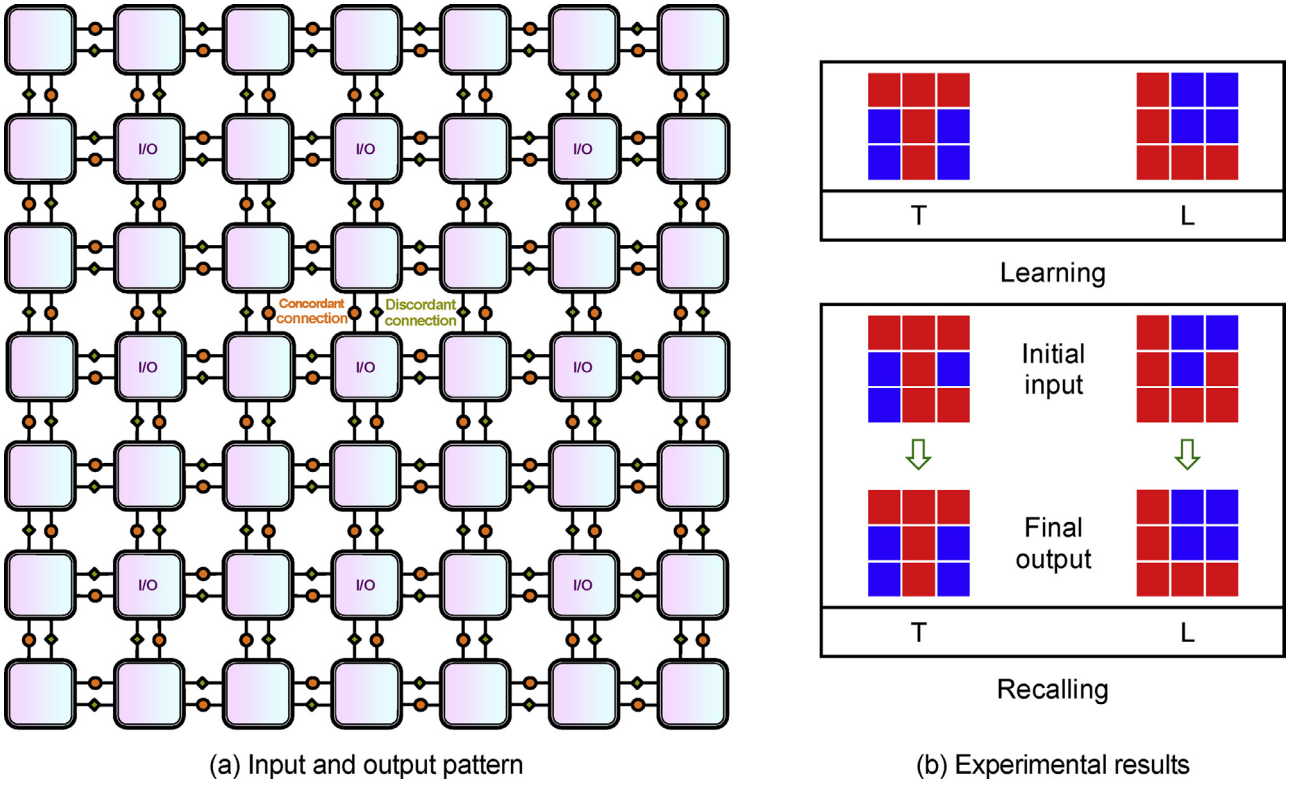

Fig. 7. Letter recognition.

putted from the terminals. First, in the learning stage, a high control voltage of 15 V is applied to the synapse TFTs to induce the characteristic shift. A letter pattern is inputted to the terminals for the positive logic in the I/O neurons as an input pattern of H and L voltages. Next, switching pulses are periodically applied to repeat the switching on and off of the two switches in the neuron circuits. A steady pattern of the binary states is generated in the hidden neurons based on the normal theory of dynamics of neural networks. After that, the synaptic connection strengths are changed, obeying modified Hebbian learning. Finally, in the recalling stage, a low control voltage of 10 V is applied to avoid the characteristic shift. A letter pattern with a slightly wrong part is initially inputted to the I/O neurons and immediately released, and an output pattern is automatically outputted from the I/O neurons. It is checked whether the output pattern is the same as the input pattern.

The experimental results of the letter recognition is shown in Fig. 7(b). Only the states in the 3×3 I/O neurons are shown, although hidden neurons exist between them. First, letter patterns of "T" and "L" are repeatedly inputted to the I/O neurons for several minutes. Finally, letter patterns with slightly different parts from "T" and "L" are initially inputted to the I/O neurons and immediately released, and output patterns are automatically outputted from the I/O neurons. It is confirmed that the output patterns are exactly the same as the letter pattern of "T" and "L" inputted first. This means that the cellular neural network can simultaneously recognize multiple simple alphabet letters of "T" and "L". Once the output patterns are exactly the same as the letter pattern inputted first, it is easy to classify the letters by a logical operation, namely, direct comparison of the letter patterns.

9. Conclusion

We have developed a cellular neural network formed by simplified processing elements composed of TFTs. First, we considered the requisite minimum functions for the neuron element. They are to: (1) generate and maintain a binary state and (2) alternate the binary state according to the input signal. Thus, we simplified the neuron circuit into a two-inverter two-switch circuit. Similarly, we considered the requisite minimum functions for the synapse element. They are to: (1) transfer the state signal from a neuron to the neighboring neuron, (2) merge the state signals from multiple neurons for the neuron to alternate the binary state following the majority rule, and (3) control the synaptic connection strength. Thus, we simplified the synapse device into only a transistor. The network architecture of the cellular neural network was modified, where each neuron is connected to four neighboring neurons through concordant and discordant connections, by which a practical effect that the relative synaptic connection strength becomes both stronger and weaker can be induced even if the actual synaptic connection strength becomes either stronger or weaker. The learning principle was also revised to modified Hebbian learning. The synaptic connection strength of the concordant connection becomes weaker when the binary states of the connected neurons are different, whereas that of the discordant connection becomes weaker when the binary states of the connected neurons are the same. By employing modified Hebbian learning and the characteristic shift of the transistor, we successfully created a synapse device that consists of just one transistor.

Next, we composed the processing elements of TFTs, which are promising for giant microelectronics applications, and formed a cellular neural network by the processing elements. The fabrication processes of the TFTs were the conventional processes for poly-Si TFT using excimer laser crystallization. The transistors in the neuron circuits were designed to avoid the characteristic shift, whereas the transistor as the synapse device was designed to induce the characteristic shift. Modified Hebbian learning can be realized using the characteristic shift of the TFTs used as synapses.

Finally, we confirmed that the cellular neural network can learn multiple logics of AND and OR even in a small-scale neural network of 5×5. Moreover, particularly in this paper, we verified that

the cellular neural network can simultaneously recognize multiple simple alphabet letters of "T" and "L" in a slightly larger-scale neural network of 7×7. Although these results are presently very primitive because the number of the processing elements is small, it is expected that the cellular neural network will acquire various abilities if a lot of processing elements are provided, which is possible because we simplified the processing elements.

In summary, we think that these results should serve as the theoretical bases to realize ultra-large scale integration for brain-type integrated circuits. We are now trying to increase the number of the processing elements to enhance the advanced functions in the cellular neural network. Currently, neural networks are mainly realized using software programs on high-performance hardware, which occupies a lot of space and consumes large power. In the future, when the brain-type integrated circuits are realized, neural networks will be compact and consume little power, enabling the wide implementation of artificial intelligence in actual societies.

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Appendix: Mathematical descriptions

Mathematical descriptions are available to execute logical simulations for design optimization, large-scale integration, etc. in the future. First, as previously mentioned, the requisite minimum functions for the neuron element are to: (1) generate and maintain a binary state and (2) alternate the binary state according to the input signal. On the other hand, the requisite minimum functions for the synapse element are to: (1) transfer the state signal from a neuron to the neighboring neuron, (2) merge the state signals from multiple neurons for the neuron to alternate the binary state following the majority rule, and (3) control the synaptic connection strength. On the basis of these requisite minimum functions, the mathematical description of the state in the neuron is as follows:

$$x(t+1) = S\left(\sum_i \left(w^c{}_i - w^d{}_i\right) x_i(t)\right) \tag{A.1}$$

Here, $x_i(t)$ is the former states in the neighboring neurons, and $x(t \pm 1)$ is the latter state in this neuron, which are either ± 1 for the fire state or -1 for the stable state. $w^c{}_i$ is the synaptic connection strength of the concordant connection, whereas $w^d{}_i$ is that of the discordant connection. Σ sums them for all the neighboring neurons, namely, i is the upper, lower, left, and right directions. S is a special step function where the output is either ± 1 when the input is positive or -1 when the input is negative. By repeating the mathematical calculation for all neurons many times as the dynamics of a neural network, a steady pattern of the binary states is obtained.

Next, as previously mentioned, the learning principle was revised to modified Hebbian learning. The synaptic connection strength of the concordant connection becomes weaker when the binary states of the connected neurons are different, whereas that of the discordant connection becomes weaker when the binary states of the connected neurons are the same. On the basis of these behaviors, the mathematical description of the synaptic connection strength is as follows:

$$\frac{dw^c{}_i}{dt} = -\eta |x - x_i|, \quad \frac{dw^d{}_i}{dt} = -\eta |x - \overline{x_i}| \tag{A.2}$$

Here, $\overline{x_i}$ is the inverted logic of x_i. η is the learning efficiency and depends on the control voltage. It should be noted that these mathematical descriptions are approximate expressions, and the actual behaviors are unveiled only by the experimental results because the cellular neural network is a kind of analog circuit.

References

[1] L.O. Chua, L. Yang, Cellular neural networks: theory, IEEE Trans. Circuits Syst 32 (10) (1988) 1257–1272.
[2] L.O. Chua, T. Roska, Cellular Neural Networks and Visual Computing, Foundations and Applications, Cambridge University Press, Cambridge, UK, 2002.
[3] H. Koeppl, L.O. Chua, An adaptive cellular non-linear network and its application, in: Proceedings of the 2007 International Symposium on Nonlinear Theory and its Applications, NOLTA 2007, Vancouver, Canada, 2007, pp. 15–18.
[4] L.O. Chua, L. Yang, Cellular neural networks: applications, IEEE Trans. Circuits Syst. 35 (10) (1988) 1273–1290.
[5] K.R. Crounse, L.O. Chua, P. Thiran, G. Setti, Characterization and dynamics of pattern formation in cellular neural networks, Int. J. Bifurcation Chaos 06 (09) (1996) 1703–1724.
[6] H. Li, X. Liao, C. Li, H. Huang, C. Li, Edge detection of noisy images based on cellular neural networks, Commun. Nonlinear Sci. Numer. Simul. 16 (2011) 3746–3759.
[7] D.E. Rumelhart, J.L. McClelland, PDP Research Group, Parallel Distributed Processing, The MIT Press, Cambridge, MA, USA, 1986.
[8] D.S. Broomhead, D. Lowe, Radial basis functions, multi-variable functional interpolation and adaptive networks, Royal Signals Radar Establ. Memo. 4148 (1988).
[9] T. Roska, L.O. Chua, The CNN universal machine: an analog array computer, IEEE Trans. Circuits Syst 40 (3) (1993) 163–173.
[10] T. Morie, M. Miyake, M. Nagata, A. Iwata, A 1-D CMOS PWM cellular neural network circuit and resistive-fuse network operation, in: Extended Abstract of the 2001 International Conference on Solid State Devices and Materials, SSDM 2001, Tokyo, Japan, 2001, pp. 90–91.
[11] K. Nomura, T. Aoki, K. Nakamura, T. Kamiya, T. Nakanishi, T. Hasegawa, M. Kimura, T. Kawase, M. Hirano, H. Hosono, Three-dimensionally stacked flexible integrated circuit: amorphous oxide / polymer hybrid complementary inverter using n-type a-In-Ga-Zn-O and p-type poly-(9,9-dioctylfluorene-co-bithiophene) thin-film transistors, Appl. Phys. Lett. 96 (26) (2010) 263509.
[12] Y. Kuo, Thin Film Transistors, Materials and Processes, Vol. 1: Amorphous Silicon Thin Film Transistors, Kluwer Academic Publishers, Dordrecht, The Netherlands, 2004.
[13] Y. Kuo, Thin Film Transistors, Materials and Processes, Vol. 2: Polycrystalline Silicon Thin Film Transistors, Kluwer Academic Publishers, Dordrecht, The Netherlands, 2004.
[14] M. Kimura, T. Matsuda, Device characterizations and novel applications of thin-film transistors, in: Proceedings of the Twentieth International Display Workshops, IDW '13, Sapporo, Japan, 2013, pp. 327–330.
[15] T. Kasakawa, H. Tabata, R. Onodera, H. Kojima, M. Kimura, H. Hara, S. Inoue, An artificial neural network at device level using simplified architecture and thin-film transistors, IEEE Trans. Electron Devices 57 (10) (2010) 2744–2750.
[16] M. Kimura, T. Miyatani, Y. Fujita, T. Kasakawa, Apoptotic self-organized electronic device using thin-film transistors for artificial neural networks with unsupervised learning functions, Jpn. J. Appl. Phys. 54 (3S) (2015) 03CB02.
[17] M. Kimura, Y. Fujita, T. Kasakawa, T. Matsuda, Novel architecture for cellular neural network suitable for high-density integration of electron devices - learning of multiple logics, in: Proceedings of the Twenty-Second International Conference, ICONIP 2015, Neural Information Processing, Part. I, Istanbul, Turkey, 2015, pp. 12–20.
[18] M. Kimura, R. Morita, Y. Koga, H. Nakanishi, N. Nakamura, T. Matsuda, Simplified architecture for cellular neural network suitable for high-density integration of electron devices, in: Proceedings of the 2015 International Symposium on Nonlinear Theory and its Applications, NOLTA 2015, Hong Kong, 2015, pp. 499–502.
[19] T. Sameshima, S. Usui, M. Sekiya, XeCl excimer laser annealing used in the fabrication of poly-Si TFT's, IEEE Electron Device Lett 7 (5) (1986) 276–278.
[20] S. Inoue, M. Matsuo, T. Hashizume, H. Ishiguro, T. Nakazawa, H. Ohshima, Low temperature CMOS self-aligned poly-Si TFTs and circuit scheme utilizing new ion doping and masking technique, in: Technical Digest of the 1991 International Electron Devices Meeting, IEDM '91, Washington, DC, USA, 1991, pp. 555–558.
[21] N. Sano, M. Sekiya, M. Hara, A. Kohno, T. Sameshima, High quality SiO_2/Si interfaces of poly-crystalline silicon thin film transistors by annealing in wet atmosphere, IEEE Electron Device Lett 16 (5) (1995) 157–160.
[22] D.O. Hebb, The Organization of Behavior, Wiley, New York, USA, 1949.
[23] Y. Uraoka, T. Hatayama, T. Fuyuki, T. Kawamura, Y. Tsuchihashi, Hot carrier effects in low-temperature polysilicon thin-film transistors, Jpn. J. Appl. Phys. 40 (4B) (2001) 2833–2836.

[24] S. Inoue, M. Kimura, T. Shimoda, Analysis and classification of degradation phenomena in polycrystalline-silicon thin film transistors fabricated by a low-temperature process using emission light microscopy, Jpn. J. Appl. Phys. 42 (3) (2003) 1168–1172.
[25] T. Kasakawa, H. Tabata, R. Onodera, H. Kojima, M. Kimura, H. Hara, S. Inoue, Degradation evaluation of poly-Si TFTs by comparing normal and reverse characteristics and behavior analysis of hot-carrier degradation, Solid State Electron. 56 (1) (2011) 207–210.
[26] T. Kaneda, D. Hirose, T. Miyasako, P.T. Tue, Y. Murakami, S. Kohara, J. Li, T. Mitani, E. Tokumitsu, T. Shimoda, Rheology printing for metal-oxide patterns and devices, J. Mater. Chem. C 2 (1) (2014) 40–49.
[27] M. Kaltenbrunner, T. Sekitani, J. Reeder, T. Yokota, K. Kuribara, T. Tokuhara, M. Drack, R. Schwoediauer, I. Graz, S. Bauer-Gogonea, S. Bauer, T. Someya, An ultra-lightweight design for imperceptible plastic electronics, Nature 499 (7459) (2013) 458–463.

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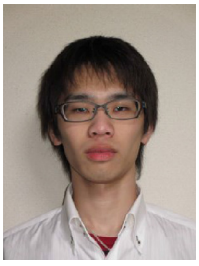

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