



Lab sessions:

Máster en Ingeniería Industrial

Lab session 3: Control of a three-phase inverter connected to the grid

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1. Introduction

During the third lab session the control has been fixed and refined and the power readings Simulink submodule has been added. The following is a brief summary of the work carried out on this third session. The final results of this lab sessions will be presented on the final report.

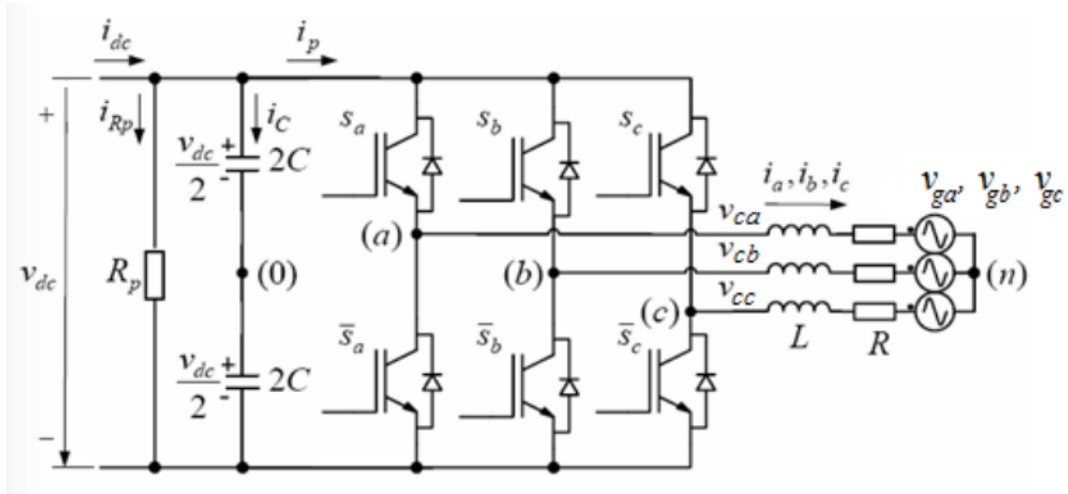


Figure 1.1: Three-phase inverter connected to the grid

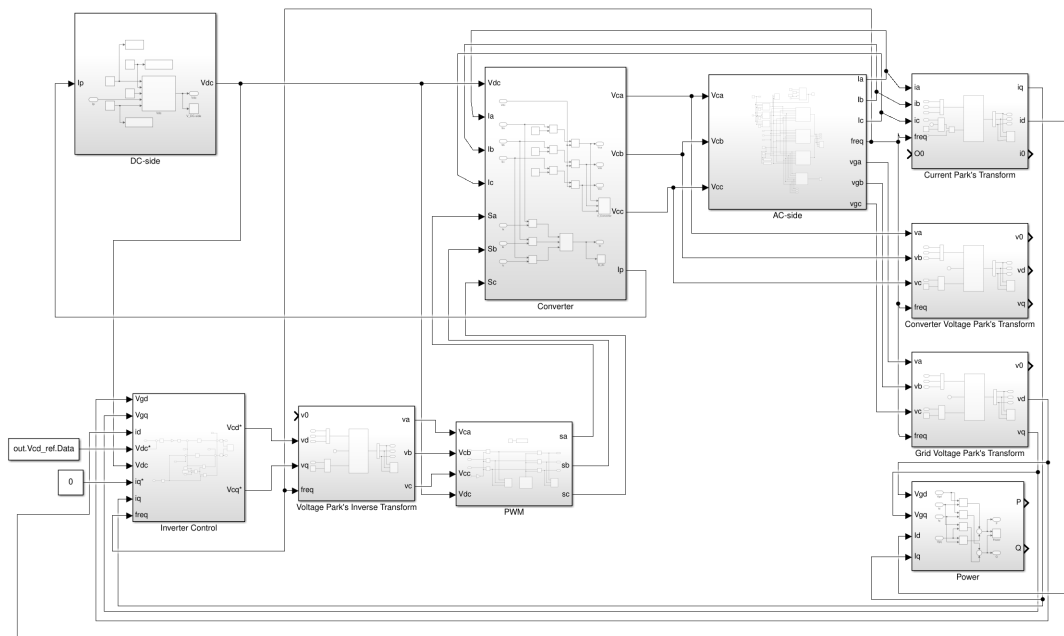
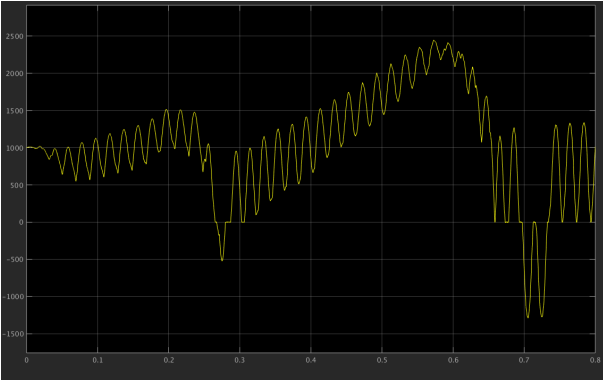


Figure 1.2: Final model after the third lab session

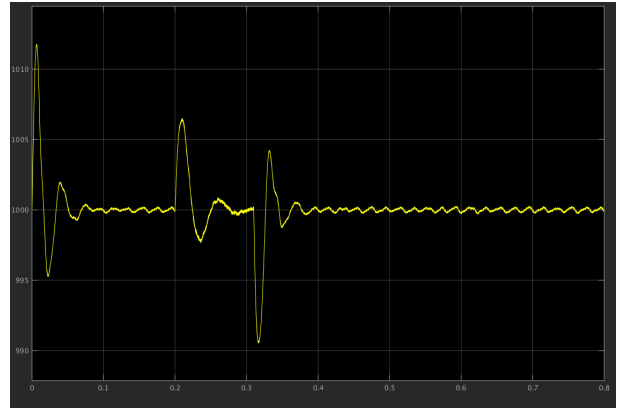
2. Fixing and tuning the control

One of the more important parts of this session was to debug the control. PI constants aside, the biggest problem I was facing was related to the sample time of the simulation, which was set to auto meaning that the model would go out of control due to an uncontrolled time step. This does not mean I changed the converter's frequency to get better results, but I changed the simulation parameters so that the model can run with less error. However this change implies the simulation is now much more expensive in terms of computing in exchange for accuracy.

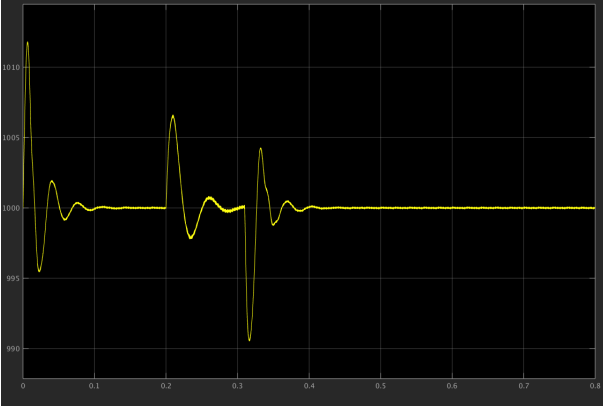
The following is a comparison with no changes to the model, constants or otherwise, of the impact the simulation sample time has on its results.



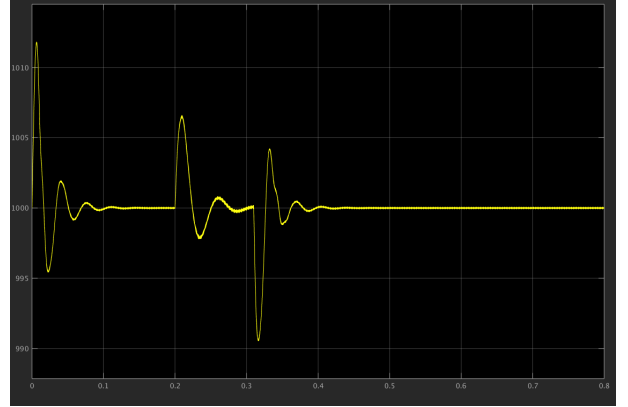
(a) Sample time: 1e-4s



(b) Sample time: 1e-5s



(c) Sample time: 1e-6s



(d) Sample time: 1e-7s

Figure 2.1: Simulation of the voltage read on the DC bus only changing simulation sample time

Finally, I decided to settle for the 1e-7s sample time given that I have enough memory and CPU power to avoid compromising the results.

After the sample time issue was solved the PI controller was much simpler to adjust given that changes on the constants made actual logical sense.

3. Power measurements

Finally I added to the model a Simulink subsystem that measures the active and reactive power.

$$p(t) = v_d * i_d + v_q * i_q$$

$$q(t) = v_q * i_d - v_d * i_q$$

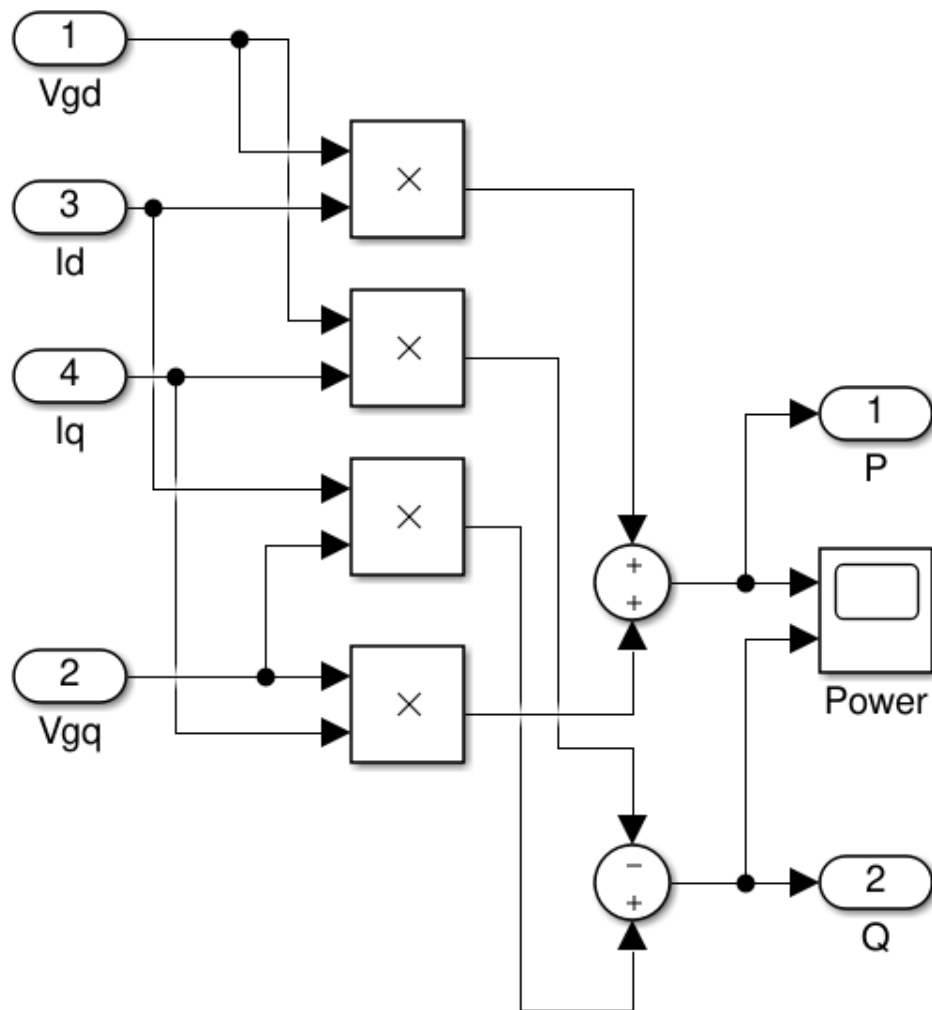


Figure 3.1: Power measurement submodule