

NASSCOM Packaging

Module 1-Packaging evolution: From Basics to 3D Integration

Module 2-From wafer to package: Assembly and Manufacturing Essentials

Module 3-Labs: Thermal simulation of semiconductor Packages with ANSYS

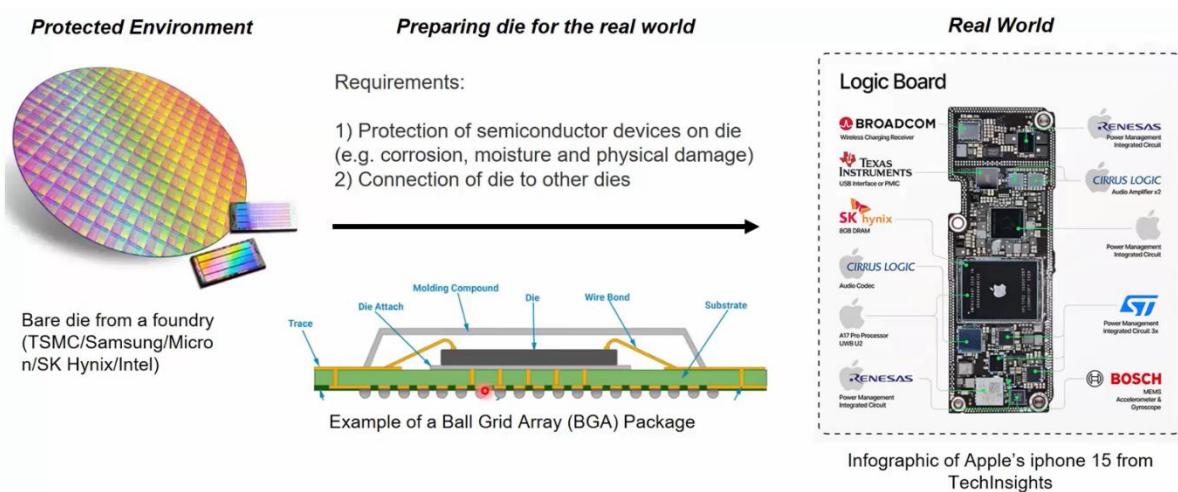
Module 4-Ensuring Packaging Reliability: Testing and Performance Validation

Module 5-Package Design and Modeling: Building a semiconductor package from scratch

Module 1

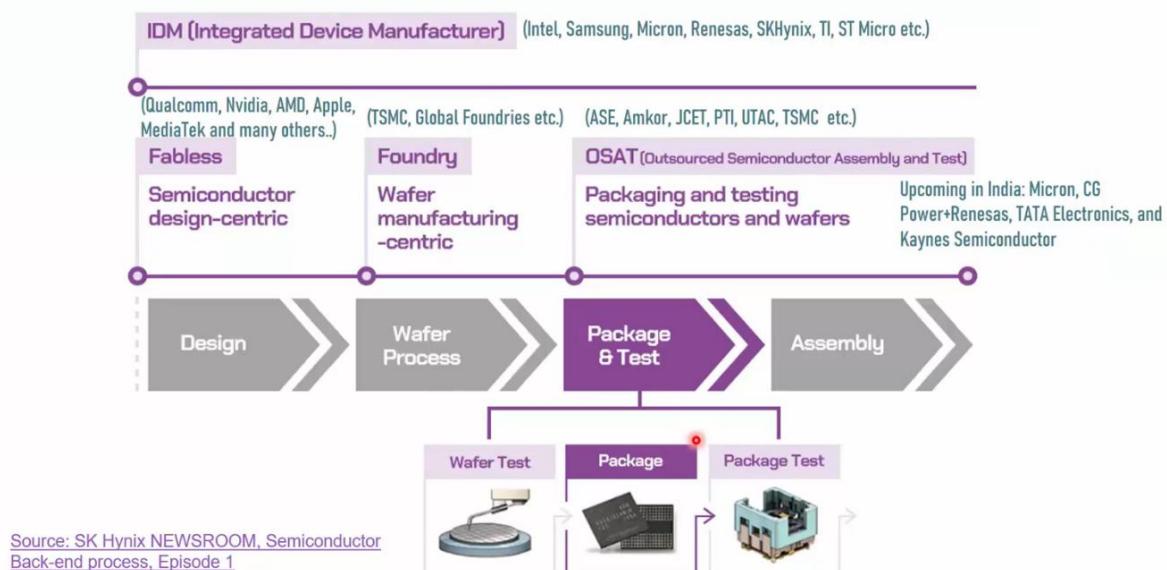
Key topics

1. Why semiconductor packaging required?

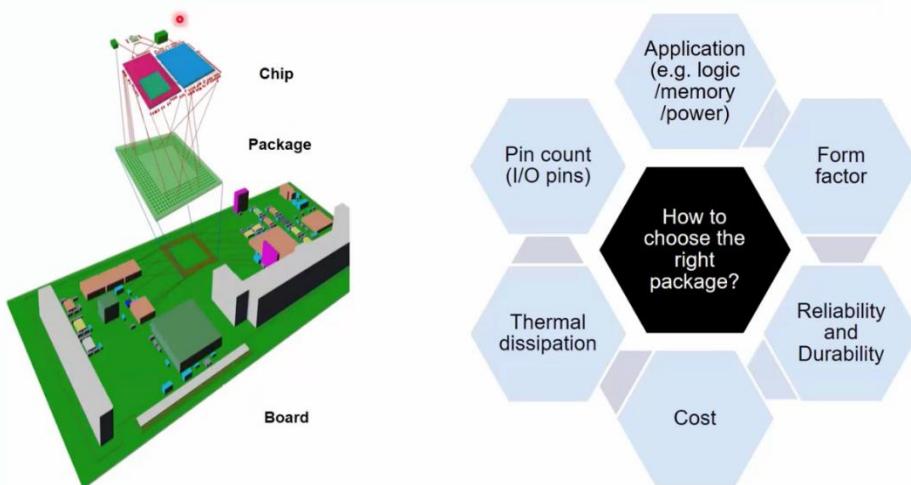


- Packaging can be thought as bringing "*Personality*" to a *skilled die*.

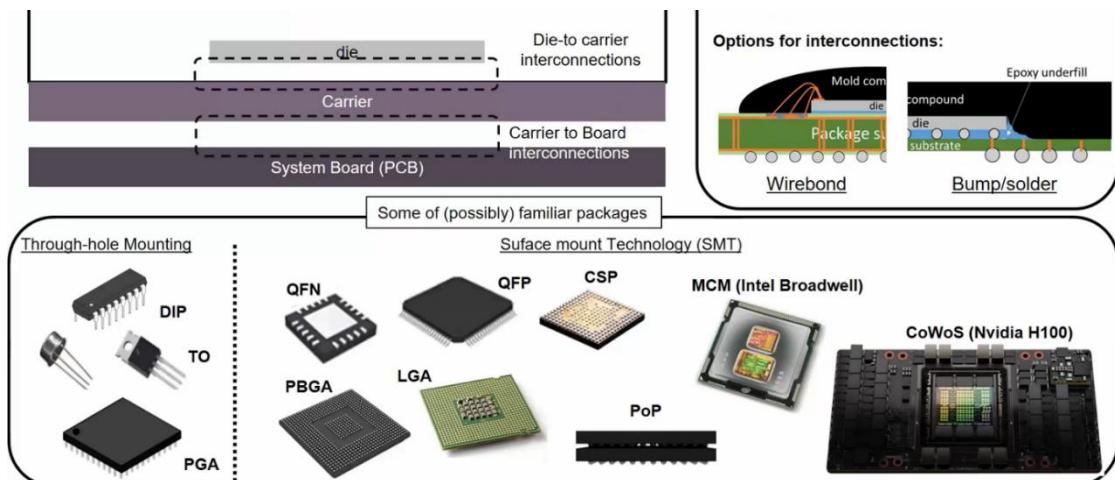
2. Semiconductor Industry: Design to Assembly chain



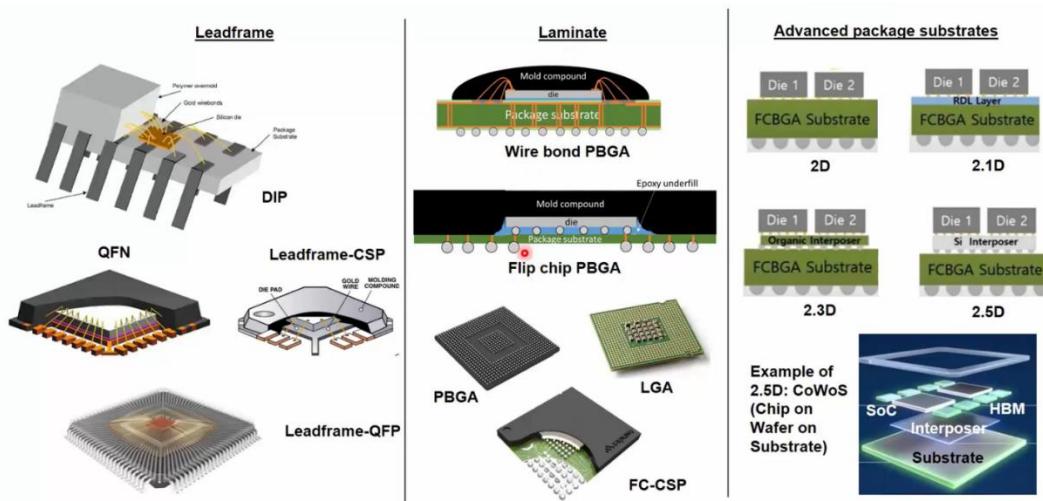
3. Choice of Package



4. IC Package- SMT & Through hole mounting



5. Type of Packages



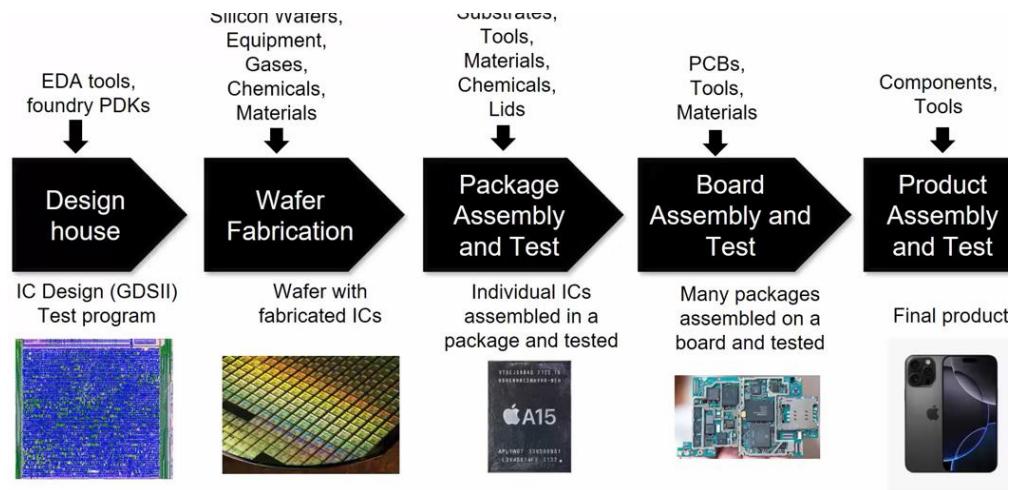
6. Comparison of Packages – Pros, Cons and applications

IC package Type							
Pros	Low cost, easy to manually assemble, durable	Compact, good thermal performance, lightweight	Higher pin density, ease of inspection, ease of solderability	Higher pin count, good electrical and thermal performance	Reduced package size, higher electrical performance at lower cost	Higher level of integration, better performance, and power efficiency	Higher density I/O and routing at lower cost
Cons	Bigger size, low pin count, incompatible with automated assembly	Testing accessibility, Reparability, smaller I/O pins than QFP	Pins susceptible to damage, difficult to repair bent pins	Difficult to inspect and rework, limited shelf life, costlier than QFN	Limited I/O pins, reliability issues (solder joint and warpage)	Longer die-to-die connections	Reliability issues in polymer RDL, lower I/O density than 2.5D
Common Application	Consumer electronics, industrial applications, legacy systems	Smartphone, tablets, automotive, telecommunications	Micro-controllers and micro-processors, ASICs	High performance ICs	Smartphones, IoT, wearable devices	Data centre chips, RF wireless modules, Space avionics	High performance computing segments

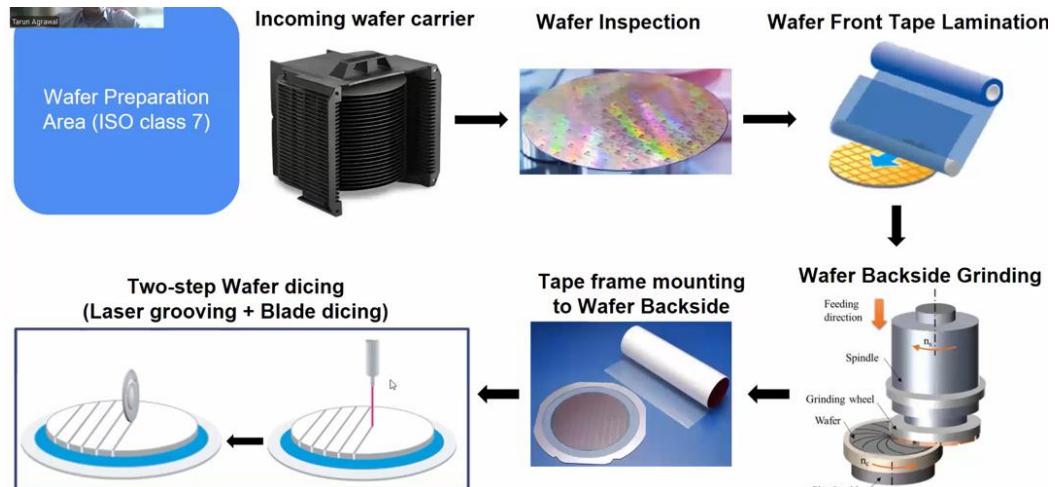
Module 2

Key topics

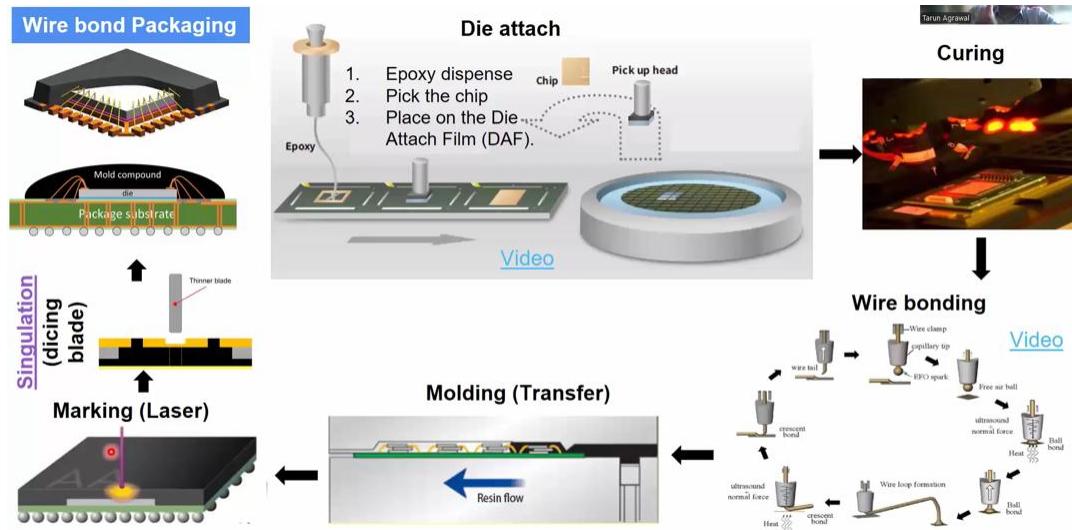
1. Semiconductor IC chip supply chain



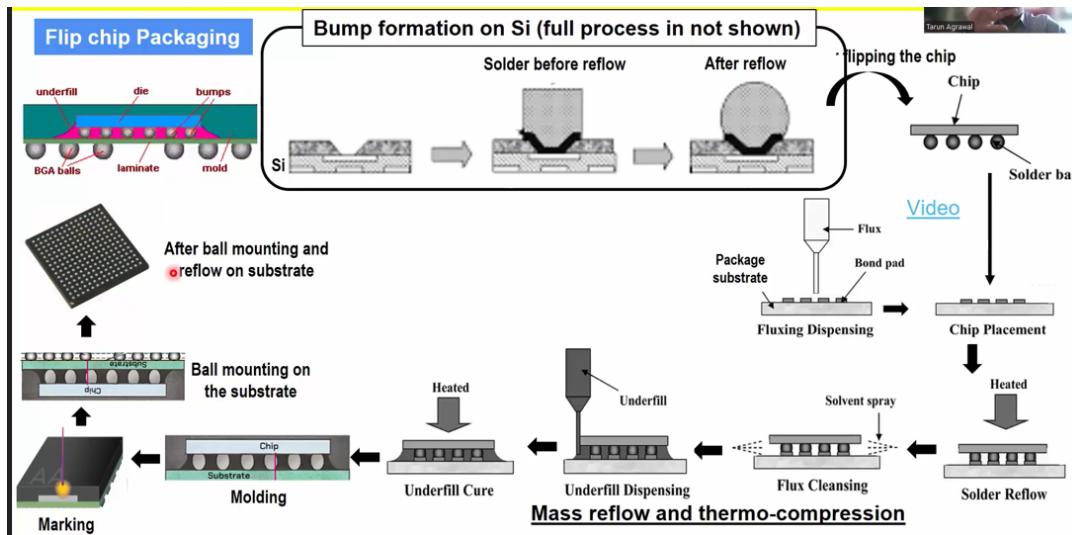
2. Wafer pre-preparation steps - Grinding & Dicing



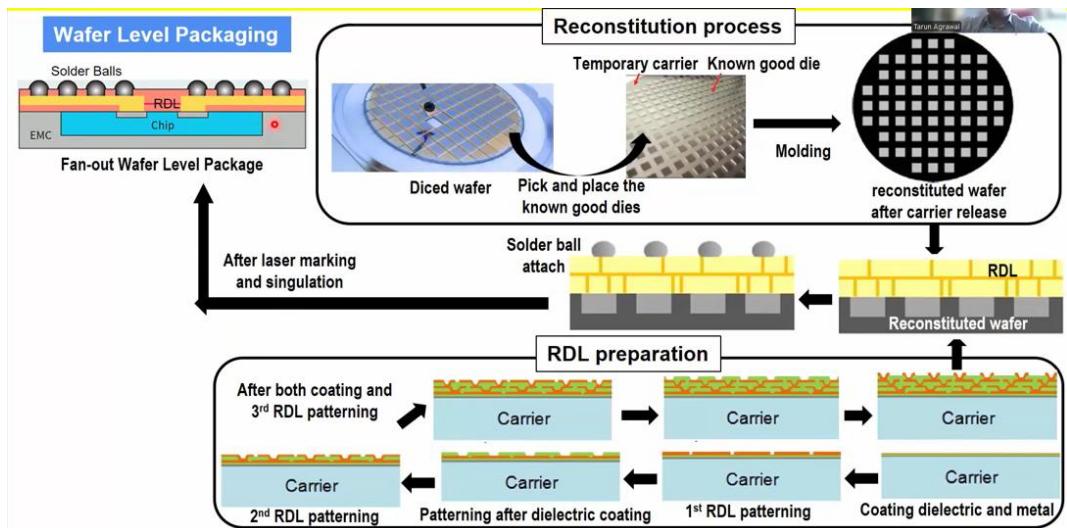
3. Wire Bond Packaging - Die Attach to Die Molding process



4. Flip Chip (FC) Assembly - Bump Formation And Underfill material



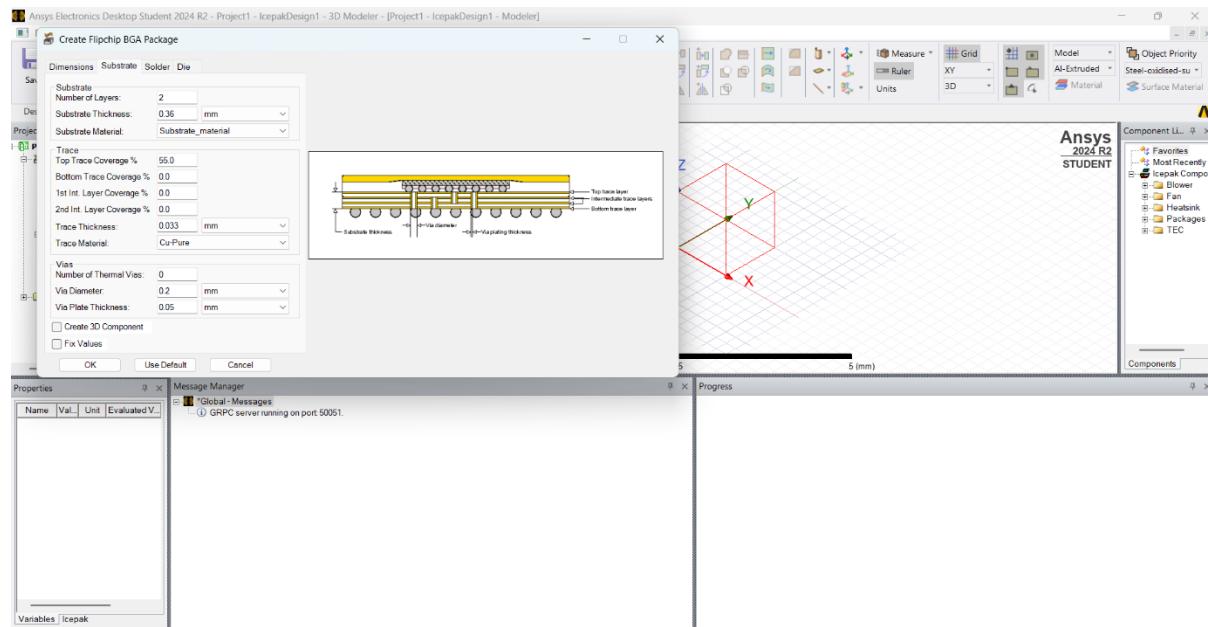
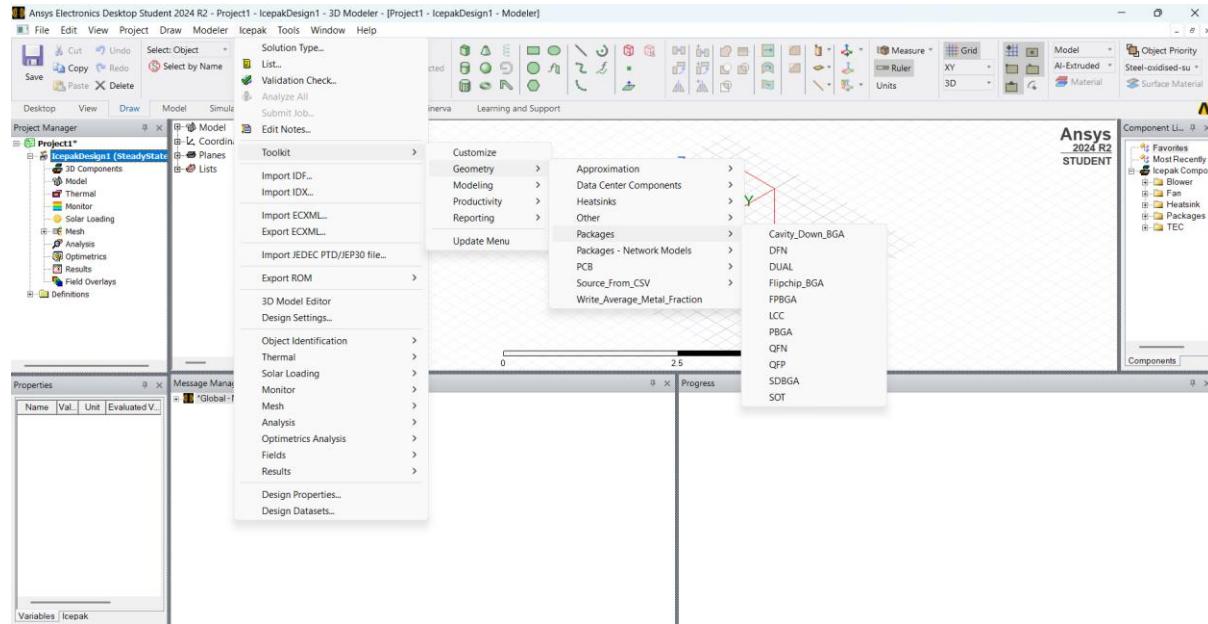
5. Wafer level packaging (WLP)

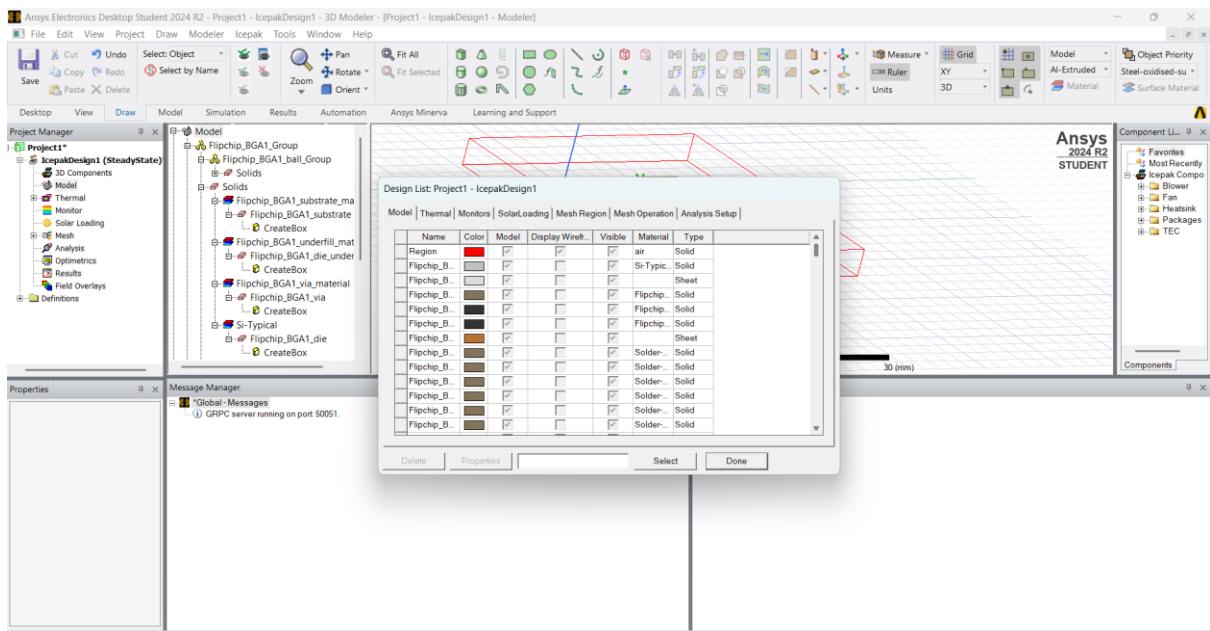
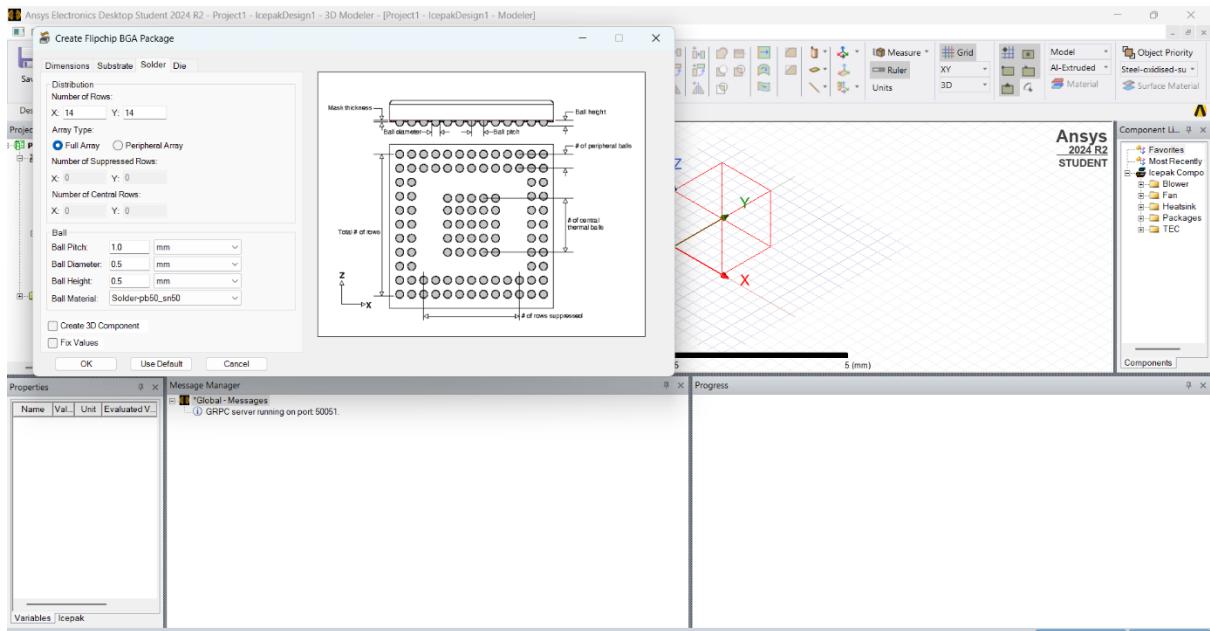


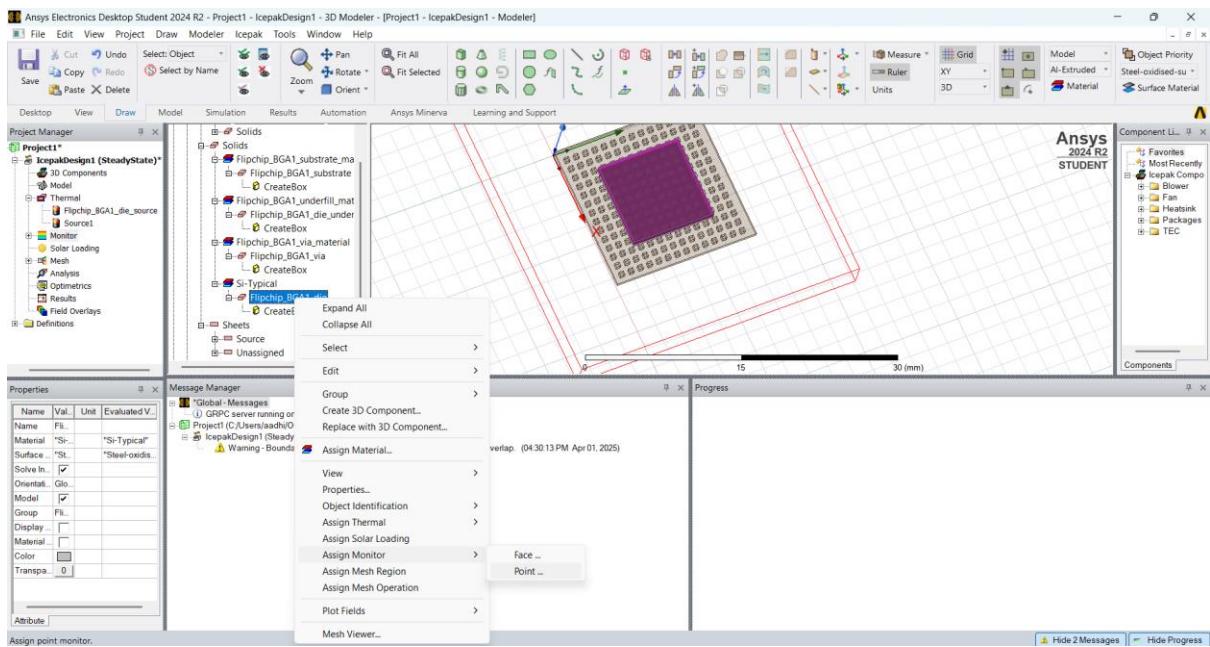
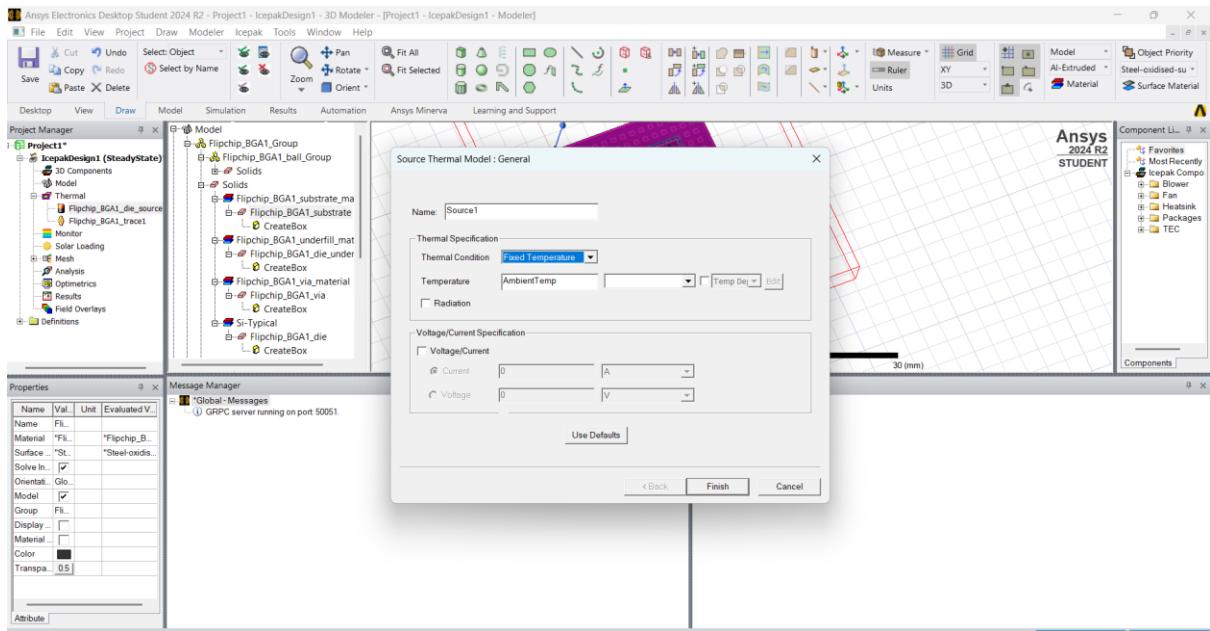
Module 3 (Lab)

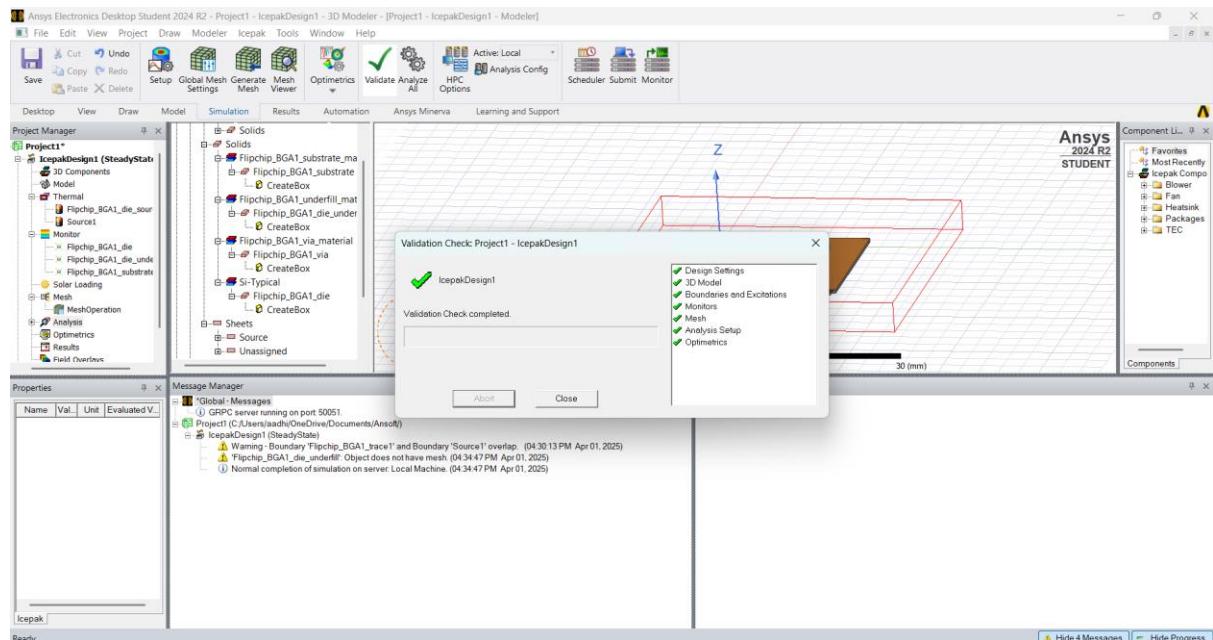
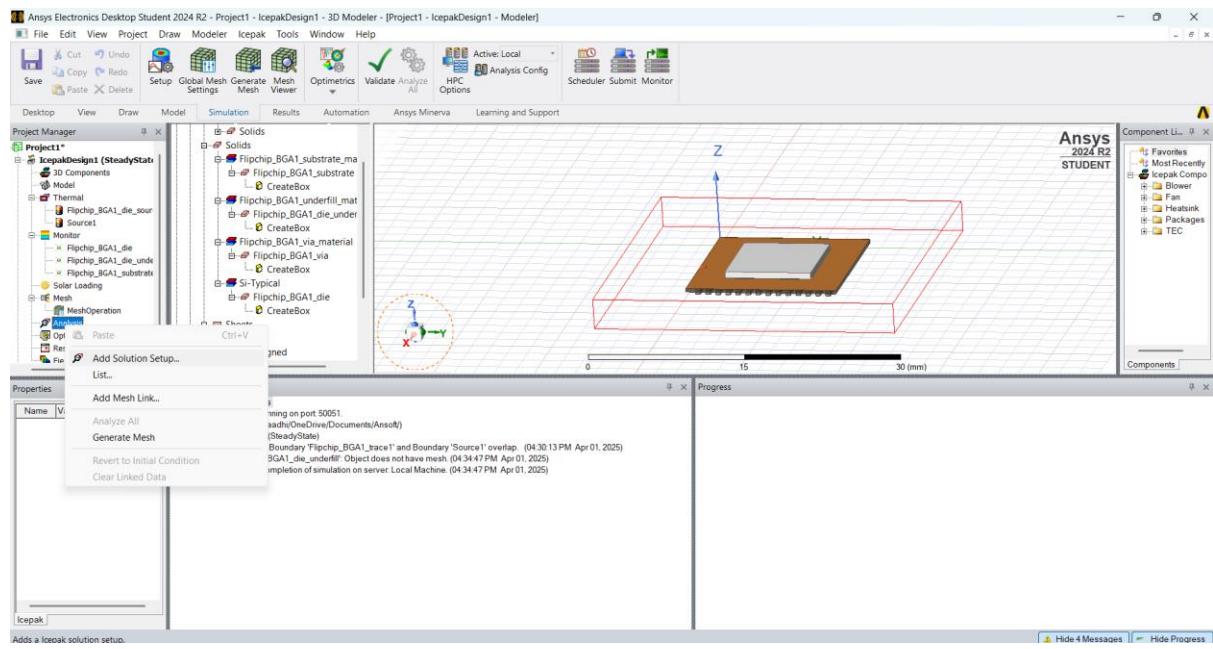
Key topics

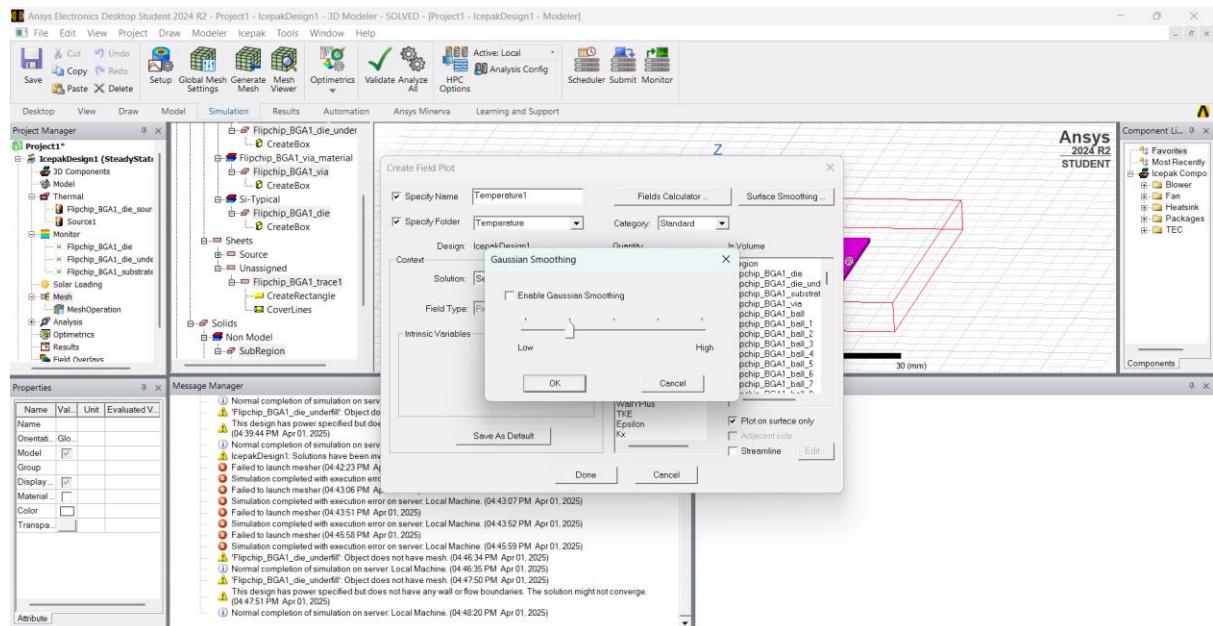
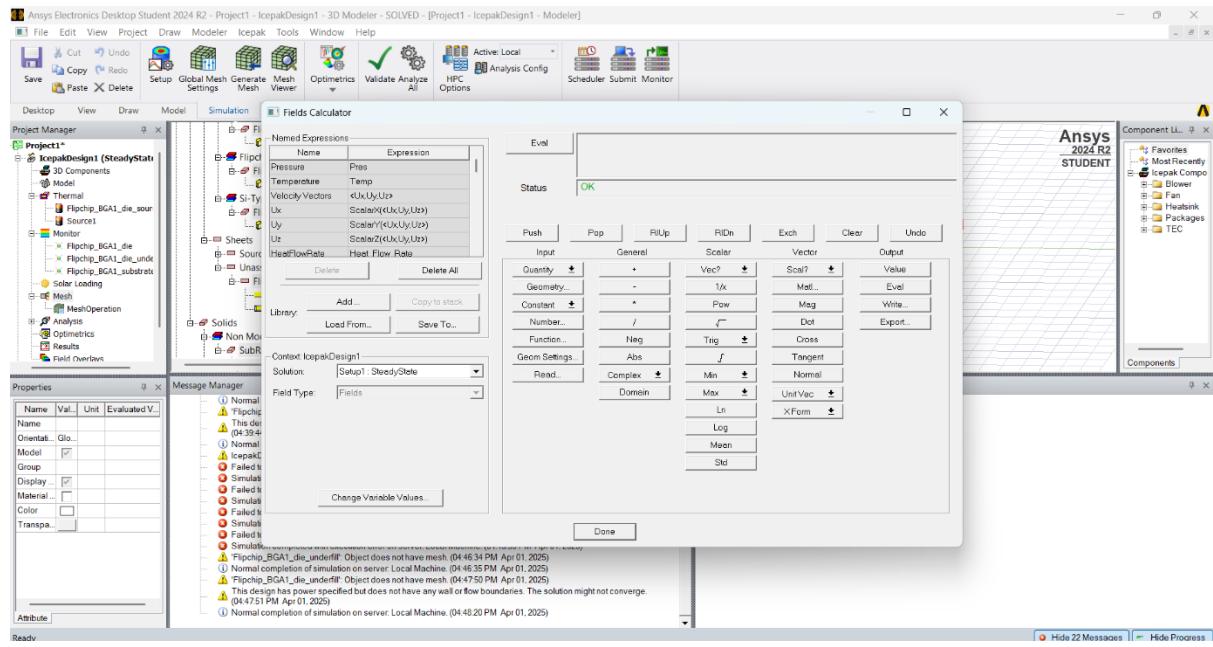
Thermal simulation of Flip-Chip (FC) BGA IC Package



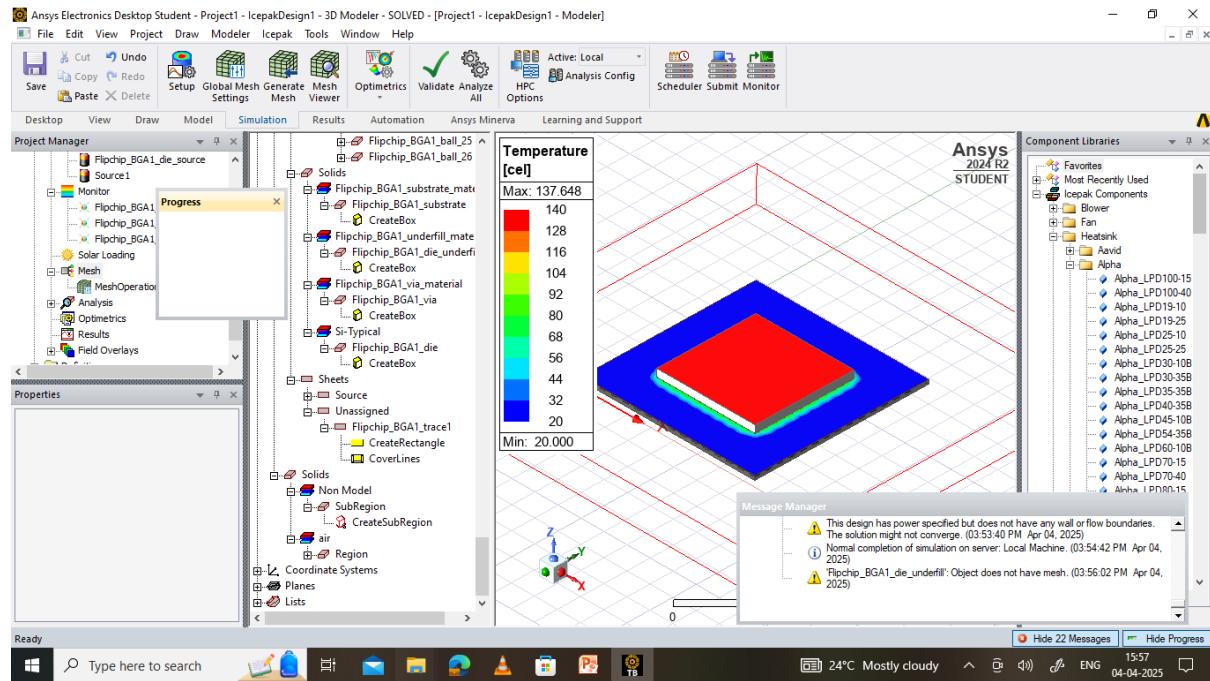








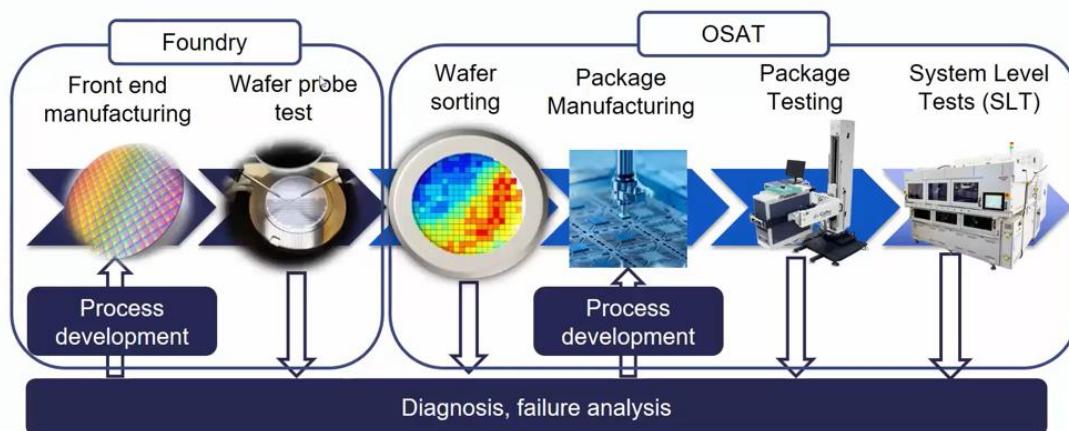
Simulated thermal profile:



Module 4

Key topics

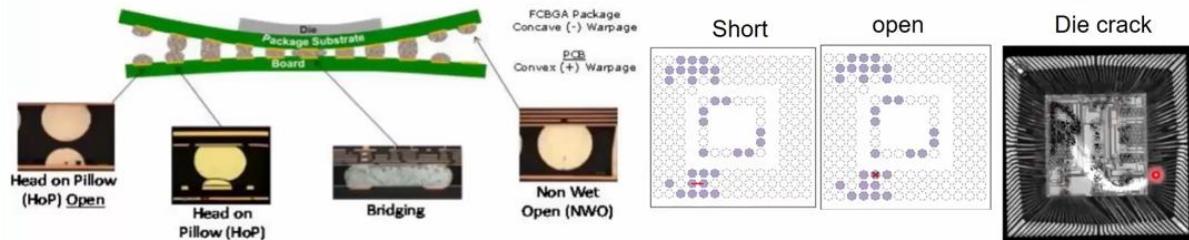
1. Testing process



2. AOST

Objective: Quick test for shorts or opens on package leads or balls.

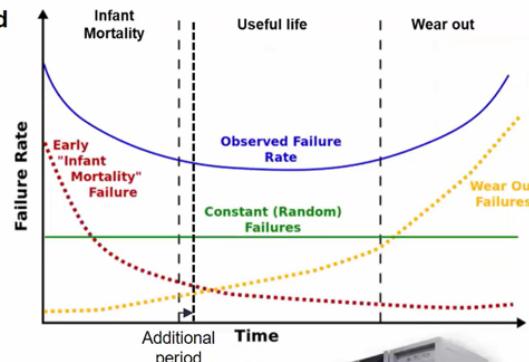
- Testing immediately follows Trim and Form (lead frame packages) or Singulation (BGA packages).
- The packages are put through an open/short test to screen for massive electrical fails before leaving assembly.
- There is also a vision inspection to check for damaged or missing balls/leads and other obvious defects
- Product Grade Sort (PGSRT) catches Assembly related fails, and sorts into Product Grades: Best (1), Better (2), Better (3), Scrap (4).



3. Burn-in Test

Objective: Testing of package components under elevated (stressful) conditions. temperature, voltage, and power cycling

- The goal of Burn-in is to identify "Infant Mortality" failures before it reaches the customer.
- Parts are loaded from trays onto Burn-in boards and then, into ovens (Burn-in system) during testing.
- Burn-in accelerates the failures by applying high voltage and high temperature stress.
- The test is carried out long enough to catch the initial rate of failures and then to test slightly over the point where the curve flattens out.
- Defects like dielectric & metallization failures, electromigration can be detected during burn-in.
- Although it removes the unreliable components with a high probability of early failure, the total life span of components is shortened with a burn-in test.



Burn-in Boards

4. Final test

Objective: A temperature corner test to verify that the packaged product meets the specifications

- Parts are loaded into handler with temperature controlled test fixtures (not ovens) during testing.
- Hot Test: Elevated temperatures according to product specifications. Parts are electrically tested at high temperatures to verify if the specifications are met.
- Cold Test: Parts are subjected to low temperatures according to product specifications and electrically tested.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾⁽³⁾

		MIN	MAX	UNIT
Supply voltage	LM741, LM741A LM741C	±22 ±18		V
Power dissipation ⁽⁴⁾		500	mW	
Differential input voltage		±30	V	
Input voltage ⁽⁵⁾		±15	V	
Output short circuit duration		Continuous		
Operating temperature	LM741, LM741A LM741C	-50 0	125 70	°C
Junction temperature	LM741, LM741A LM741C		150 100	°C
Soldering information	PDIP package (10 seconds) CQFP or TO-99 package (10 seconds)	260 300	°C	
Storage temperature, T _{stg}		-65	150	°C

LM741 OPamp (T1) Datasheet

ATE (Electrical Testing Unit) with Handler (Placing DUT)



[video](#)

6.5 Electrical Characteristics, LM741⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input offset voltage	R ₀ ≤ 10 kΩ T _A = 25°C T _{AMIN} ≤ T _A ≤ T _{AMAX}	1 6	5 mV		mV
Input offset voltage adjustment range	T _A = 25°C, V _B = ±20 V		±15		mV
Input offset current	T _A = 25°C T _{AMIN} ≤ T _A ≤ T _{AMAX}	20	200	200	nA
Input bias current	T _A = 25°C T _{AMIN} ≤ T _A ≤ T _{AMAX}	85	500	500	nA
Input resistance	T _A = 25°C, V _B = ±20 V	80	500	500	nA
Input voltage range	T _{AMIN} ≤ T _A ≤ T _{AMAX}	0.3	2	1.5	µA
Large signal voltage gain	V _B = ±15 V, V _O = ±10 V, R _L ≥ 2 kΩ T _A = 25°C T _{AMIN} ≤ T _A ≤ T _{AMAX}	50	200	25	Vi/mV
Output voltage swing	V _B = ±15 V R _L ≥ 10 kΩ	±12	±14	±10	V
	R _L ≥ 2 kΩ	±10	±13		

5. ATE

Automatic Test Equipment (ATE)

- Test equipment's that send automatic test pattern generation (ATPG) to the device under test (DUT).
- Major test categories:
 - ✓ Parametric Tests: measures current (or voltage) from the unit to ensure the circuits are functioning within specified parameters.
 - ✓ Functional Tests: evaluate functionality of the unit under operating conditions.
 - ✓ Speed Tests: assesses speed of units according to data sheet specifications. Sorting is done based on speed.
- Yield, Testing Time and Test coverage are key performance indicator during testing.

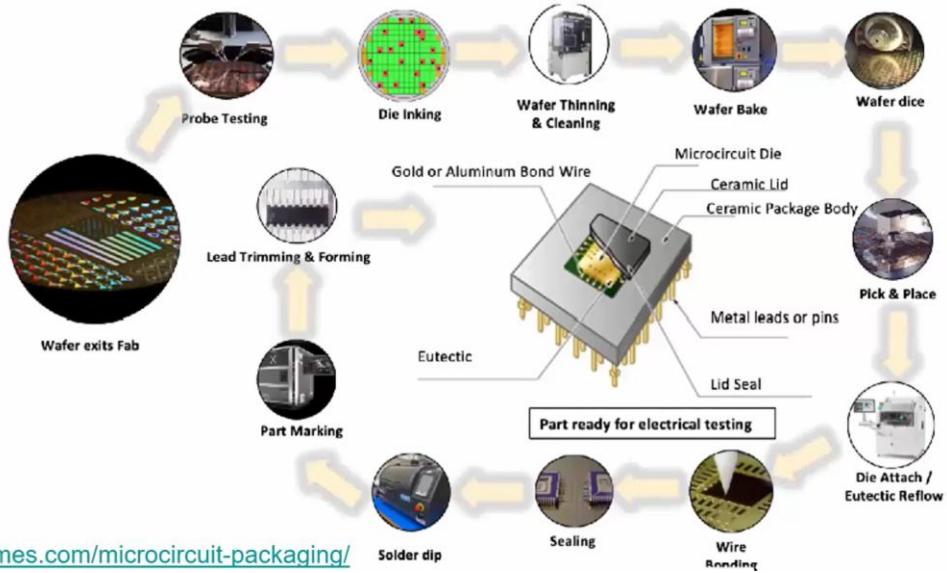
[Video: ATE at different stages](#)



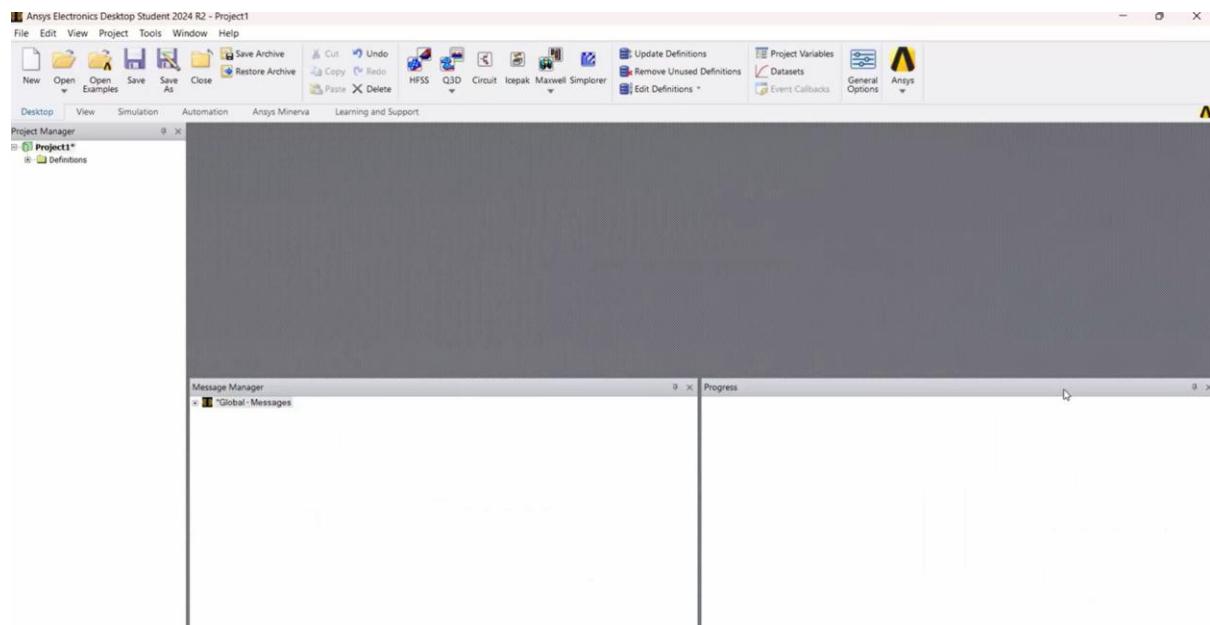
Module 5 (Lab)

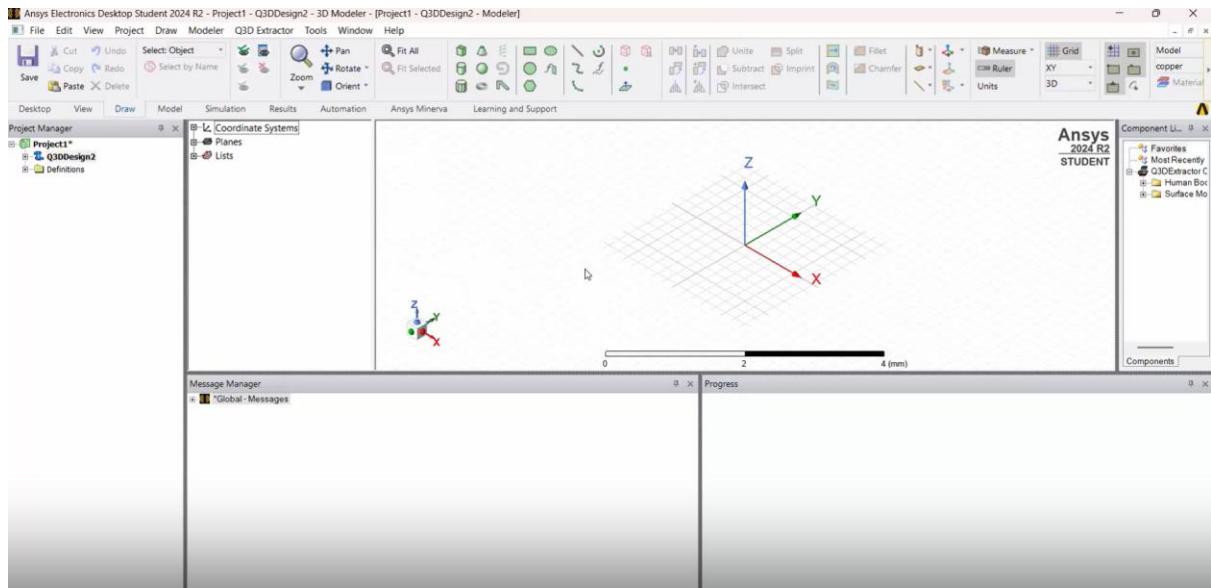
Key topics

Objective: Create a virtual model of the package cross-section till molding/sealing stage

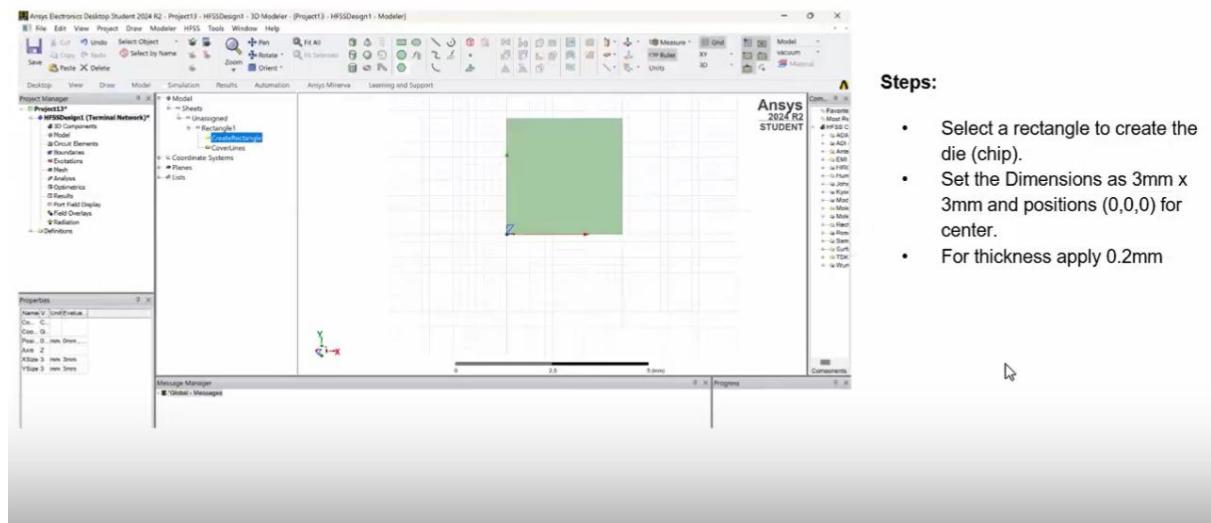


Source: <https://gemes.com/microcircuit-packaging/>



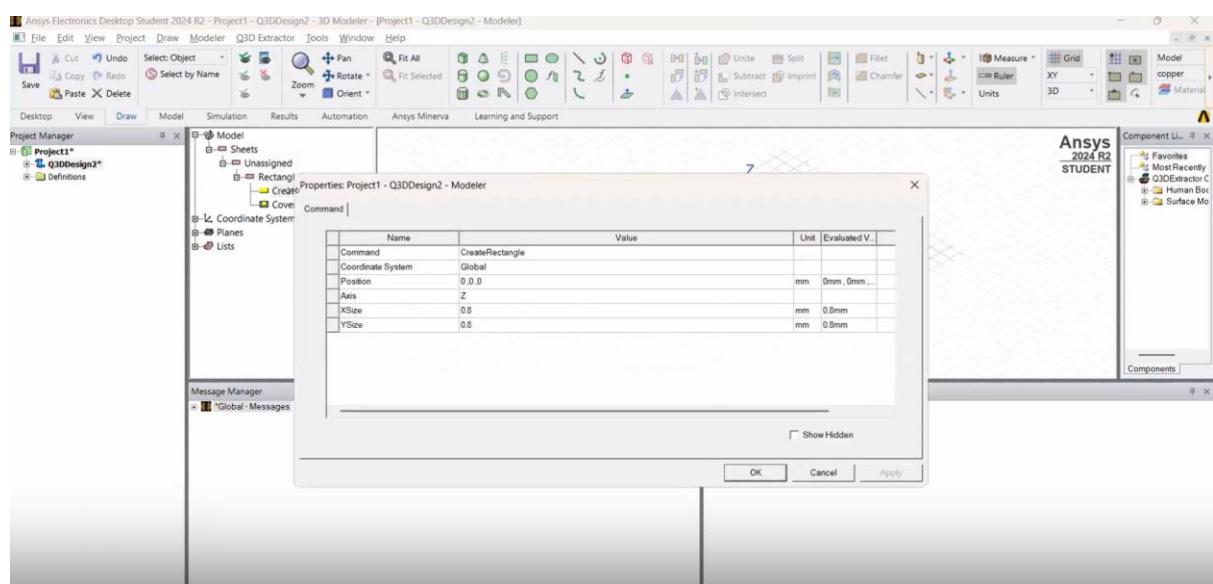
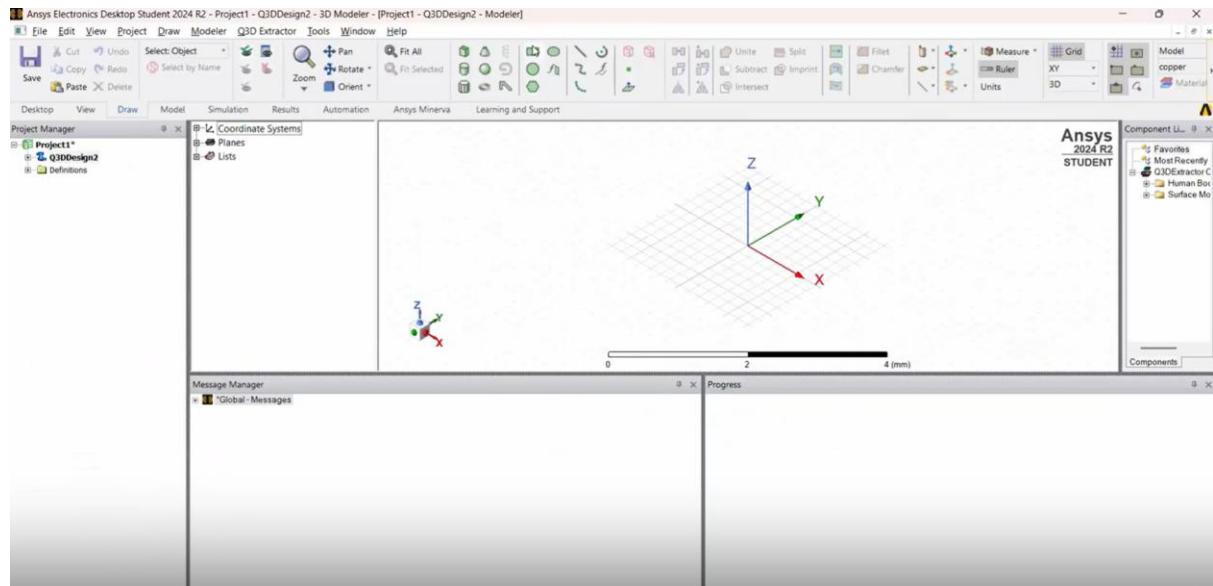


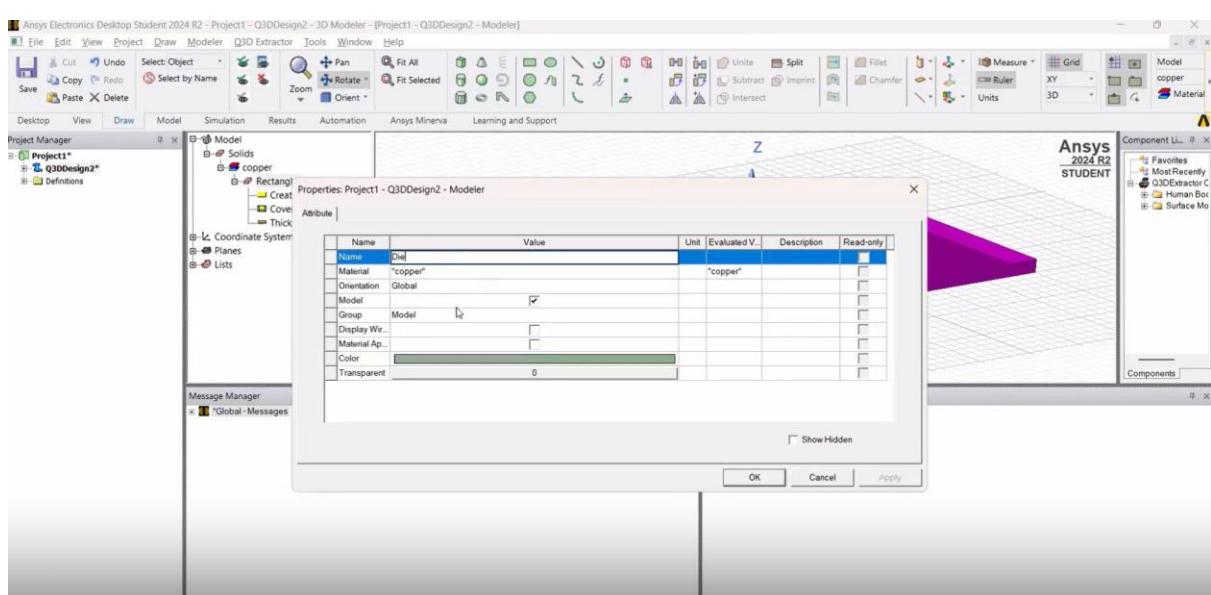
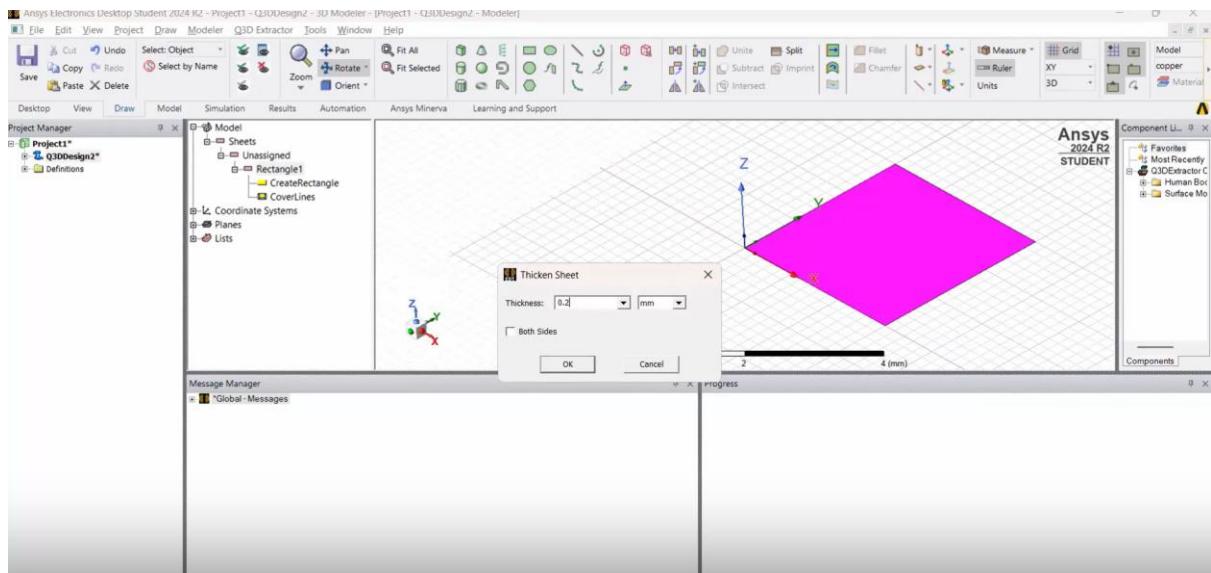
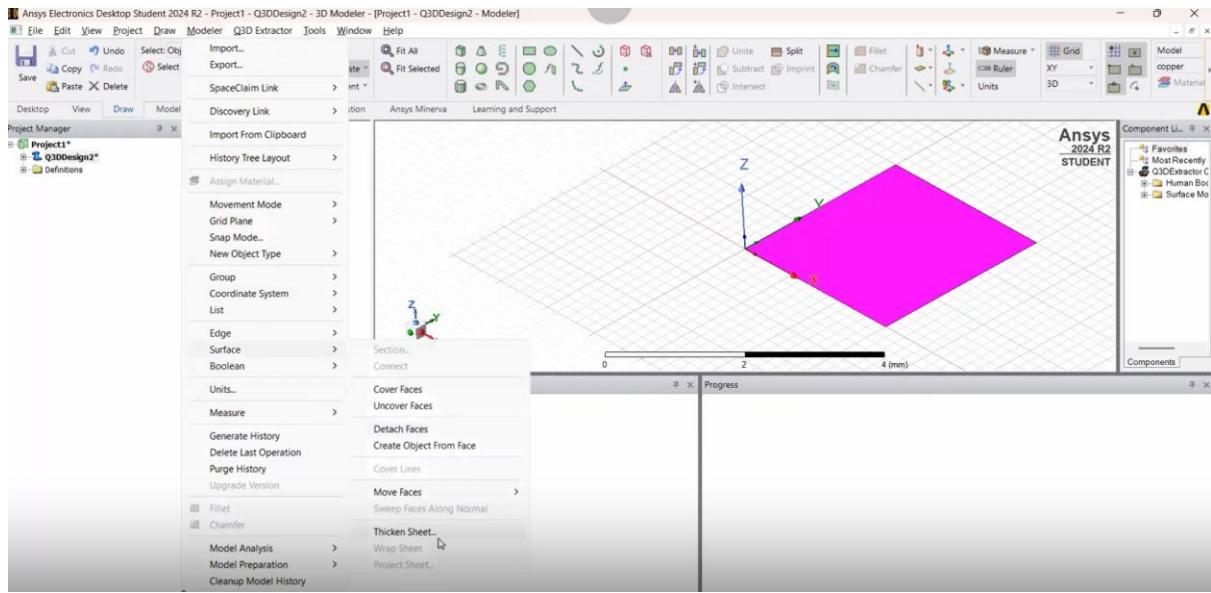
Step 2: Create the die

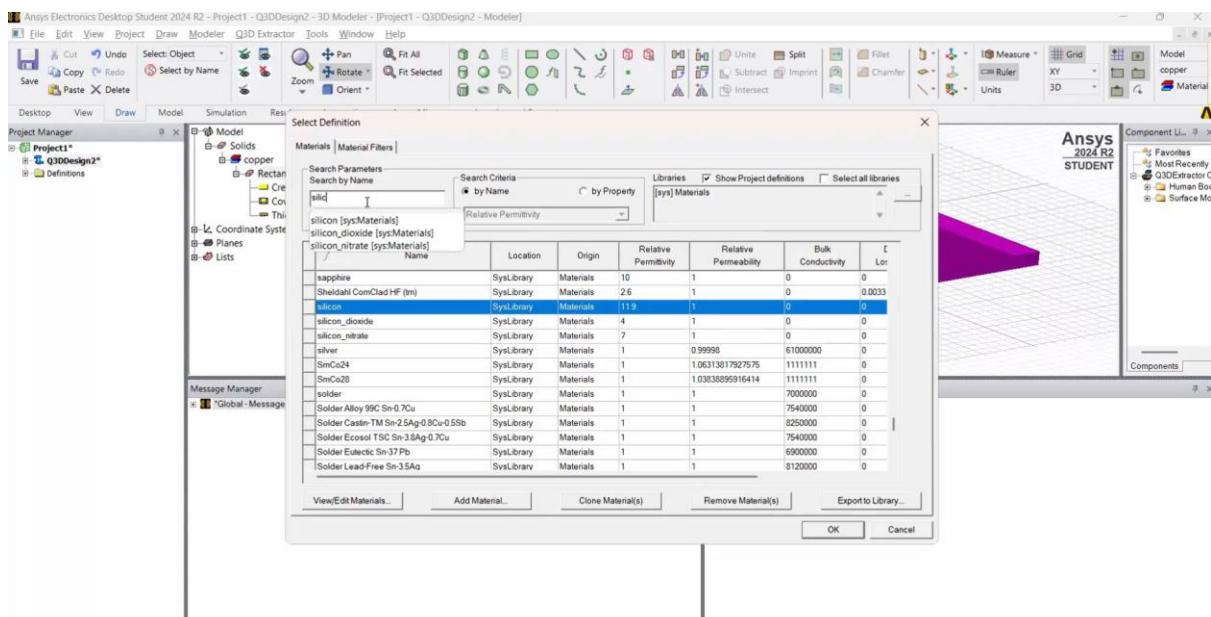
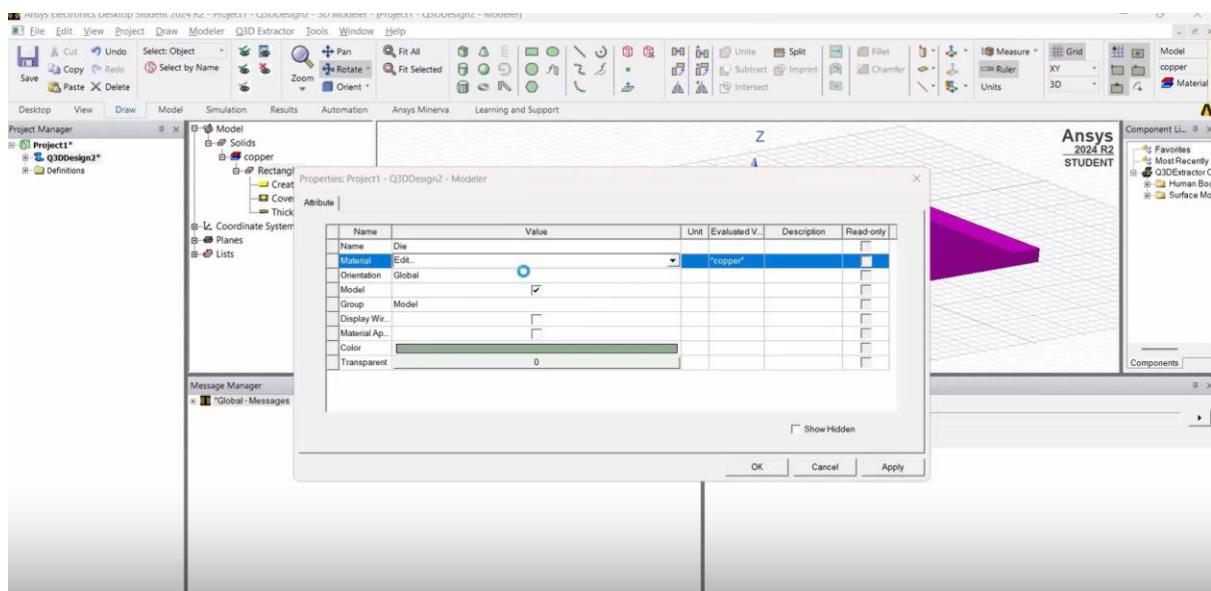


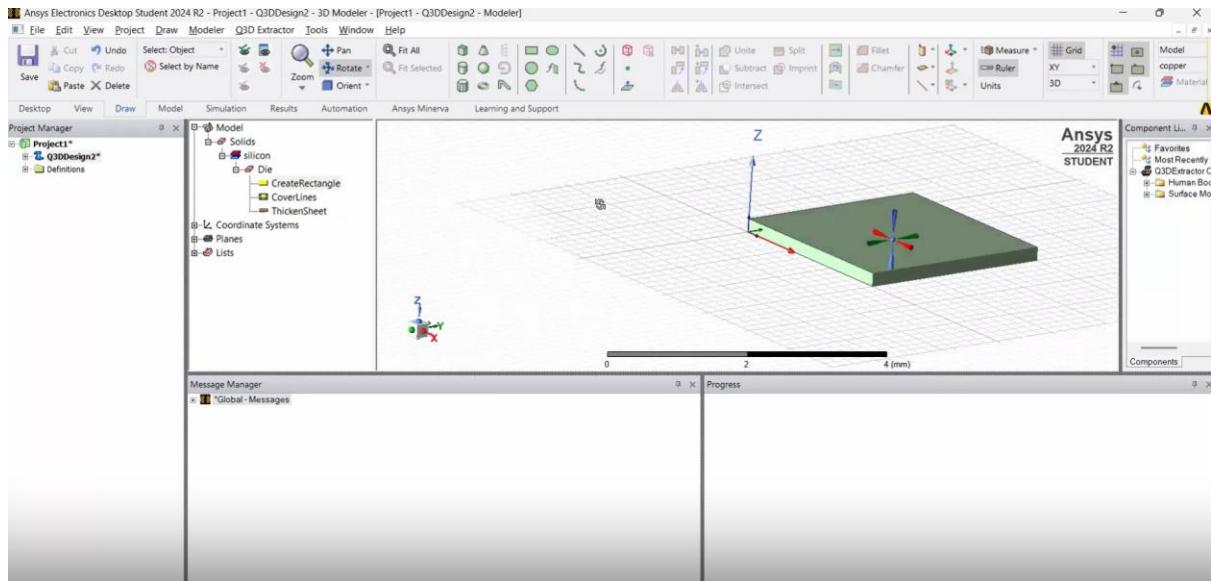
Steps:

- Select a rectangle to create the die (chip).
- Set the Dimensions as 3mm x 3mm and positions (0,0,0) for center.
- For thickness apply 0.2mm

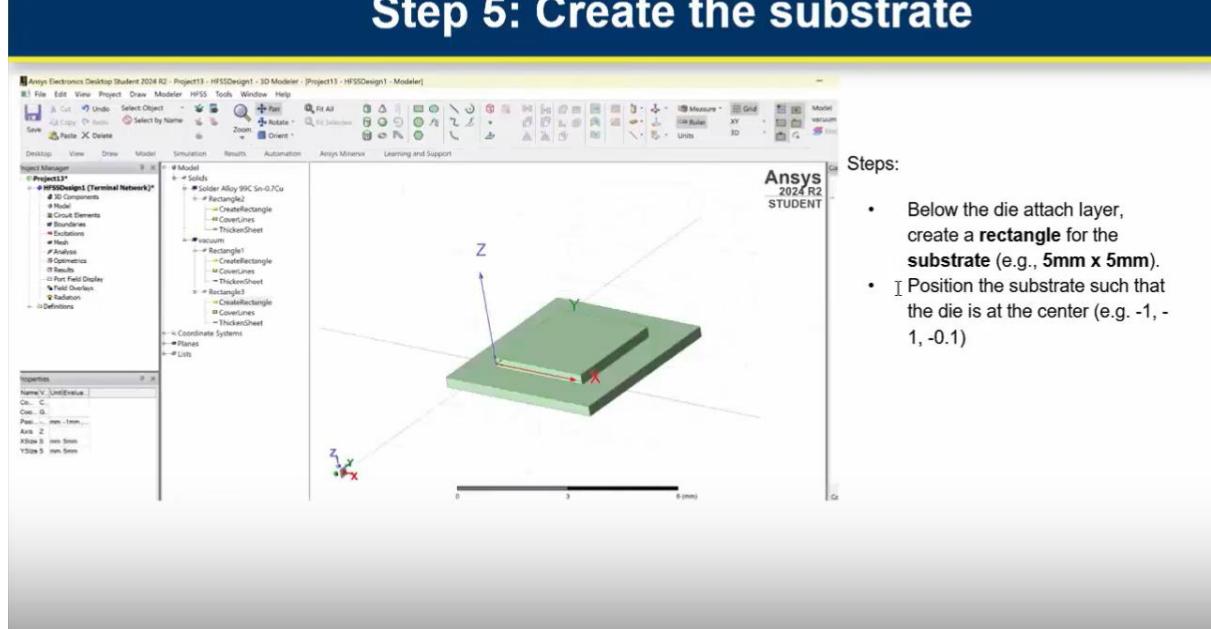


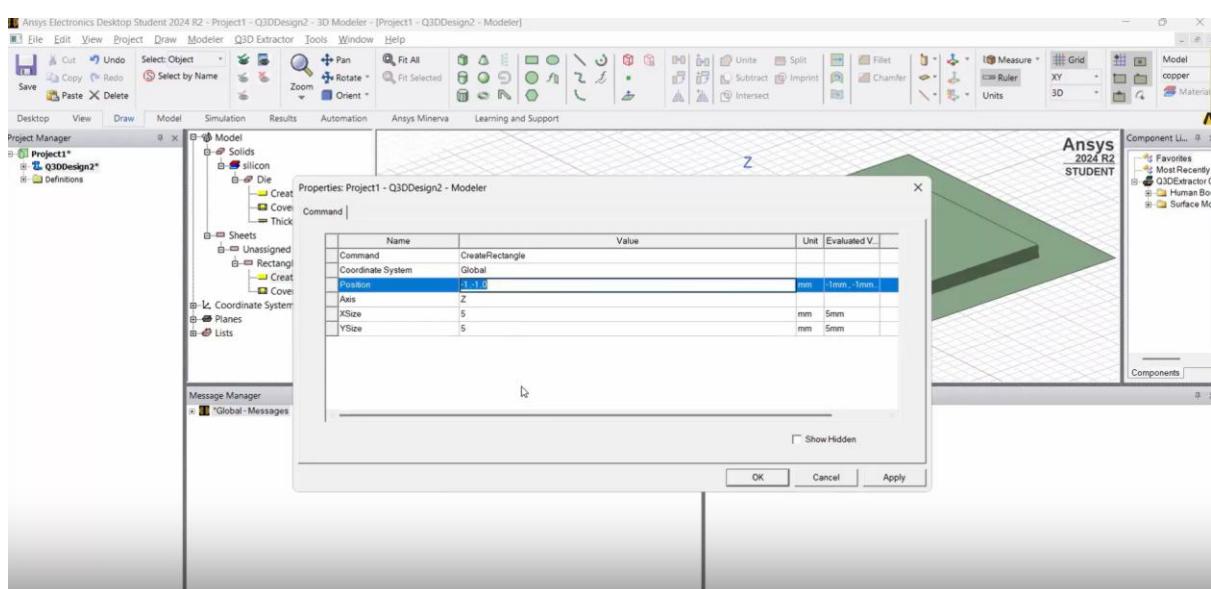
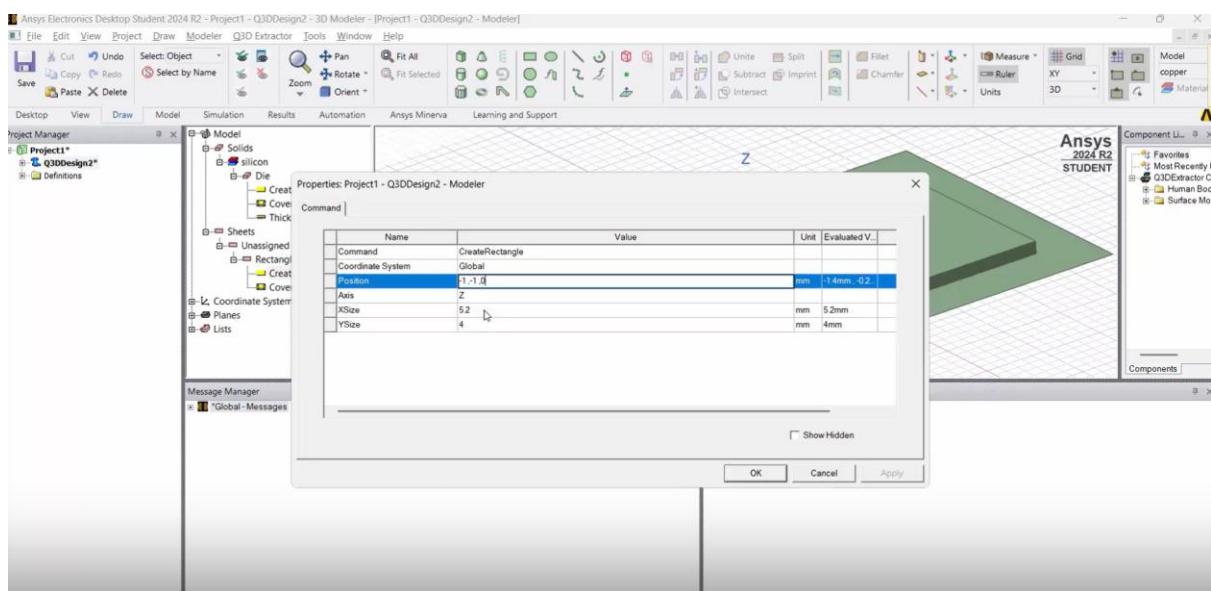
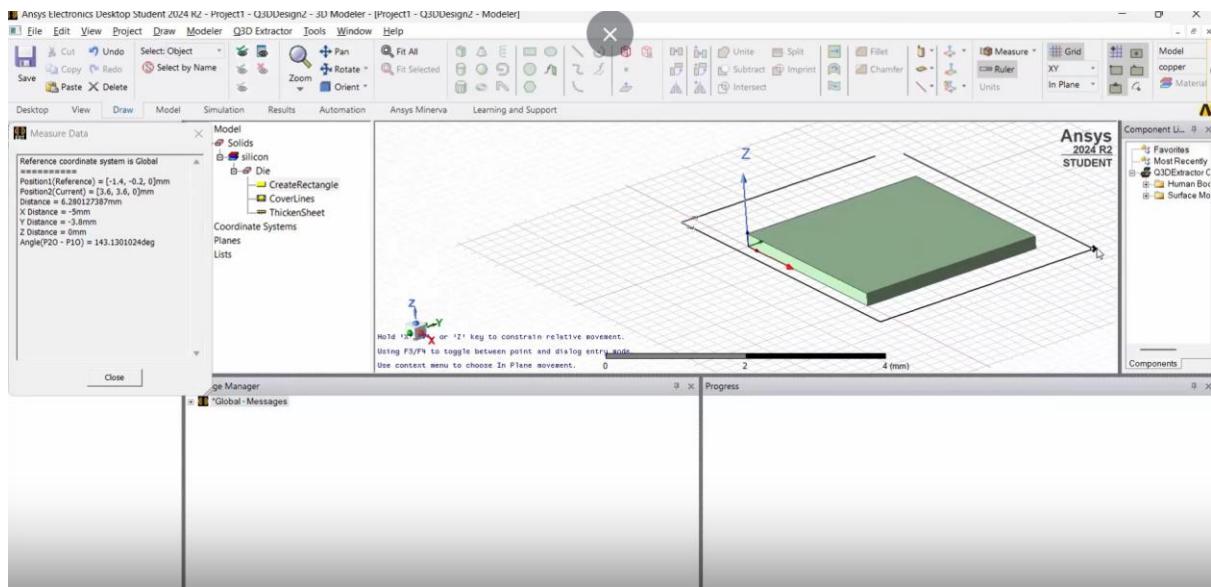


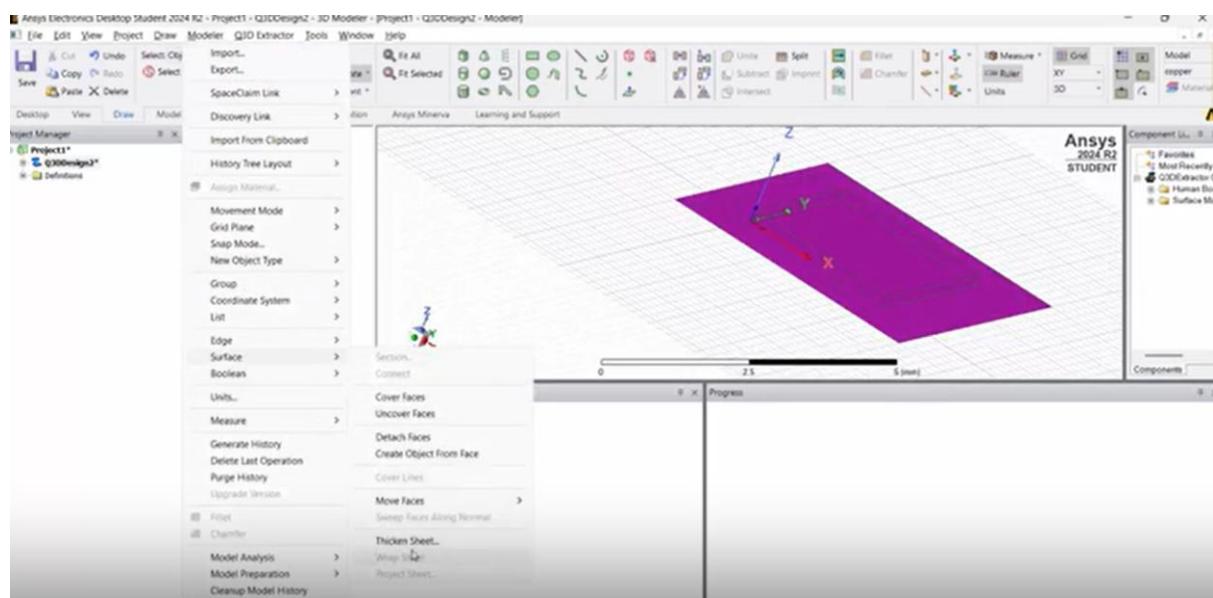
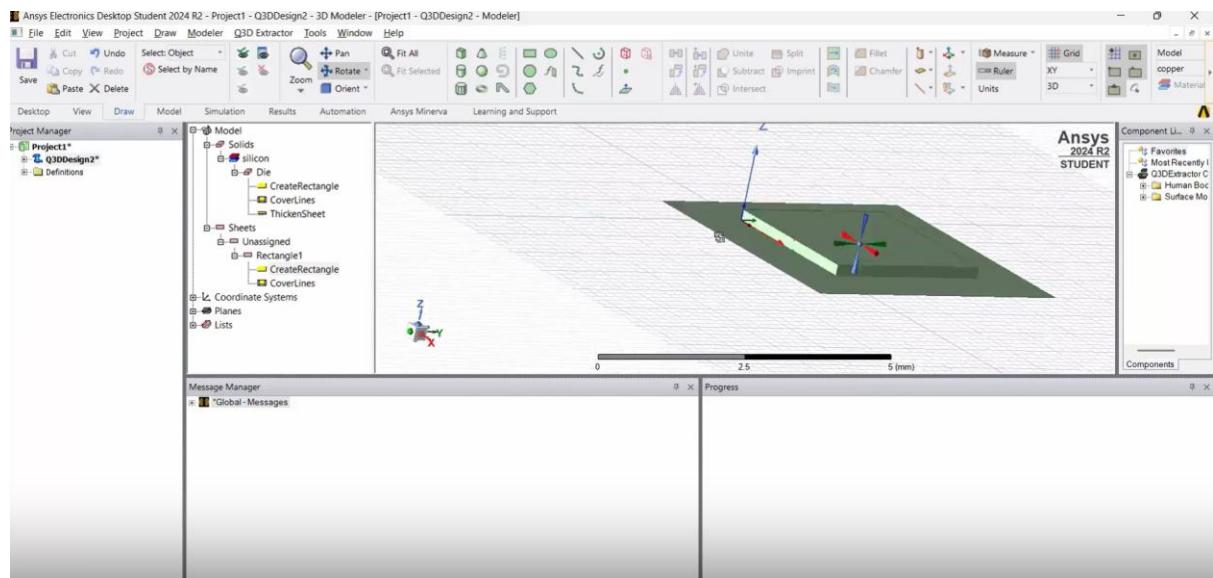


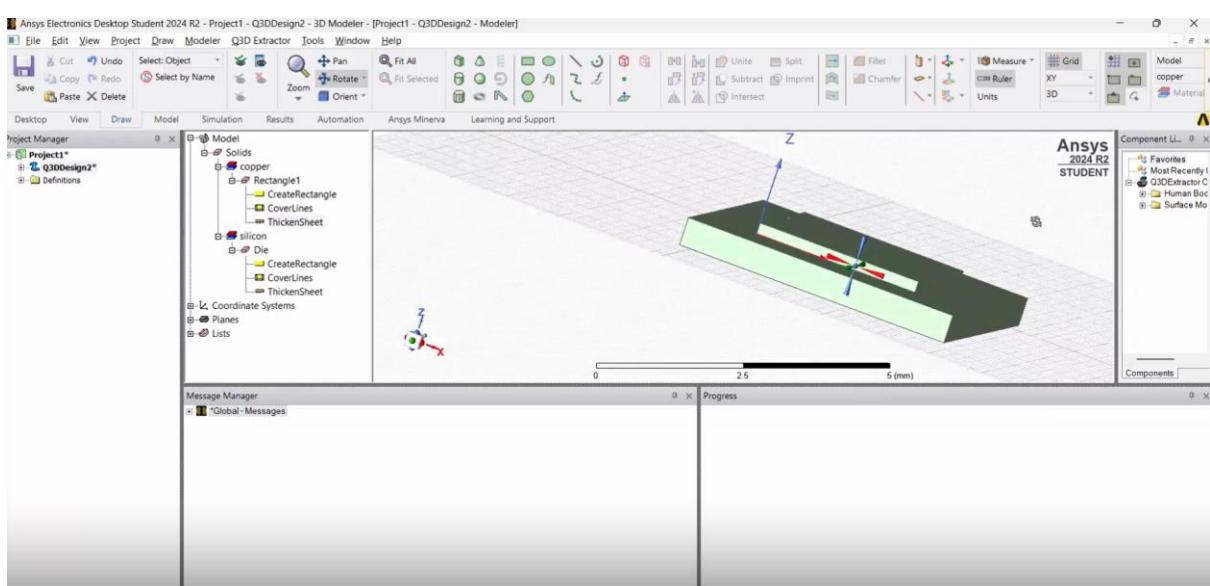
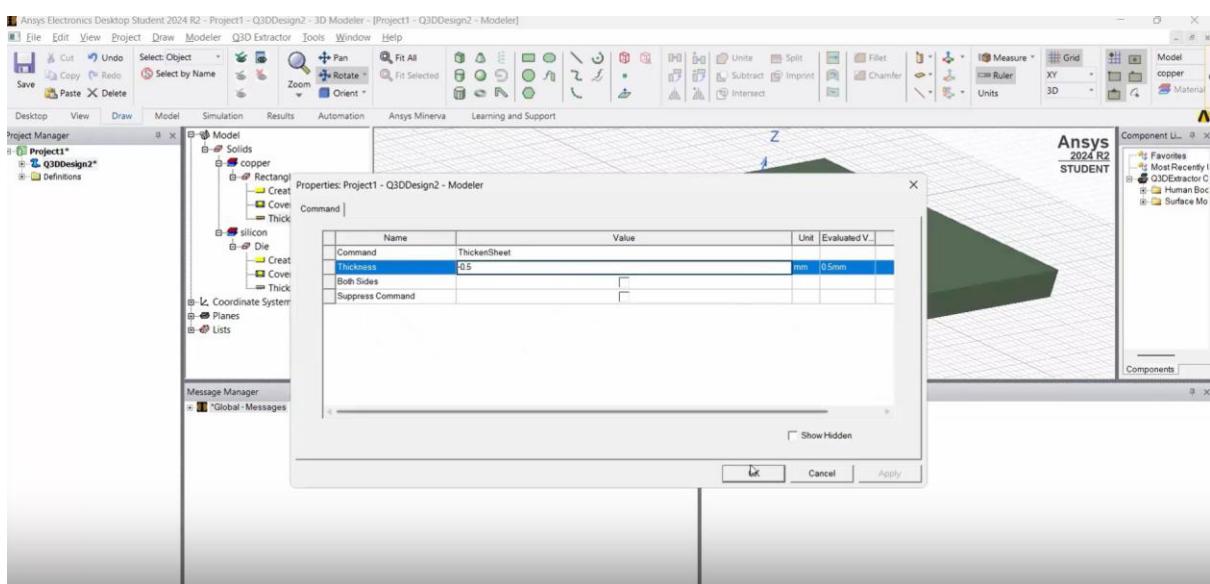
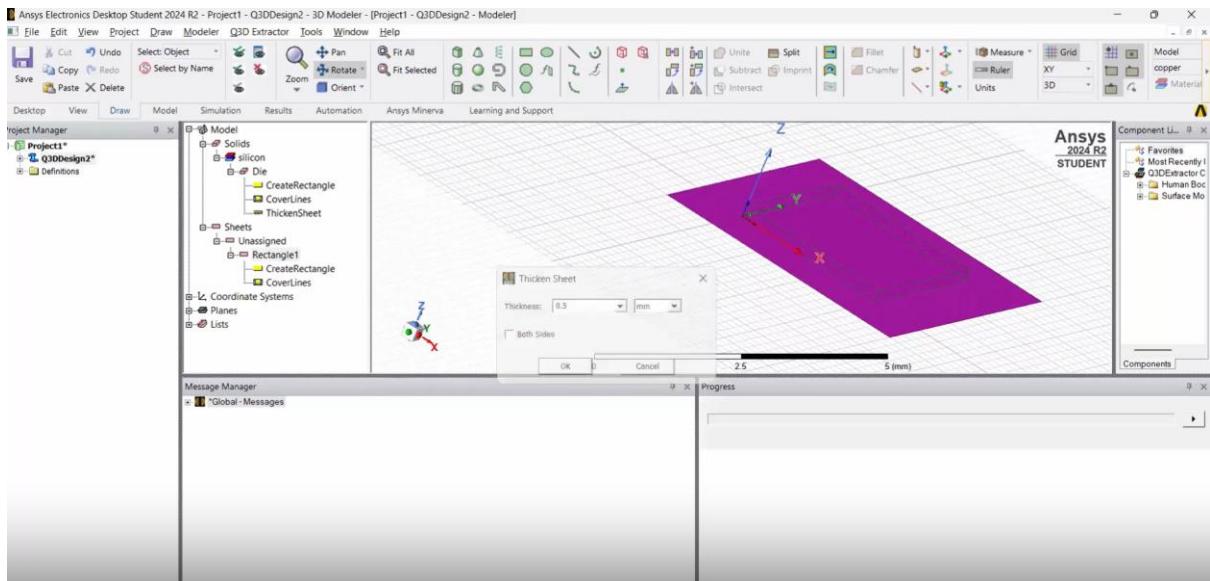


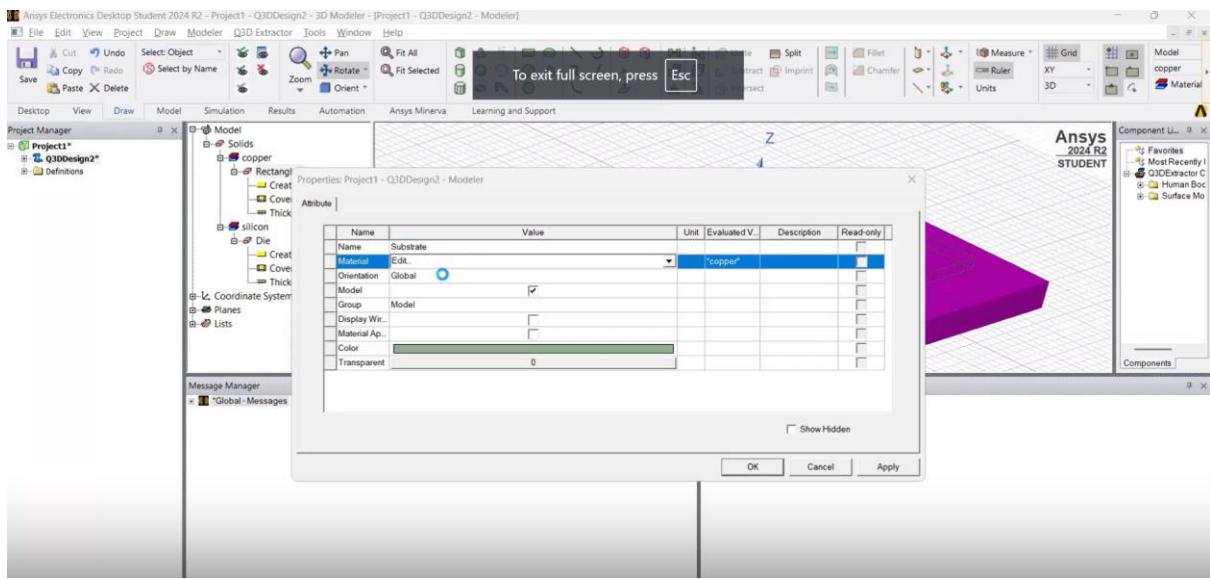
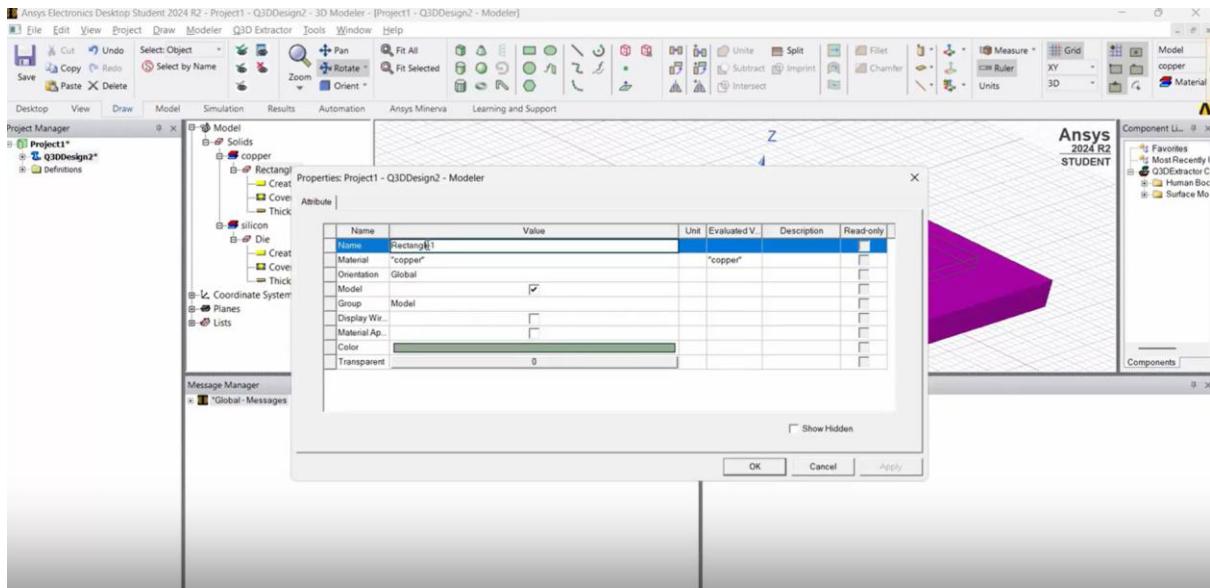
Step 5: Create the substrate

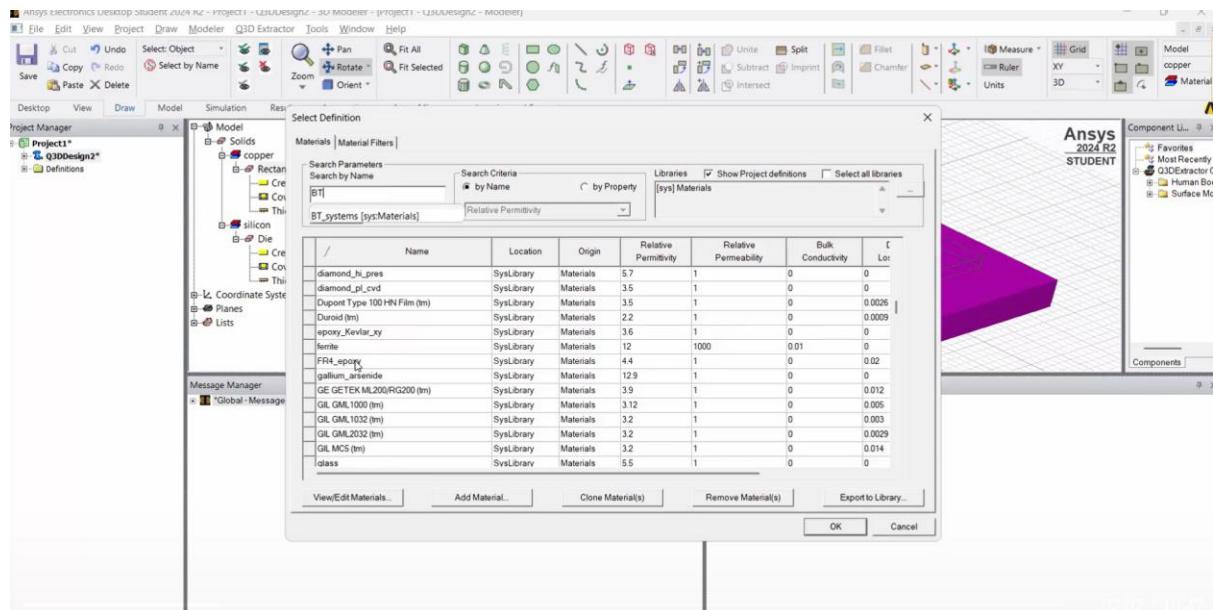
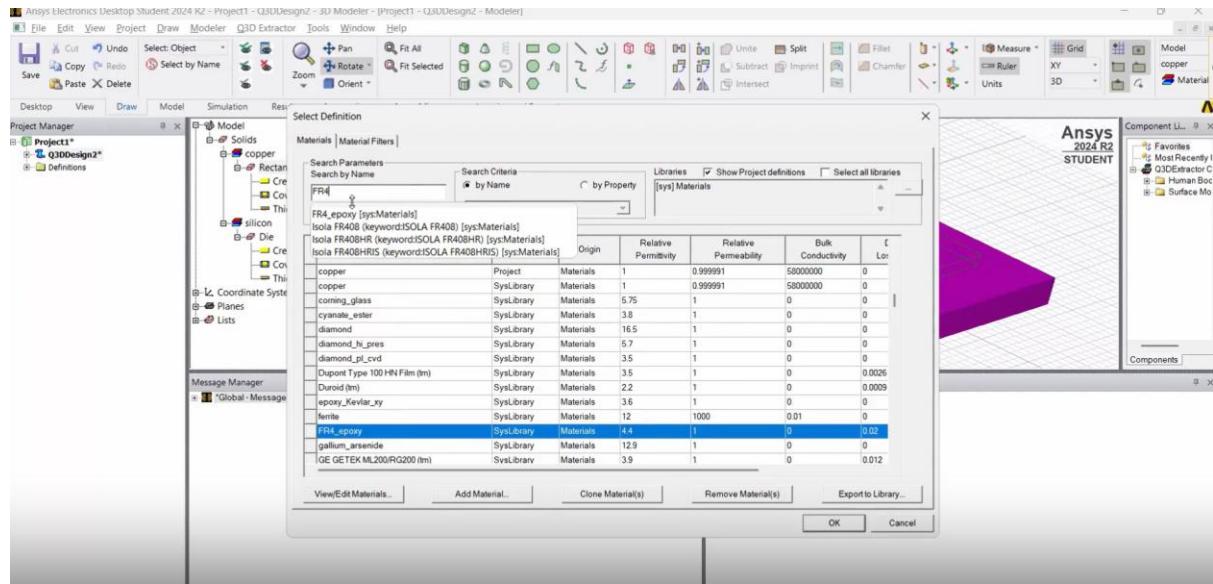


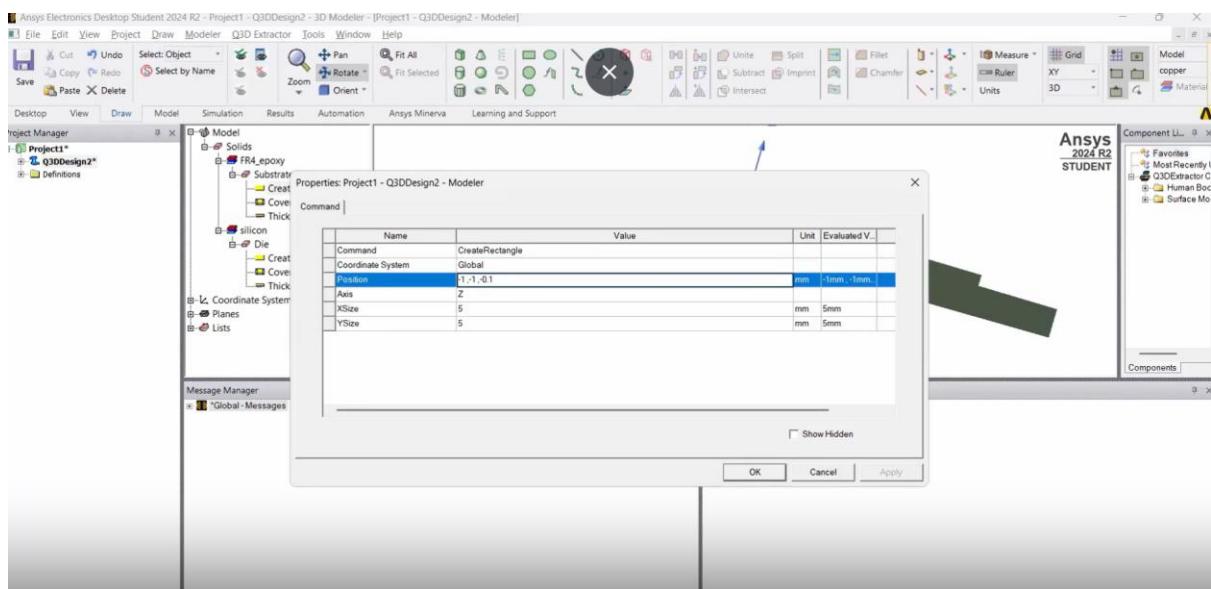
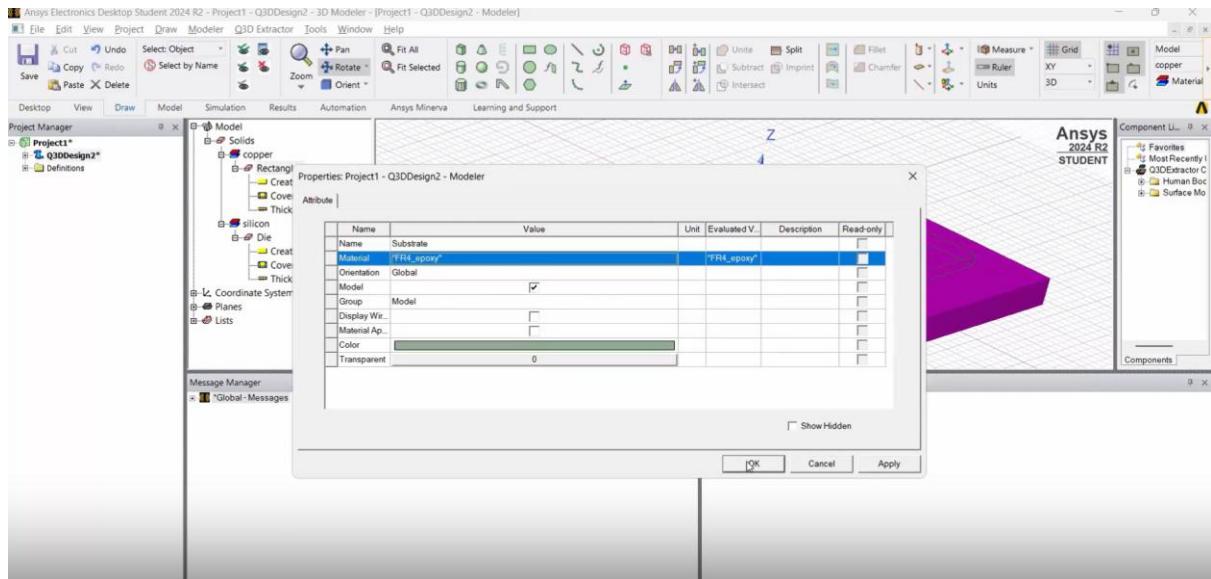




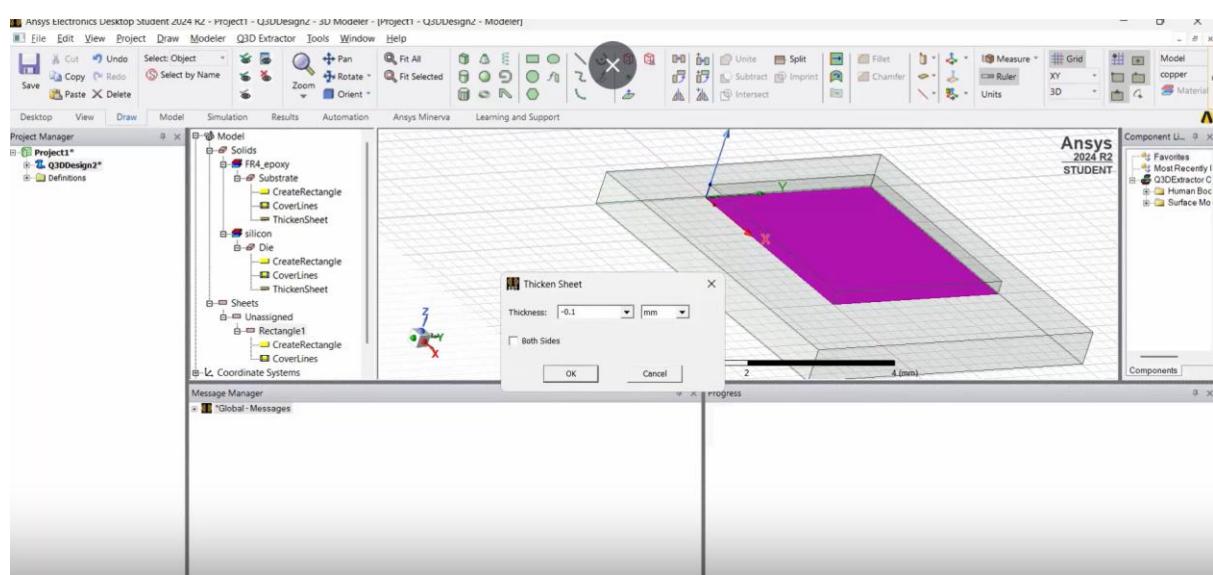
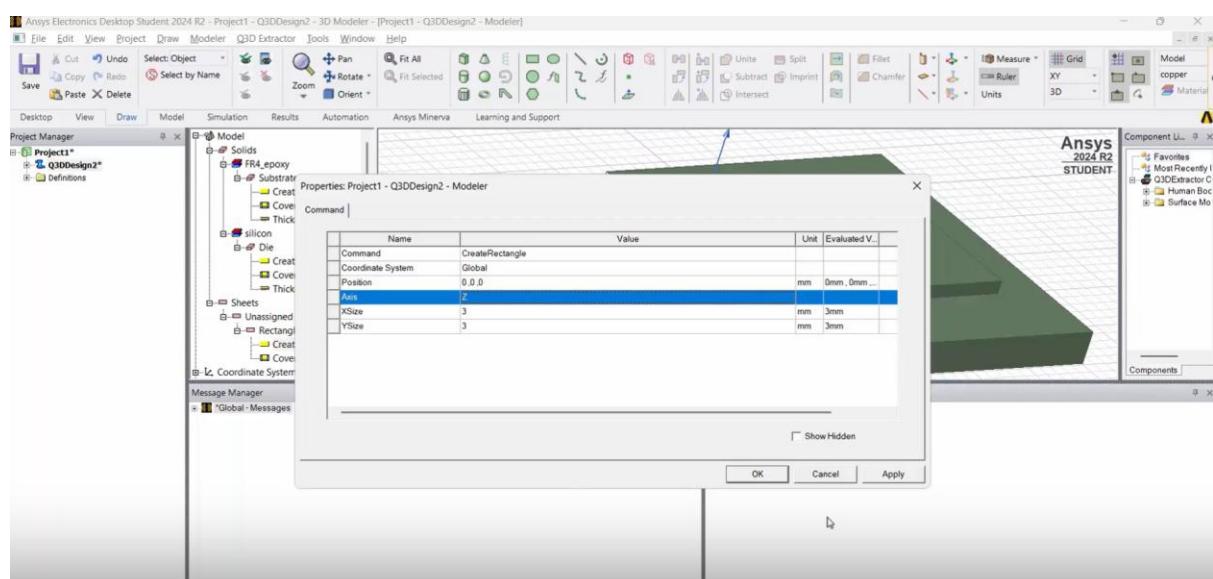
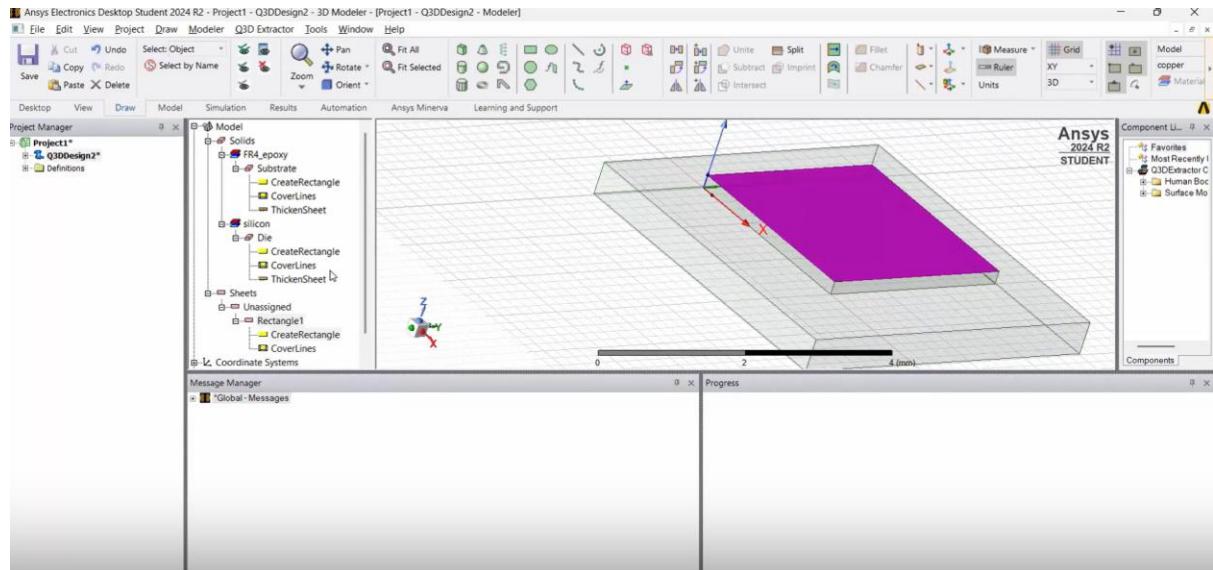


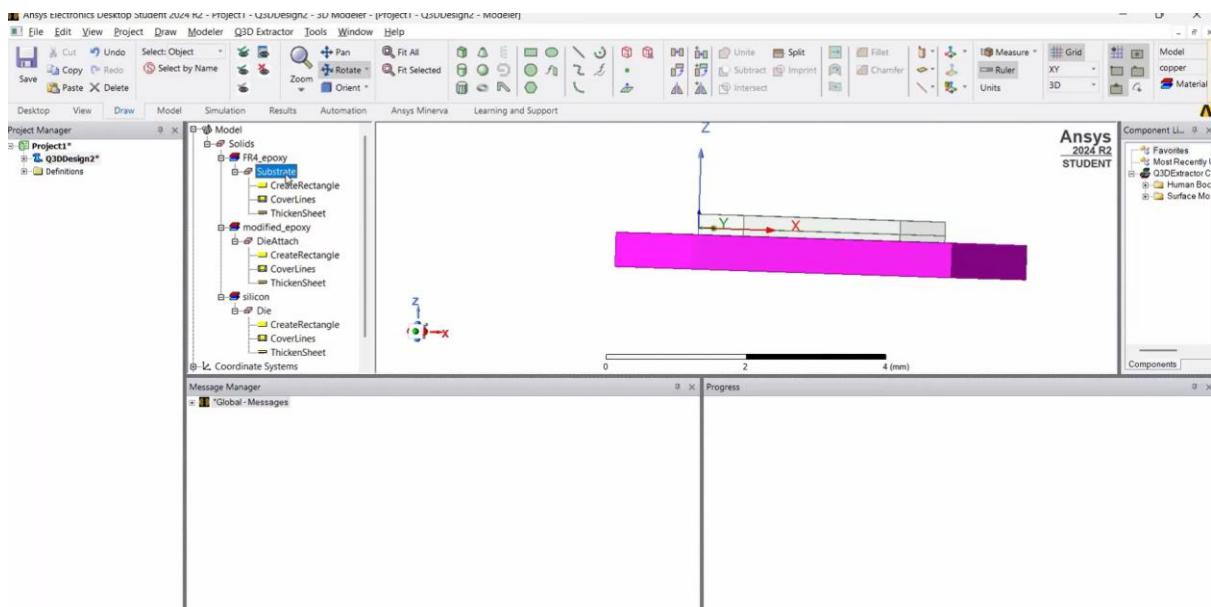
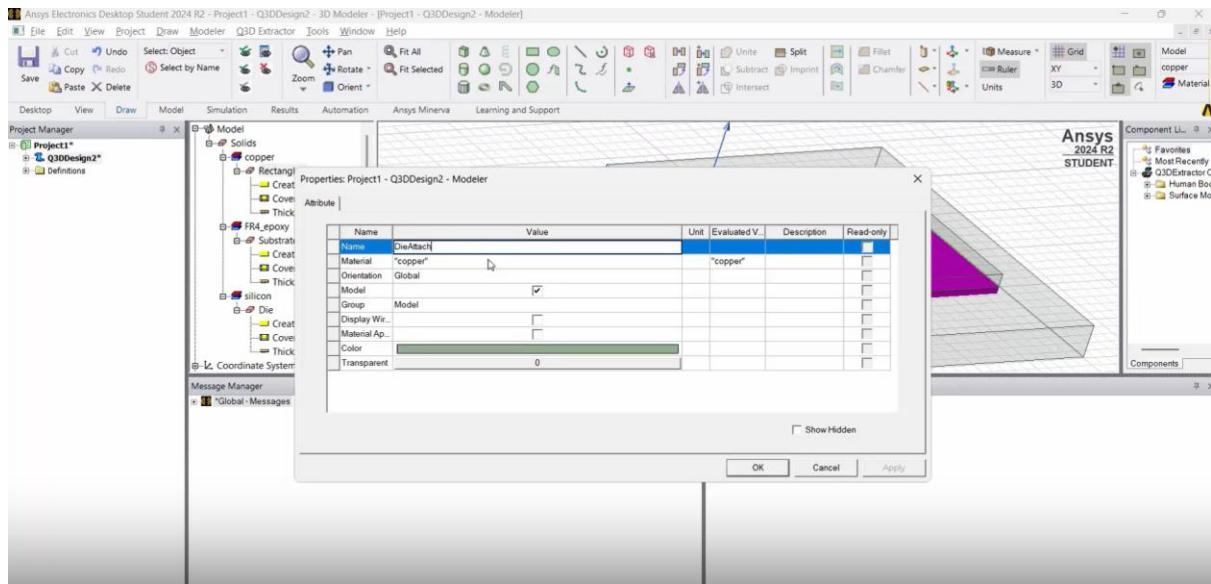






Die attach





Wire bonding

