UM1974
User manual

STM32 Nucleo-144 boards (MB1137)

Introduction

The STM32 Nucleo-144 boards based on the MB1137 reference board (NUCLEO-F207ZG, NUCLEO-F303ZE, NUCLEO-F412ZG, NUCLEO-F413ZH, NUCLEO-F429ZI, NUCLEO-F439ZI, NUCLEO-F446ZE, NUCLEO-F722ZE, NUCLEO-F746ZG, NUCLEO-F756ZG, NUCLEO-F767ZI, and NUCLEO-H743ZI) provide an affordable and flexible way for users to try out new concepts and build prototypes with STM32 microcontrollers, choosing from the various combinations of performance, power consumption and features. The ST Zio connector, which extends the ARDUINO® Uno V3 connectivity, and the ST morpho headers make it easy to expand the functionality of the Nucleo open development platform with a wide choice of specialized shields. The STM32 Nucleo-144 boards do not require any separate probe as they integrate the ST-LINK/V2-1 debugger/programmer. The STM32 Nucleo-144 boards come with the comprehensive free software libraries and examples available with the STM32Cube MCU Package.

Figure 1. Nucleo-144 board (top view)

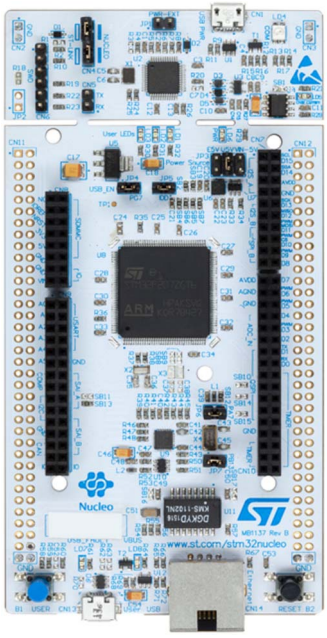
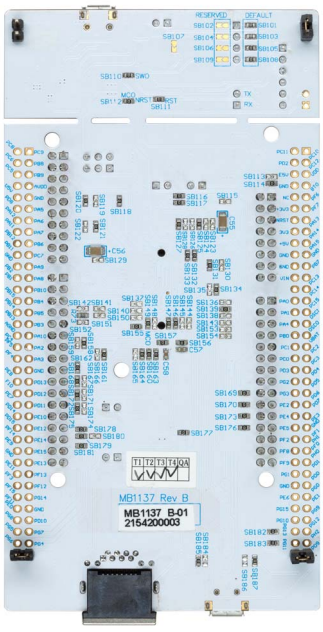


Figure 2. Nucleo-144 board (bottom view)



Pictures are not contractual.

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1 Features

The STM32 Nucleo-144 boards offer the following features:

- Common features
  - STM32 Arm®(a) Cortex® core-based microcontroller in an LQFP144 package
  - 3 user LEDs
  - 2 user and reset push-buttons
  - 32.768 kHz crystal oscillator
  - Board connectors:
    - USB with Micro-AB
    - SWD
    - ST Zio expansion connector including ARDUINO® Uno V3
    - ST morpho expansion connector
  - Flexible power-supply options: ST-LINK USB V_{BUS} or external sources
  - On-board ST-LINK/V2-1 debugger/programmer with USB re-enumeration capability: mass storage, Virtual COM port and debug port
  - Comprehensive free software libraries and examples available with the STM32Cube MCU Package
  - Supported by a wide choice of Integrated Development Environments (IDEs) including IAR Embedded Workbench®, MDK-ARM, STM32CubeIDE
- Board-specific features
  - Ethernet compliant with IEEE-802.3-2002
  - USB OTG or full-speed device
  - Board connectors:
    - Ethernet RJ45

arm

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Ordering information

To order the STM32 Nucleo-144 board, refer to *Table 1*. Additional information is available from the datasheet and reference manual of the target microcontroller.

Table 1. Ordering information

Order code	Board reference	Target STM32	Differentiating features
NUCLEO-F207ZG	MB1137(1)	STM32F207ZGT6	– Ethernet – USB OTG FS on Micro-AB connector
NUCLEO-F303ZE		STM32F303ZET6	– Ethernet – Device-only USB on Micro-AB connector
NUCLEO-F412ZG		STM32F412ZGT6	– USB OTG FS on Micro-AB connector
NUCLEO-F413ZH		STM32F413ZHT6	– USB OTG FS on Micro-AB connector
NUCLEO-F429ZI		STM32F429ZIT6	– Ethernet – USB OTG FS on Micro-AB connector
NUCLEO-F439ZI		STM32F439ZIT6	– Ethernet – USB OTG FS on Micro-AB connector – Cryptography
NUCLEO-F446ZE		STM32F446ZET6	– USB OTG FS on Micro-AB connector
NUCLEO-F722ZE		STM32F722ZET6	– USB OTG FS on Micro-AB connector
NUCLEO-F746ZG		STM32F746ZGT6	– Ethernet – USB OTG FS on Micro-AB connector
NUCLEO-F756ZG		STM32F756ZGT6	– Ethernet – USB OTG FS on Micro-AB connector – Cryptography
NUCLEO-F767ZI		STM32F767ZIT6	– Ethernet – On-board USB OTG – USB OTG FS on Micro-AB connector
NUCLEO-H743ZI(2)		STM32H743ZIT6	– Ethernet – USB OTG FS on Micro-AB connector

1. Subsequently named main board in the rest of the document.
2. Replaced with NUCLEO-H743ZI2.

2.1 Codification

The meaning of the codification is explained in *Table 2*.

Table 2. Codification explanation

NUCLEO-TXXXZY	Description	Example: NUCLEO-F446ZE
TXXX	MCU product line in STM32 32-bit Arm Cortex MCUs	STM32F446
Z	STM32 package pin count – Z for 144 pins	144 pins
Y	STM32 flash memory size – E for 512 Kbytes – G for 1 Mbyte – H for 1.5 Mbytes – I for 2 Mbytes	512 Kbytes

3 Development environment

3.1 System requirements

- Multi-OS support: Windows®(a) 10, Linux®(b) 64-bit, or macOS® (c)
- USB Type-A or USB Type-C® to Micro-B cable

3.2 Development toolchains

- IAR Systems® - IAR Embedded Workbench®(d)
- Keil® - MDK-ARM(d)
- STMicroelectronics - STM32CubeIDE

3.3 Demonstration software

The demonstration software, included in the STM32Cube MCU Package corresponding to the on-board microcontroller, is preloaded in the STM32 flash memory for easy demonstration of the device peripherals in standalone mode. The latest versions of the demonstration source code and associated documentation can be downloaded from *www.st.com*.

4 Conventions

Table 3 provides the conventions used for the ON and OFF settings in the present document.

Table 3. ON/OFF conventions

Convention	Definition
Jumper JPx ON	Jumper fitted
Jumper JPx OFF	Jumper not fitted
Solder bridge SBx ON	SBx connections closed by solder or 0 ohm resistor
Solder bridge SBx OFF	SBx connections left open

In this document the references for all information that is common to all sale types, are “STM32 Nucleo-144 board” and “STM32 Nucleo-144 boards”.

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b. Linux® is a registered trademark of Linus Torvalds.

c. macOS® is a trademark of Apple Inc. registered in the U.S. and other countries and regions.

d. On Windows® only.

5 Quick start

The STM32 Nucleo-144 board is a low-cost and easy-to-use development kit, used to evaluate and start a development quickly with an STM32 microcontroller in LQFP144 package.

Before installing and using the product, accept the Evaluation Product License Agreement from the www.st.com/epla webpage. For more information on the STM32 Nucleo-144 and for demonstration software, visit the www.st.com/stm32nucleo webpage.

5.1 Getting started

Follow the sequence below to configure the Nucleo-144 board and launch the demonstration application (for components location refer to *Figure 4: Top layout*):

1. Check jumper position on the board:

   JP1 OFF (PWR-EXT) selected (see *Section 6.4.1: Power supply input from ST-LINK/V2-1 USB connector* for more details)

   JP3 on U5V (Power source) selected (for more details see *Table 7: External power sources*)

   JP5 ON (IDD) selected (for more details see *Section 6.7: JP5 (I_{DD})*)

   CN4 ON selected (for more details see *Table 4: CN4 states of the jumpers*)
2. For the correct identification of the device interfaces from the host PC and before connecting the board, install the Nucleo USB driver available on the www.st.com/stm32nucleo website.
3. To power the board connect the STM32 Nucleo-144 board to a PC with a USB cable ‘Type-A to Micro-B’ through the USB connector CN1 on the ST-LINK. As a result, the green LED LD6 (PWR) and LD4 (COM) light up and the red LED LD3 blinks.
4. Press button B1 (left button).
5. Observe the blinking frequency of the three LEDs LD1 to LD3 changes, by clicking on the button B1.
6. The software demonstration and the several software examples, that allow the user to use the Nucleo features, are available at the www.st.com/stm32nucleo webpage.
7. Develop an application, using the available examples.

6 Hardware layout and configuration

The STM32 Nucleo-144 board is designed around the STM32 microcontrollers in a 144-pin LQFP package.

Figure 3 shows the connections between the STM32 and its peripherals (ST-LINK/V2-1, push-buttons, LEDs, USB, Ethernet, ST Zio connectors and ST morpho headers).

Figure 4 and *Figure 5* show the location of these features on the STM32 Nucleo-144 board.

The mechanical dimensions of the board are shown in *Figure 6* and *Figure 7*.

Figure 3. Hardware block diagram

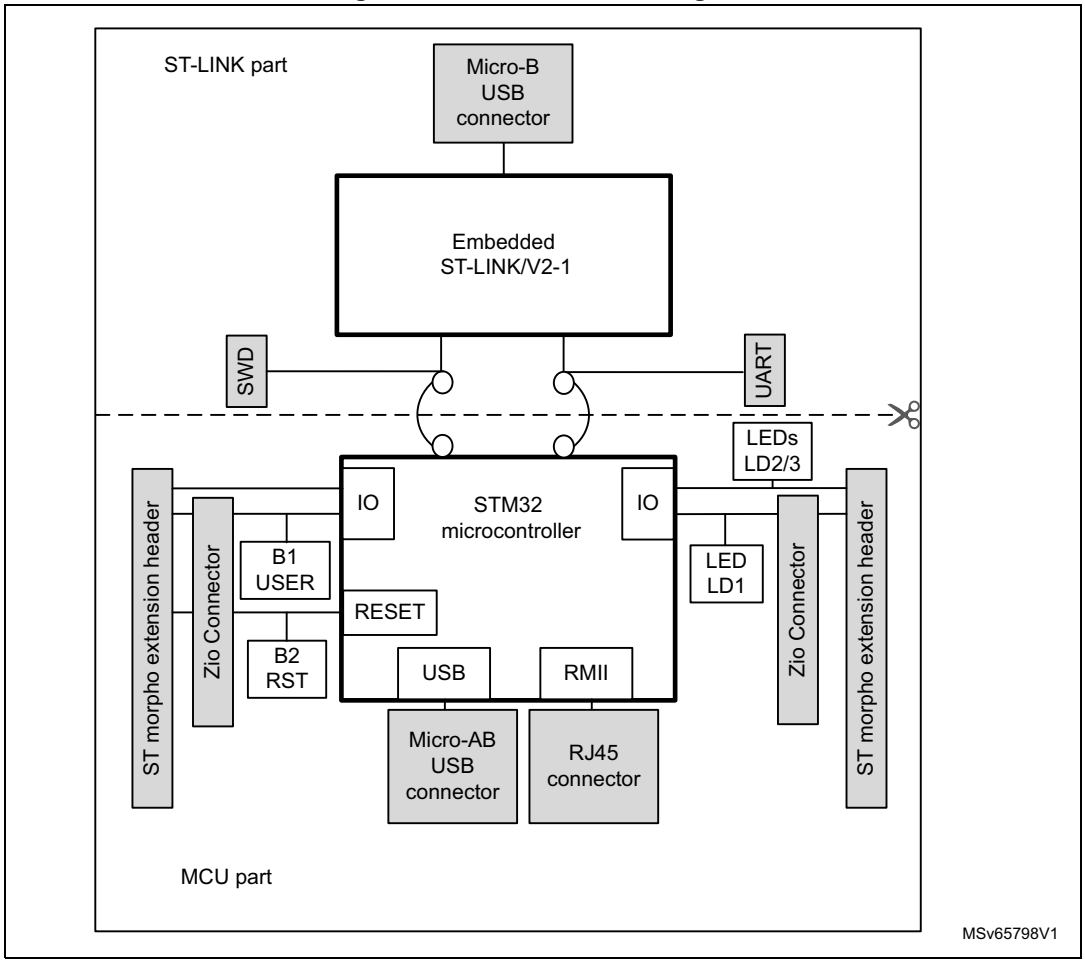


Figure 4. Top layout

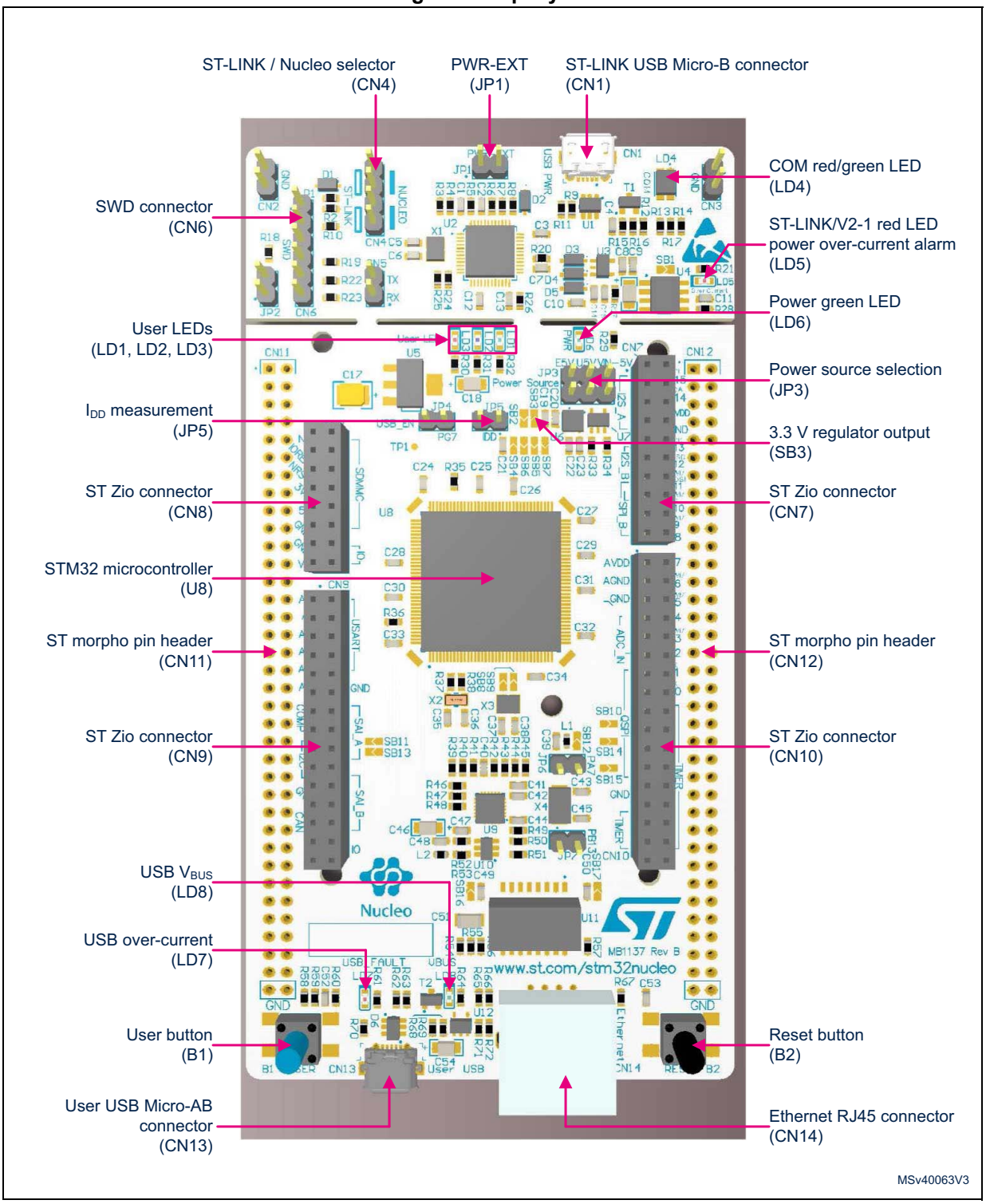
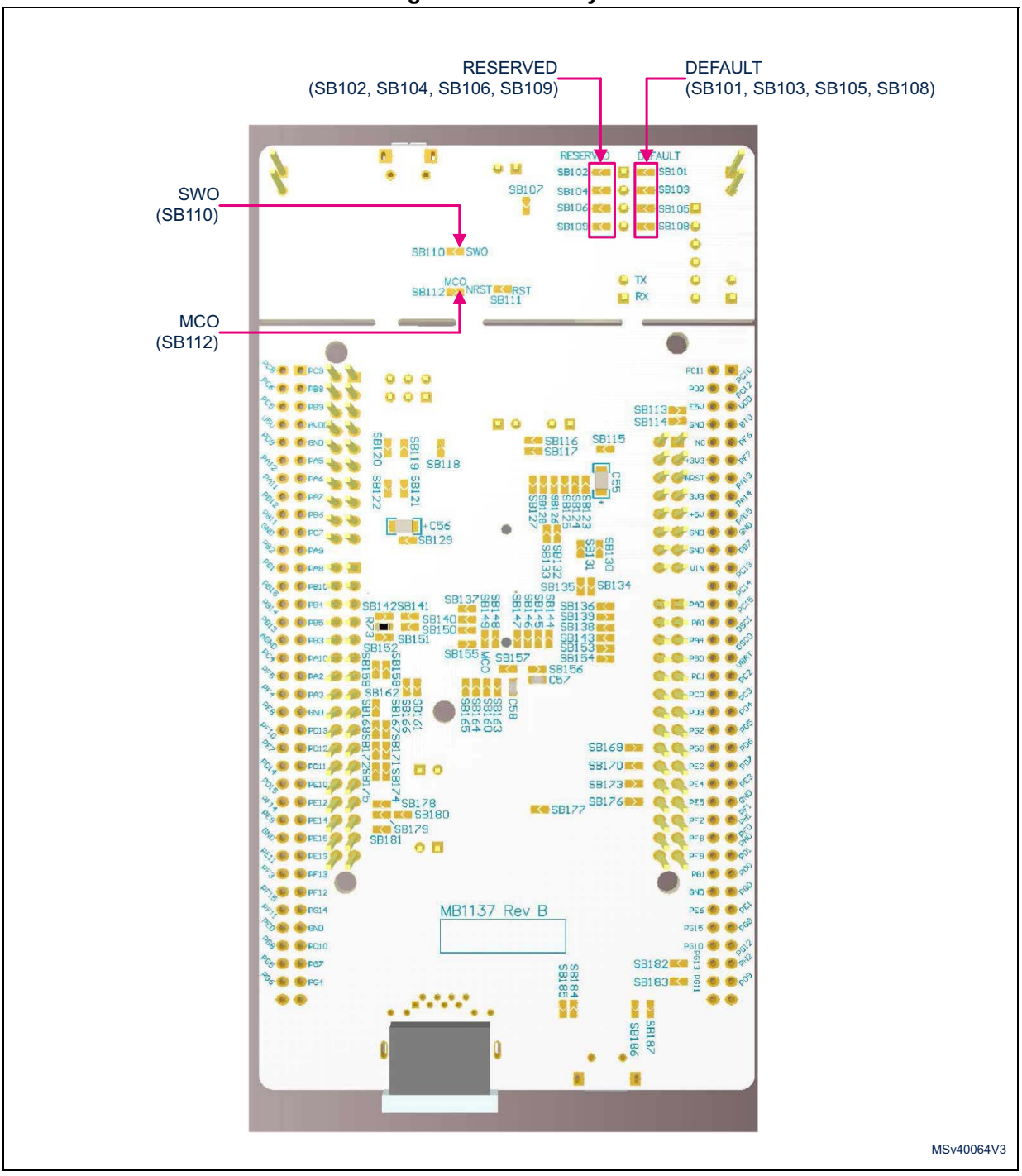


Figure 5. Bottom layout



6.1 Mechanical drawing

Figure 6. Nucleo-144 board mechanical drawing in millimeter

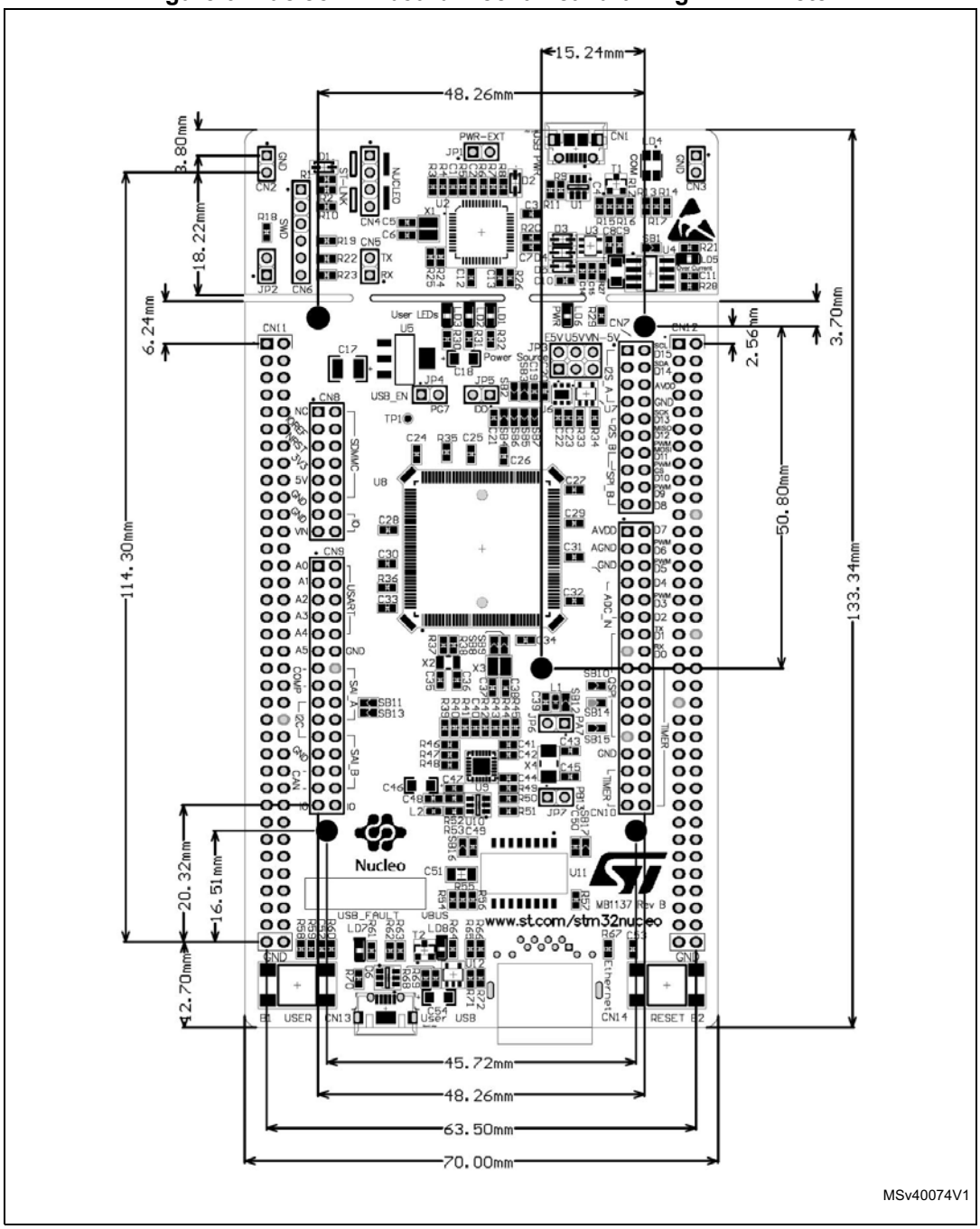
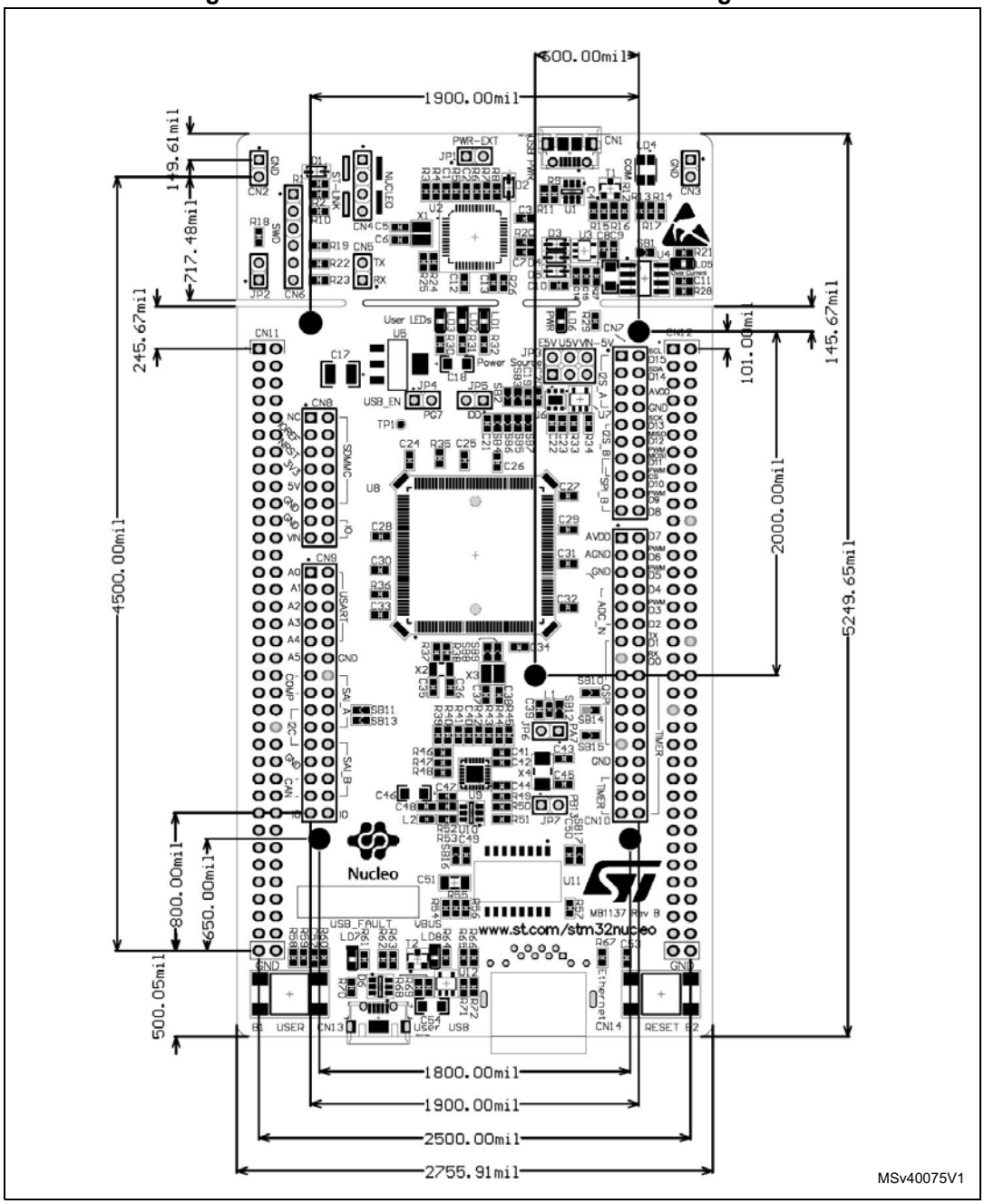


Figure 7. Nucleo-144 board mechanical drawing in mil



6.2 Cuttable PCB

The STM32 Nucleo-144 board is divided into two parts: ST-LINK and target STM32. The ST-LINK part of the PCB can be cut out to reduce the board size. In this case the remaining target STM32 part can only be powered by V_{IN}, E5V and 3.3 V on ST morpho connector CN11, or V_{IN} and 3.3 V on ST Zio connector CN8. It is still possible to use the ST-LINK part to program the STM32, using wires between CN6 and SWD available signals on the ST morpho connector (SWCLK CN11 pin 15, SWDIO CN11 pin 13 and NRST CN11 pin 14).

6.3 Embedded ST-LINK/V2-1

The ST-LINK/V2-1 programming and debugging tool is integrated in the STM32 Nucleo-144 board.

The ST-LINK/V2-1 makes the STM32 Nucleo-144 board mbed enabled.

The embedded ST-LINK/V2-1 supports only SWD for STM32 devices. For information about debugging and programming features refer to the *ST-LINK/V2 in-circuit debugger/programmer for STM8 and STM32* user manual (UM1075), which describes in details all the ST-LINK/V2 features, and to the *Overview of ST-LINK derivatives* technical note (TN1235).

The changes versus ST-LINK/V2 version are listed below.

Additional features supported on ST-LINK/V2-1:

- USB software re-enumeration
- Virtual com port interface on USB
- Mass storage interface on USB
- USB power management request for more than 100mA power on USB

Features not supported on ST-LINK/V2-1:

- SWIM interface
- Minimum supported application voltage limited to 3 V

There are two different ways to use the embedded ST-LINK/V2-1, depending on the jumper state (see *Table 4*):

- Program/debug the STM32 on board
- Program/debug the STM32 in an external application board, using a cable connected to SWD connector CN6

Table 4. CN4 states of the jumpers

Jumper state	Description
Both CN4 jumpers ON	ST-LINK/V2-1 functions enabled for on-board programming (default). See *Section 6.3.3*.
Both CN4 jumpers OFF	ST-LINK/V2-1 functions enabled for external CN6 connector (SWD supported). See *Section 6.3.4*.

6.3.1 Drivers

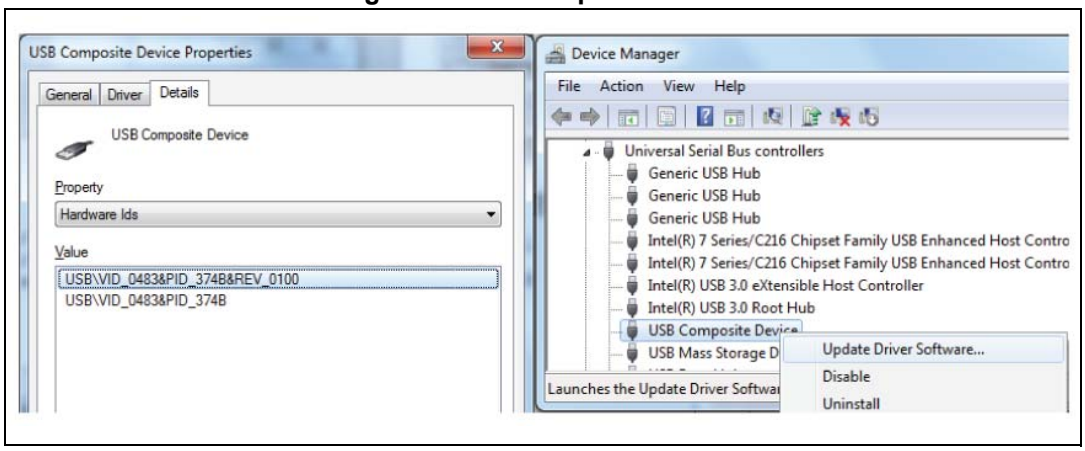
Before connecting the Nucleo-144 board to a Windows® 7, Windows® 8 or Windows® 10 PC via USB, a driver for ST-LINK/V2-1 must be installed. It can be downloaded from the *www.st.com* website.

In case the STM32 Nucleo-144 board is connected to the PC before installing the driver, the PC device manager may report some Nucleo interfaces as “Unknown”.

To recover from this situation, after installing the dedicated driver, the association of “Unknown” USB devices found on the STM32 Nucleo-144 board to this dedicated driver, must be updated in the device manager manually.

Note: It is recommended to proceed using USB Composite Device, as shown in Figure 8.

Figure 8. USB composite device



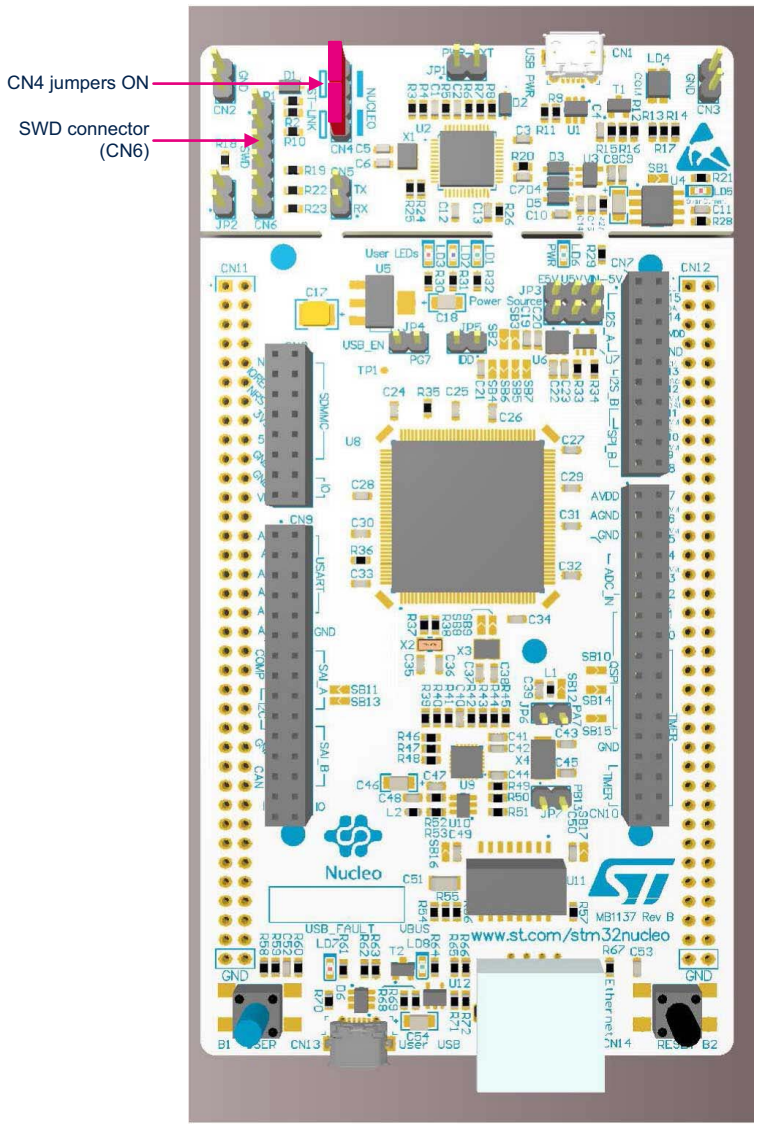
6.3.2 ST-LINK/V2-1 firmware upgrade

The ST-LINK/V2-1 embeds a firmware upgrade mechanism for in-situ upgrade through the USB port. As the firmware may evolve during the lifetime of the ST-LINK/V2-1 product (for example new functionalities, bug fixes, support for new microcontroller families), it is recommended to keep the ST-LINK/V2-1 firmware up to date before starting to use the STM32 Nucleo-144 board. The latest version of this firmware is available from the *www.st.com* website.

6.3.3 Using the ST-LINK/V2-1 to program and debug the on-board STM32

To program the on-board STM32, place the two jumpers marked in red on the connector CN4, as shown in *Figure 9*. The CN6 connector must not be used, since it might disturb the communication with the STM32 microcontroller of the Nucleo-144 board.

Figure 9. Connecting the STM32 Nucleo-144 board to program the on-board STM32



6.3.4 Using ST-LINK/V2-1 to program and debug an external STM32 application

It is very easy to use the ST-LINK/V2-1 to program the STM32 on an external application.

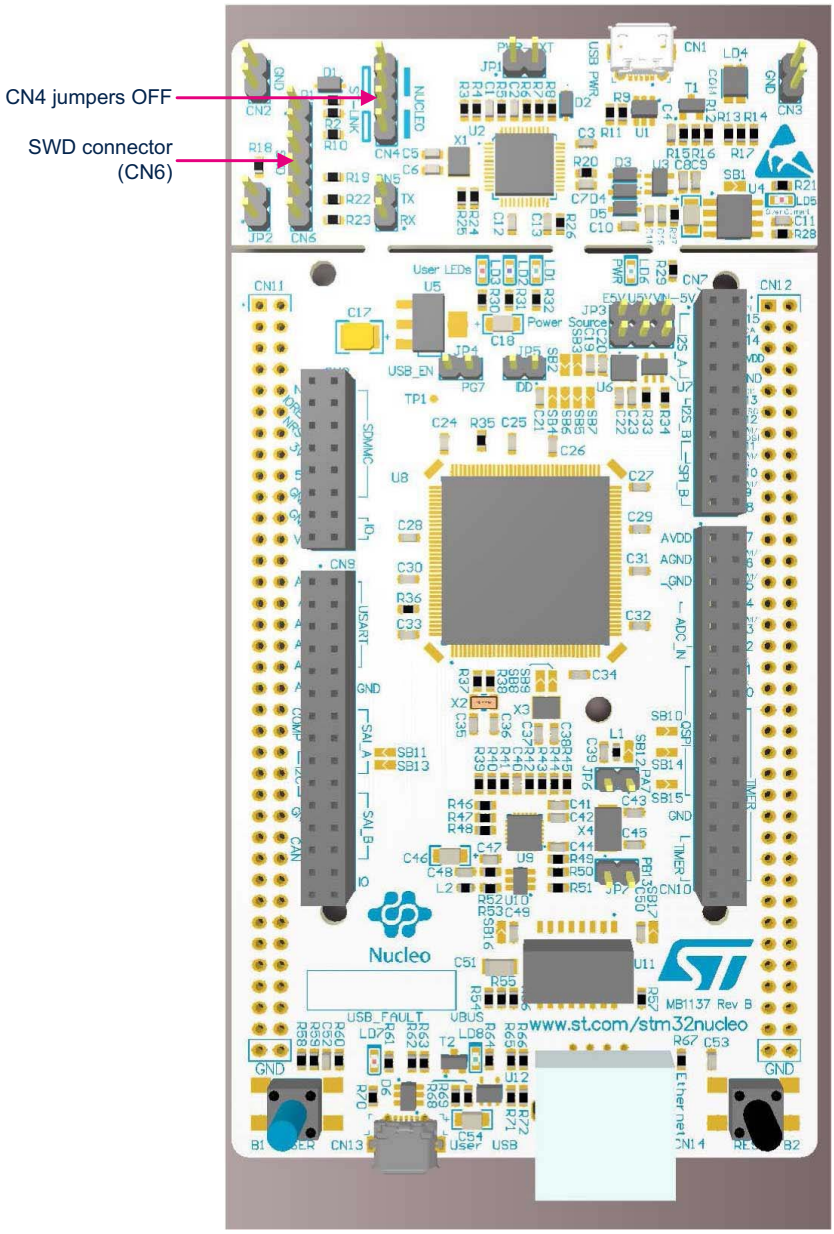
Simply remove the two jumpers from CN4, as shown in *Figure 10* and connect the application to the CN6 debug connector according to *Table 5*.

Note: SB111 NRST (target STM32 RESET) must be OFF when CN6 pin 5 is used in an external application.

Table 5. Debug connector CN6 (SWD)

Pin	CN6	Designation
1	VDD_TARGET	VDD from application
2	SWCLK	SWD clock
3	GND	Ground
4	SWDIO	SWD data input/output
5	NRST	RESET of target STM32
6	SWO	Reserved

Figure 10. Using ST-LINK/V2-1 to program the STM32 on an external application



6.4 Power supply and power selection

The power supply is provided either by the host PC through the USB cable or by an external source: V_{IN} (7 V-12 V), E5V (5 V) or +3.3 V power supply pins on CN8 or CN11. In case V_{IN}, E5V or +3.3 V is used to power the Nucleo-144 board, this power source must comply with the standard EN-60950-1: 2006+A11/2009 and must be Safety Extra Low Voltage (SELV) with limited power capability.

In case the power supply is +3.3 V, the ST-LINK is not powered and cannot be used.

6.4.1 Power supply input from ST-LINK/V2-1 USB connector

The STM32 Nucleo-144 board and shield can be powered from the ST-LINK USB connector CN1 (U5V), by placing a jumper between the pins 3 and 4 of JP3, as shown in *Table 8: Power related jumper*. Note that only the ST-LINK part is power supplied before the USB enumeration, as the host PC only provides 100 mA to the board at that time. During the USB enumeration, the STM32 Nucleo-144 board requires 300mA of current to the host PC. If the host is able to provide the required power, the targeted STM32 microcontroller is powered and the green LED LD6 is turned ON, thus the STM32 Nucleo-144 board and its shield consume a maximum of 300 mA current, not more. If the host is not able to provide the required current, the targeted STM32 microcontroller and the extension boards are not power supplied. As a consequence the green LED LD6 stays turned OFF. In such case it is mandatory to use an external power supply as explained in the next section.

After the USB enumeration succeeds, the ST-LINK U5V power is enabled, by asserting the PWR_EN pin. This pin is connected to a power switch (ST890), which powers the board. This power switch features also a current limitation to protect the PC in case of short-circuit on board. If an overcurrent (more than 500 mA) happens on board, the red LED LD5 is lit.

JP1 is configured according to the maximum current consumption of the board when powered by USB (U5V). JP1 jumper can be set to ON to inform the host PC that the maximum current consumption does not exceed 100 mA (including potential extension board or ST Zio shield). In such condition USB enumeration will always succeed, since no more than 100 mA is requested to the PC. Possible configurations of JP1 are summarized in *Table 6*.

Table 6. JP1 configuration table

Jumper state	Power supply	Allowed current
JP1 jumper OFF	USB power through CN1	300 mA max
JP1 jumper ON		100 mA max
JP1 jumper (do not care)	V_{IN}, +3.3 V, +5 V power	For current limitation refer to *Table 8*

Caution: In case the maximum current consumption of the STM32 Nucleo-144 board and its shield boards exceeds 300 mA, it is mandatory to power the STM32 Nucleo-144 board with an external power supply connected to E5V, V_{IN} or +3.3 V.

Note: In case the board is powered by a USB charger, there is no USB enumeration, so the green LED LD6 stays in OFF state permanently and the target STM32 is not powered. In this specific case the jumper JP1 must be set to ON, to allow the board to be powered anyway. But in any case the current is limited to 500 mA by U4 (ST890).

6.4.2 External power supply inputs

The Nucleo-144 board and its shield boards can be powered in three different ways from an external power supply, depending on the voltage used. The three power sources are summarized in the *Table 7*.

When STM32 Nucleo-144 board is power supplied by V_{IN} or E5V, the jumper configuration must be the following:

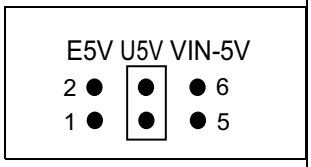
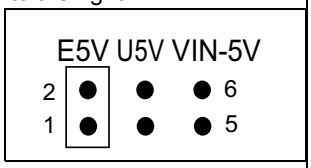
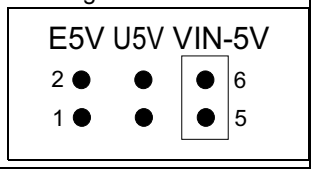
- Jumper JP3 on pin 1 and pin 2 for E5V or jumper JP3 on pin 5 and pin 6 for V_{IN}
- Jumper JP1 OFF

Table 7. External power sources

Input power name	Connector pins	Voltage range	Max current	Limitation
V_{IN}	CN8 pin 15 CN11 pin 24	7 V to 12 V	800 mA	From 7 V to 12 V only and input current capability is linked to input voltage: 800 mA input current when V_{IN}=7 V 450 mA input current when 7 V<V_{IN}<9 V 250 mA input current when 9 V<V_{IN}<12 V
E5V	CN11 pin 6	4.75 V to 5.25 V	500 mA	-
+3.3 V	CN8 pin 7 CN11 pin 16	3 V to 3.6 V	-	Two possibilities: ST-LINK PCB is cut SB3 and SB111 OFF (ST-LINK not powered)

The 5 V power source is selected by the jumper JP3 as shown in *Table 8*.

Table 8. Power related jumper

Jumper	Description
JP3	U5V (ST-LINK V_{BUS}) is used as power source when JP3 is set as shown to the right (Default setting) 
	E5V is used as power source when JP3 is set as shown to the right: 
	V_{IN} is used as power source when JP3 is set as shown to the right: 

Using V_{IN} or E5V as an external power supply

When powered by V_{IN} or E5V, it is still possible to use the ST-LINK for programming or debugging only, but it is mandatory to power the board first using V_{IN} or E5V, then to connect the USB cable to the PC. In this way the enumeration succeeds, thanks to the external power source.

The following power-sequence procedure must be respected:

1. Connect jumper JP3 between pin 1 and pin 2 for E5V or between pin 5 and pin 6 for V_{IN}
2. Check that JP1 is removed
3. Connect the external power source to V_{IN} or E5V
4. Power on the external power supply 7 V< V_{IN} < 12 V to V_{IN}, or 5 V for E5V
5. Check that the green LED LD6 is turned ON
6. Connect the PC to the USB connector CN1

If this order is not respected, the board may be powered by USB (U5V) first, then by V_{IN} or E5V as the following risks may be encountered:

1. If more than 300 mA current is needed by the board, the PC may be damaged or the current supplied can be limited by the PC. As a consequence the board is not powered correctly.
2. 300 mA is requested at enumeration (since JP1 must be OFF) so there is risk that the request is rejected and the enumeration does not succeed if the PC cannot provide such current. Consequently the board is not power supplied (LED LD6 remains OFF).

External power supply input: + 3.3 V

When the 3.3 V is provided by a shield board, it is interesting to use the +3.3 V (CN8 pin 7 or CN11 pin 16) directly as power input. In this case the programming and debugging features are not available, since the ST-LINK is not powered.

When the board is powered with +3.3 V, two different configurations are possible:

- ST-LINK is removed (PCB cut)
- SB3 (3.3 V regulator) and SB111 (NRST) are OFF.

6.4.3 External power supply output

When powered by USB, V_{IN} or E5V, the +5 V (CN8 pin 9 or CN11 pin 18) can be used as output power supply for an ST Zio shield or an extension board. In this case, the maximum current of the power source specified in *Table 7: External power sources* must be respected.

The +3.3 V (CN8 pin 7 or CN11 pin 16) can be used also as power supply output. The current is limited by the maximum current capability of the regulator U6 (500 mA max).

6.5 LEDs

User LD1: a green user LED is connected to the STM32 I/O PB0 (SB120 ON and SB119 OFF) or PA5 (SB119 ON and SB120 OFF) corresponding to the ST Zio D13.

User LD2: a blue user LED is connected to PB7.

User LD3: a red user LED is connected to PB14.

These user LEDs are on when the I/O is HIGH value, and are off when the I/O is LOW.

LD4 COM: the tricolor LED LD4 (green, orange, red) provides information about ST-LINK communication status. LD4 default color is red. LD4 turns to green to indicate that communication is in progress between the PC and the ST-LINK/V2-1, with the following setup:

- Slow blinking red/off: at power-on before USB initialization
- Fast blinking red/off: after the first correct communication between PC and ST-LINK/V2-1 (enumeration)
- Red LED on: when the initialization between the PC and ST-LINK/V2-1 is complete
- Green LED on: after a successful target communication initialization
- Blinking red/green: during communication with target
- Green on: communication finished and successful
- Orange on: communication failure

LD5 USB power fault: LD5 indicates that the board power consumption on USB exceeds 500 mA, consequently the user must power the board using an external power supply.

LD6 PWR: the green LED indicates that the STM32 part is powered and +5 V power is available on CN8 pin 9 and CN11 pin 18.

LD7 and LD8 USB FS: refer to *Section 6.10: USB OTG FS or device*.

6.6 Push-buttons

B1 USER: the user button is connected to the I/O PC13 by default (Tamper support, SB173 ON and SB180 OFF) or PA0 (Wakeup support, SB180 ON and SB173 OFF) of the STM32 microcontroller.

B2 RESET: this push-button is connected to NRST and is used to RESET the STM32 microcontroller.

6.7 JP5 (I_{DD})

Jumper JP5, labeled IDD, is used to measure the STM32 microcontroller consumption by removing the jumper and by connecting an ammeter:

- JP5 ON: STM32 is powered (default)
- JP5 OFF: an ammeter must be connected to measure the STM32 current. If there is no ammeter, the STM32 is not powered

To get a correct current consumption, the Ethernet PHY must be set in power-down mode or SB13 must be removed. Refer to *Section 6.11: Ethernet* for details.

6.8 OSC clock

6.8.1 OSC clock supply

There are four ways to configure the pins corresponding to the external high-speed clock (HSE):

- **MCO from ST-LINK (Default):** MCO output of ST-LINK is used as input clock. This frequency cannot be changed, it is fixed at 8 MHz and connected to the PF0/PH0-OSC_IN of STM32 microcontroller. The configuration must be:
  - SB148 OFF
  - SB112 and SB149 ON
  - SB8 and SB9 OFF
- **HSE on-board oscillator from X3 crystal (not provided):** for typical frequencies and its capacitors and resistors, refer to the STM32 microcontroller datasheet and to the *Oscillator design guide for STM8S, STM8A and STM32 microcontrollers* Application note *(*AN2867) for the oscillator design guide. The X3 crystal has the following characteristics: 8 MHz, 8 pF, 20 ppm. It is recommended to use NX3225GD-8.000M-EXS00A-CG04874 manufactured by NIHON DEMPA KOGYO CO., LTD. The configuration must be:
  - SB148 and SB163 OFF
  - SB8 and SB9 ON
  - C37 and C38 soldered with 4.3 pF capacitors
  - SB112 and SB149 OFF
- **Oscillator from external PF0/PH0:** from an external oscillator through the pin 29 of the CN11 connector. The configuration must be:
  - SB148 ON
  - SB112 and SB149 OFF
  - SB8 and SB9 removed
- **HSE not used:** PF0/PH1 and PF1/PH1 are used as GPIOs instead of as clock. The configuration must be:
  - SB148 and SB163 ON
  - SB112 and SB149 (MCO) OFF
  - SB8 and SB9 removed

6.8.2 OSC 32 KHz clock supply

There are three ways to configure the pins corresponding to low-speed clock (LSE):

- **On-board oscillator (Default):** X2 crystal. Refer to the *Oscillator design guide for STM8S, STM8A and STM32 microcontrollers* Application note *(*AN2867) for oscillator design guide for STM32 microcontrollers. It is recommended to use NX3214SA-32.768KHZ-EXS00A-MU00525 (32.768 kHz, 6 pF load capacitance, 200 ppm) from Nihon Dempa Kogyo CO, LTD.

Note: For STM32F0 and STM32F3 Series it is recommended to use the low-drive-mode configuration of the LSE (low-drive capability in LSEDRV register), due to the 6 pF load capacitance of the crystal on the board.

- **Oscillator from external PC14:** from external oscillator through the pin 25 of CN11 connector. The configuration must be:
  - SB144 and SB145 ON
  - R37 and R38 removed
- **LSE not used:** PC14 and PC15 are used as GPIOs instead of low-speed clock. The configuration must be:
  - SB144 and SB145 ON
  - R37 and R38 removed

6.9 USART communication

The USART3 interface available on PD8 and PD9 of the STM32 can be connected either to ST-LINK or to ST morpho connector. The choice is changed by setting the related solder bridges. By default the USART3 communication is enabled between the target STM32 and both the ST-LINK and the ST morpho connector.

Table 9. USART3 pins

Pin name	Function	Virtual COM port	ST morpho connection
PD8	USART3 TX	SB5 ON and SB7 OFF	SB5 OFF and SB7 ON
PD9	USART3 RX	SB6 ON and SB4 OFF	SB6 OFF and SB4 ON

6.10 USB OTG FS or device

The STM32 Nucleo-144 board supports USB OTG or device-full-speed communication via a USB Micro-AB connector (CN13) and USB power switch (U12) connected to V_{BUS}.

Note: The NUCLEO-F303ZE board supports the USB device FS only. All the other STM32 Nucleo-144 boards support the USB OTG.

Warning: USB Micro–AB connector (CN13) cannot power the Nucleo-144 board. To avoid damaging the STM32, it is mandatory to power the Nucleo-144 before connecting a USB cable on CN13. Otherwise there is a risk of current injection on STM32 I/Os.

A green LED LD8 lights up in one of these cases:

- Power switch (U12) is ON and STM32 Nucleo-144 board works as a USB host
- V_{BUS} is powered by another USB host when the STM32 Nucleo-144 board works as a USB device.

The red LED LD7 lights up if over-current occurs when +5 V is enabled on V_{BUS} in USB host mode.

Note: 1. It is recommended to power Nucleo-144 board by an external power supply when using USB OTG or host function.

2. JP4 must be ON when using USB OTG FS.

The NUCLEO-F303ZE board does not support the OTG function but it supports USB 2.0 full-speed, device-mode communication via a USB Micro-AB connector (CN13). USB disconnection simulation is implemented by PG6, which controls 1.5 K pull-up resistor (R70) on USB D+ line. Detection of 5 V power on USB connector (CN13) is available on PG7 thanks to a bridge between R62 and R63 resistors.

Table 10. USB pins configuration

Pin name	Function	Configuration when using USB connector	Configuration when using ST morpho connector	Remark
PA8	USB SOF	-	-	Test point TP1
PA9	USB V_{BUS}	SB127 ON	SB127 OFF	Not on NUCLEO-F303ZE
PA10	USB ID	SB125 ON	SB125 OFF	Not on NUCLEO-F303ZE
PA11	USB DM	SB133 ON	SB133 OFF	-
PA12	USB DP	SB132 ON	SB132 OFF	-
PG6	USB GPIO OUT	NUCLEO-F303ZE: SB186 ON, SB187 OFF	NUCLEO-F303ZE: SB186 OFF	NUCLEO-F303ZE: D+ pull up control
		All other Nucleo boards: SB186 OFF, SB187 ON	All other Nucleo boards: SB187 OFF	All other Nucleo boards: USB power switch control

Table 10. USB pins configuration (continued)

Pin name	Function	Configuration when using USB connector	Configuration when using ST morpho connector	Remark
PG7	USB GPIO IN	NUCLEO-F303ZE: JP4 ON, SB184 ON, SB185 OFF	JP4 OFF	NUCLEO-F303ZE: V_{BUS} detection
		All other Nucleo boards: JP4 ON, SB184 OFF SB185 ON		All other Nucleo boards: USB overcurrent alarm

ESD protection part ESDA6V1BC6 is implemented on USB port because all USB pins on STM32 can be used as V_{BUS} or GPIO on the STM32 Nucleo-144 board.

Note: If these pins are dedicated to USB port only, the USBLC6-4SC6 protection part is more suitable to protect USB port. If USB pin ID is not used, USBLC6-2SC6 can be used.

6.11 Ethernet

The STM32 Nucleo-144 board supports 10M/100M Ethernet communication by a PHY (U9) and RJ45 connector (CN14). Ethernet PHY is connected to the STM32 microcontroller via the RMII interface. 50MHz clock for the STM32 microcontroller is generated by the PHY RMII_REF_CLK.

Note: 1. NUCLEO-F303ZE, NUCLEO-F412ZG, NUCLEO-F413ZH, NUCLEO-F446ZE, and NUCLEO-F722ZE do not support the Ethernet function.

2. JP6 and JP7 must be ON when using Ethernet.

3. Ethernet PHY must be set in power-down mode (in this mode Ethernet PHY ref clock turns off) to achieve the expected low-power mode current. This is done by configuring Ethernet PHY Basic Control Register (at address 0x00) Bit 11 (Power Down) to '1'. SB13 can also be removed to get the same effect.

Table 11. Ethernet pins

Pin name	Function	Conflict with ST Zio connector signal	Configuration when using Ethernet	Configuration when using ST Zio or ST morpho connector
PA1	RMII Reference Clock	-	SB13 ON	SB13 OFF
PA2	RMII MDIO	-	SB160 ON	SB160 OFF
PC1	RMII MDC	-	SB164 ON	SB164 OFF
PA7	RMII RX Data Valid	D11	JP6 ON	JP6 OFF
PC4	RMII RXD0	-	SB178 ON	SB178 OFF
PC5	RMII RXD1	-	SB181 ON	SB181 OFF
PG11	RMII TX Enable	-	SB183 ON	SB183 OFF

Table 11. Ethernet pins (continued)

Pin name	Function	Conflict with ST Zio connector signal	Configuration when using Ethernet	Configuration when using ST Zio or ST morpho connector
PG13	RXII TXD0	-	SB182 ON	SB182 OFF
PB13	RMII TXD1	I2S_A_CK	JP7 ON	JP7 OFF

6.12 Solder bridges

SBxx can be found on top layer and SB1xx can be found on bottom layer of the Nucleo-144 board.

Table 12. Solder bridges

Bridge	State(1)	Description
SB2 (+3.3 V_PER)	**ON**	Peripheral power +3.3V_PER is connected to +3.3 V.
	OFF	Peripheral power +3.3V_PER is not connected.
SB3 (3.3 V)	**ON**	Output of voltage regulator LD39050PU33R is connected to 3.3 V.
	OFF	Output of voltage regulator LD39050PU33R is not connected.
SB7, SB4 (GPIO)	**ON**	PD8 and PD9 on STM32 are connected to ST morpho connectors CN11 and CN12. If these pins are used on ST morpho connectors, SB5 and SB6 must be OFF.
	OFF	PD8 and PD9 on STM32 are disconnected to ST morpho connectors CN11 and CN12.
SB5, SB6 (ST-LINK-USART)	**ON**	PA2 and PA3 on ST-LINK STM32F103CBT6 are connected to PD8 and PD9 to enable virtual COM port for mbed support. Thus PD8 and PD9 on ST morpho connectors cannot be used.
	OFF	PA2 and PA3 on ST-LINK STM32F103CBT6 are disconnected to PD8 and PD9 on STM32.
SB12 (V_{DDA})	**ON**	V_{DDA} and V_{REF+} on STM32 is connected to V_{DD}.
	OFF	V_{DDA} and V_{REF+} on STM32 is not connected to V_{DD} and can be provided from pin 6 of CN7 (Used for external V_{REF+} provided by ARDUINO® shield).
SB101,103,105,108 (DEFAULT)	**ON**	Reserved, do not modify.
SB102,104,106,109 (RESERVED)	**OFF**	Reserved, do not modify.
SB107 (STM_RST)	**OFF**	No incidence on ST-LINK STM32F103CBT6 NRST signal.
	ON	ST-LINK STM32F103CBT6 NRST signal is connected to GND (ST-LINK reset to reduce power consumption).
SB110 (SWO)	**ON**	SWO signal of the STM32 (PB3) is connected to ST-LINK SWO input.
	OFF	SWO signal of STM32 is not connected.

Table 12. Solder bridges (continued)

Bridge	State[1]	Description
SB111 (NRST)	**ON**	Board RESET signal (NRST) is connected to ST-LINK reset control I/O (T_NRST).
	OFF	Board RESET signal (NRST) is not connected to ST-LINK reset control I/O (T_NRST).
SB113, SB114 (IOREF)	**OFF, ON**	IOREF is connected to +3.3 V.
	ON, OFF	IOREF is connected to +3.3V_PER.
SB116 (SDMMC_D0), SB117 (SDMMC_D1)	**ON**	These pins are connected to ST morpho connector CN12.
	OFF	These pins are disconnected from ST morpho connector CN12 to avoid stub of SDMMC data signals on PCB.
SB120, SB119 (LD1-LED)	**ON, OFF**	Green user LED LD1 is connected to PB0.
	OFF,ON	Green user LED LD1 is connected to D13 of ARDUINO® signal (PA5).
	OFF, OFF	Green user LED LD1 is not connected.
	ON,ON	Forbidden
SB139 (LD2-LED)	**ON**	Blue user LED LD2 is connected to PB7.
	OFF	Blue user LED LD2 is not connected.
SB118 (LD3-LED)	**ON**	Red user LED LD3 is connected to PB14.
	OFF	Red user LED LD3 is not connected.
SB121, SB122 (D11)	**ON, OFF**	D11 (Pin 14 of CN7) is connected to STM32 PA7 (SPI_A_MOSI/TIM_E_PWM1).
	OFF,ON	D11 (Pin 14 of CN7) is connected to STM32 PB5 (SPI_A_MOSI/TIM_D_PWM2).
SB144,145 (X2 crystal)	**OFF**	PC14, PC15 are not connected to ST morpho connector CN11. (X2 used to generate 32KHz clock).
	ON	PC14, PC15 are connected to ST morpho connector CN11. (R37 and R38 must be removed).
SB148 (PF0/PH0), SB163 (PF1/PH1) (Main clock)	**OFF, ON**	PF0/PH0 is not connected to ST morpho PF1/PH1 is connected to ST morpho connector CN11 (MCO is used as main clock for STM32 on PF0/PH0).
	OFF, OFF	PF0/PH0, PF1/PH1 are not connected to ST morpho connector CN11 (X3, C37, C38, SB8 and SB9 provide a clock. In this case SB149 must be removed).
	ON, ON	PF0/PH0 and PF1/PH1 are connected to ST morpho connector CN11. (SB8, SB9 and SB149 must be removed).
SB112, SB149 (MCO)	**ON**	MCO of ST-LINK (STM32F103CBT6) is connected to PF0/PH0 of STM32.
	OFF	MCO of ST-LINK (STM32F103CBT6) is not connected to PF0/PH0 of STM32.
SB8, SB9 (external 8M crystal)	**OFF**	PF0/PH0 and PF1/PH1 are not connected to external 8 MHz crystal X3.
	ON	PF0/PH0 and PF1/PH1 are connected to external 8 MHz crystal X3.

Table 12. Solder bridges (continued)

Bridge	State[1]	Description
SB156 (V_{BAT})	**ON**	V_{BAT} pin of STM32 is connected to V_{DD}.
	OFF	V_{BAT} pin of STM32 is not connected to V_{DD}.
SB173, SB180 (B1-USER)	**ON, OFF**	B1 push-button is connected to PC13.
	OFF,ON	B1 push-button is connected to PA0 (Set SB179 OFF if ST Zio connector is used).
	OFF,OFF	B1 push-button is not connected.
SB179 (PA0)	**ON**	PA0 is connected to ST Zio connector (Pin 29 of CN10)
	OFF	PA0 is not connected to ST Zio connector (Pin 29 of CN10)
SB142, SB152 (BOOT1, Only for F2 and F4 Series)	**OFF, OFF**	BOOT1 (PB2) function is not used.
	ON, OFF	BOOT1 (PB2) is pulled up.
	OFF,ON	BOOT1 (PB2) is pulled down.
	ON, ON	Forbidden
SB147,SB157 (A4 and A5) Or SB167, SB171 (only for NUCLEO-F303ZE) Or SB140,SB150 (only for NUCLEO-F412ZG and NUCLEO-F413ZH)	**ON**	ADC_IN are connected to A4 and A5 (pin 9 and 11) on ST Zio connector CN9. Thus SB138 and SB143 must be OFF.
	OFF	ADC_IN are not connected to A4 and A5 (pin 9 and 11) on ST Zio connector CN9.
SB138,SB143 (I2C on A4 and A5)	**OFF**	PB9 and PB8 (I^2C) are not connected to A4 and A5 (pin 9 and 11) on ST Zio connector CN9.
	ON	PB9 and PB8 (I2C) are connected to A4 and A5 (pin 9 and 11) on ST Zio connector CN9. Thus SB147 and SB157 (or SB167 and SB171 for NUCLEO-F303ZE or SB140 and SB150 for NUCLEO-F412ZG and NUCLEO-F413ZH) must be OFF.
RMII Signals SB13 (PA1), SB164 (PC1), SB160 (PA2), SB178 (PC4), SB181 (PC5), SB182 (PG13), SB183 (PG11)	**ON**	These pins are used as RMII signals and connected to Ethernet PHY. These ports must not be used on ST morpho or ST Zio connectors.
	OFF	These pins are used as GPIOs on ST morpho connectors and not connected to Ethernet PHY.
SB177 (Ethernet nRST)	**ON**	NRST of STM32 is connected to Ethernet PHY (U9).
	OFF	NRST of STM32 is not connected to Ethernet PHY (U9).
USB signals: SB186 (NUCLEO-F303ZE) or SB187 (all other Nucleo boards) (PG6)	**ON**	PG6 is connected to R70 to control USB D+ pull up (NUCLEO-F303ZE). PG6 is connected to 5 V switch Enable (U12) to control V_{BUS} or CN13 (All other NUCLEO).
	OFF	This pin is used as GPIO on ST morpho connectors.
SB132 (PA12), SB133 (PA11)	**ON**	These pins are used as D+ and D- on USB connector CN13.
	OFF	These pins are used as GPIOs on ST morpho connectors.

1. Default SBx state is shown in bold.

All the other solder bridges present on the STM32 Nucleo-144 board are used to configure several I/Os and power supply pins for compatibility of features and pinout with the target STM32 supported.

The STM32 Nucleo-144 board is delivered with the solder bridges configured, according to the target STM32 supported.

6.13 Extension connectors

For each STM32 Nucleo-144 board the following figures show the signals connected by default to the ST Zio connectors (CN7, CN8, CN9, CN10), including the support for ARDUINO® Uno V3.

Figure 11. NUCLEO-F207ZG, NUCLEO-F429ZI, NUCLEO-F439ZI, NUCLEO-F746ZG, NUCLEO-F756ZG, NUCLEO-F767ZI and NUCLEO-H743ZI

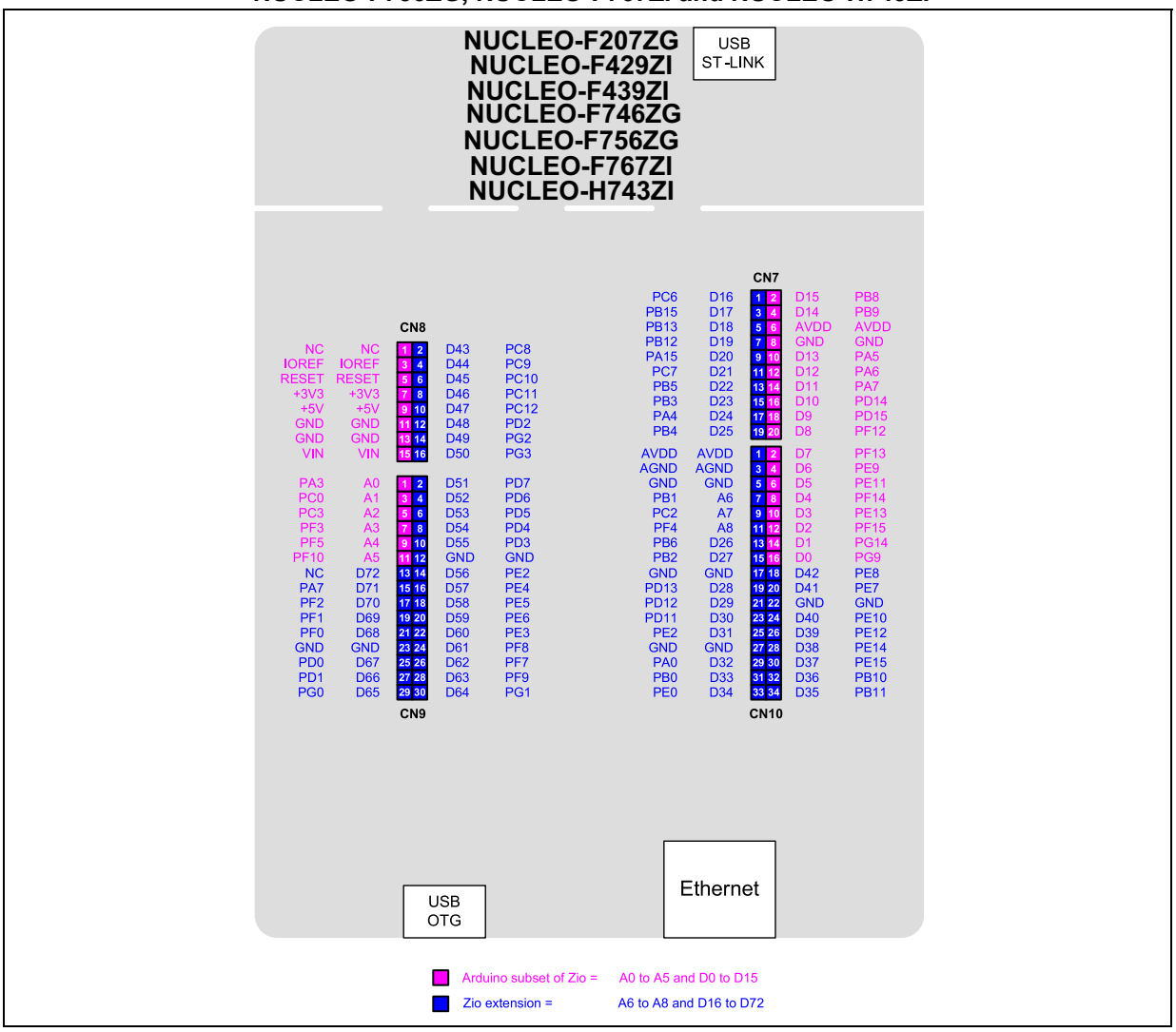


Figure 12. NUCLEO-F303ZE

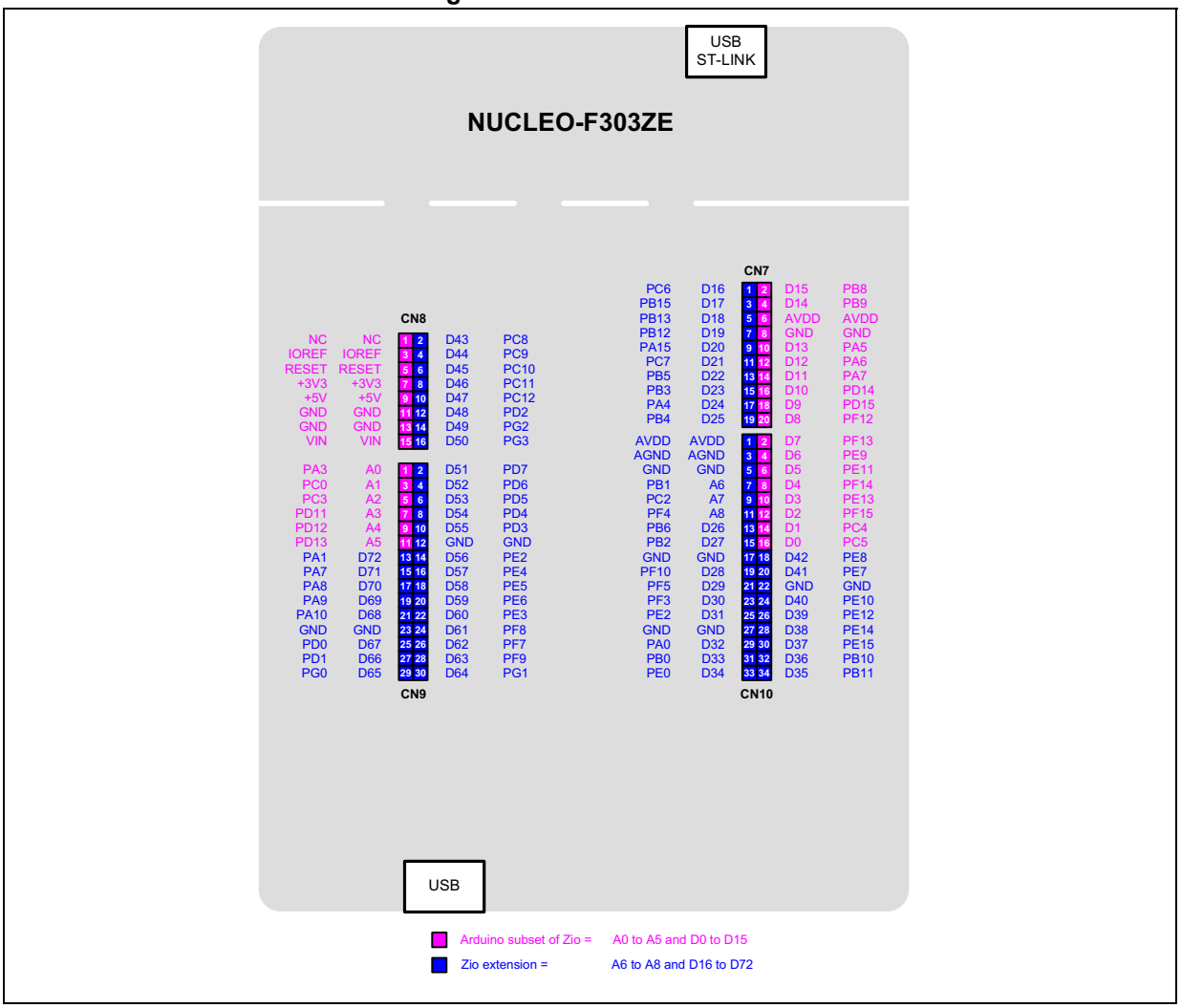


Figure 13. NUCLEO-F412ZG and NUCLEO-F413ZH

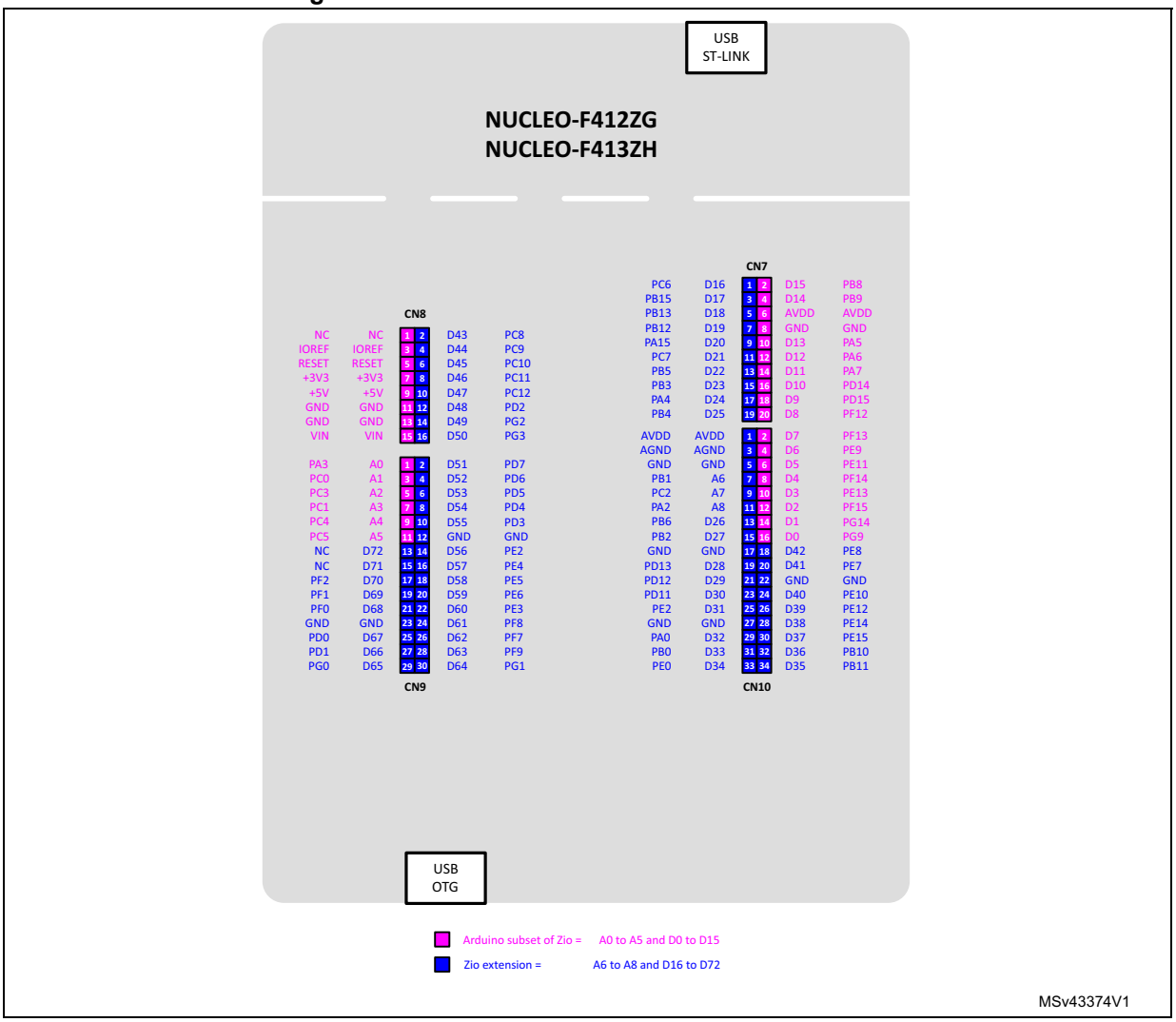
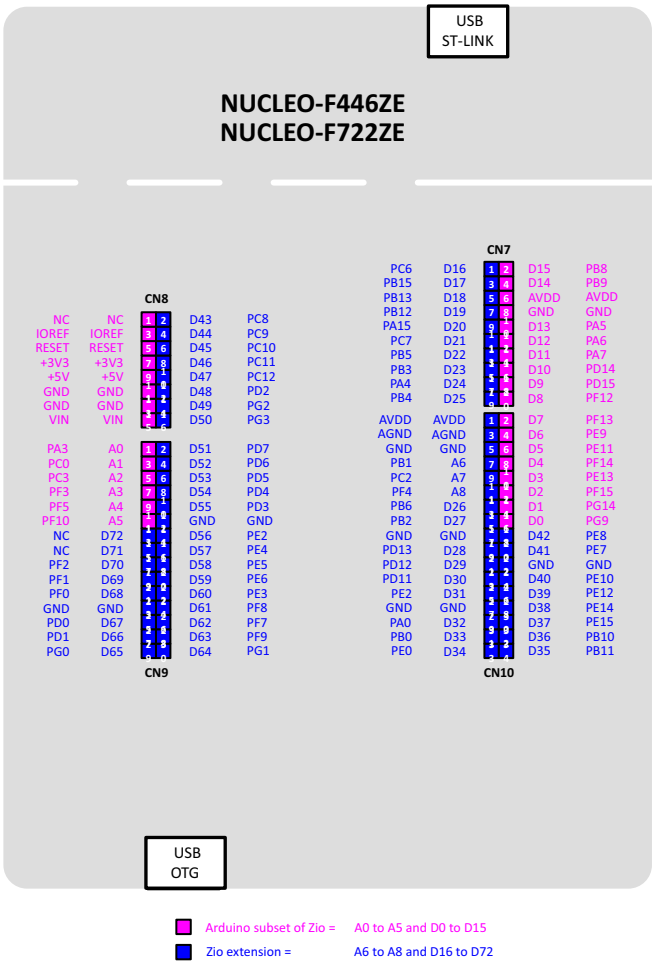


Figure 14. NUCLEO-F446ZE and NUCLEO-F722ZE



6.14 ST Zio connectors

CN7, CN8, CN9 and CN10 are female on top side and male on bottom side connectors. They include support for ARDUINO® Uno V3. Most shields designed for ARDUINO® Uno V3 can fit to the STM32 Nucleo-144 board.

To cope with ARDUINO® Uno V3, apply the following modifications:

- SB138 and SB143 must be ON
- SB140/147/150/157/167/171 must be OFF to connect I^2C on A4 (pin 5) and A5 (pin 6 of CN9).

Caution:1 The I/Os of STM32 microcontroller are 3.3 V compatible instead of 5 V for ARDUINO® Uno V3.

Caution:2 SB12 must be removed before implementing ARDUINO® shield with V_{REF+} power being provided on CN7 pin 6. Refer to *Table 12: Solder bridges* for details on SB12.

Table 13 to *Table 20* show the pin assignment for each STM32 microcontroller on the ST Zio connectors.

Table 13. NUCLEO-F207ZG pin assignments

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
Left connectors						
CN8	1	NC	NC	-	-	ARDUINO® support
	3	IOREF	IOREF	-	3.3 V Ref	
	5	RESET	RESET	NRST	RESET	
	7	+3.3 V	+3.3 V	-	3.3 V input/output	
	9	+5 V	+5 V	-	5 V output	
	11	GND	GND	-	ground	
	13	GND	GND	-	-	
	15	V_{IN}	V_{IN}	-	Power input	
	2	D43	SDMMC_D0	PC8	SDMMC/I2S_A	-
	4	D44	SDMMC_D1/ I2S_A_CKIN	PC9		
	6	D45	SDMMC_D2	PC10		
	8	D46	SDMMC_D3	PC11		
	10	D47	SDMMC_CK	PC12		
	12	D48	SDMMC_CMD	PD2		
	14	D49	I/O	PG2	I/O	
	16	D50	I/O	PG3		
CN9	1	A0	ADC	PA3	ADC123_IN3	ARDUINO® support
	3	A1	ADC	PC0	ADC123_IN10	
	5	A2	ADC	PC3	ADC123_IN13	
	7	A3	ADC	PF3	ADC3_IN9	
	9	A4	ADC	PF5 or PB9(1)	ADC3_IN15 (PF5) or I2C1_SDA (PB9)	
	11	A5	ADC	PF10 or PB8(1)	ADC3_IN8 (PF10) or I2C1_SCL (PB8)	
	13	D72	NC	-	-	-
	15	D71	I/O	PA7(2)	I/O	
	17	D70	I2C_B_SMBA	PF2	I2C_2	
	19	D69	I2C_B_SCL	PF1		
	21	D68	I2C_B_SDA	PF0		
	23	GND	GND	-	ground	

Table 13. NUCLEO-F207ZG pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN9	25	D67	CAN_RX	PD0	CAN_1	-
	27	D66	CAN_TX	PD1		
	29	D65	I/O	PG0	I/O	
	2	D51	USART_B_SCLK	PD7	USART_2	
	4	D52	USART_B_RX	PD6		
	6	D53	USART_B_TX	PD5		
	8	D54	USART_B_RTS	PD4		
	10	D55	USART_B_CTS	PD3		
	12	GND	GND	-	ground	
	14	D56	I/O	PE2(3)	I/O	
	16	D57	I/O	PE4		
	18	D58	I/O	PE5		
	20	D59	I/O	PE6		
	22	D60	I/O	PE3		
	24	D61	I/O	PF8		
	26	D62	I/O	PF7		
	28	D63	I/O	PF9		
	30	D64	I/O	PG1		
Right Connectors						
CN7	1	D16	I2S_A_MCK	PC6	I2S_2	-
	3	D17	I2S_A_SD	PB15		
	5	D18	I2S_A_CK	PB13(4)		
	7	D19	I2S_A_WS	PB12		
	9	D20	I2S_B_WS	PA15	I2S_3 / SPI3	
	11	D21	I2S_B_MCK	PC7		
	13	D22	I2S_B_SD/ SPI_B_MOSI	PB5		
	15	D23	I2S_B_CK/ SPI_B_SCK	PB3		
	17	D24	SPI_B_NSS	PA4		
	19	D25	SPI_B_MISO	PB4		
	2	D15	I2C_A_SCL	PB8	I2C1_SCL	ARDUINO® support
	4	D14	I2C_A_SDA	PB9	I2C1_SDA	
	6	AREF	AREF	-	AVDD/VREF+	
	8	GND	GND	-	ground	

Table 13. NUCLEO-F207ZG pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN7	10	D13	SPI_A_SCK	PA5	SPI1_SCK	ARDUINO® support
	12	D12	SPI_A_MISO	PA6	SPI1_MISO	
	14	D11	SPI_A_MOSI/ TIM_E_PWM1	PA7(1)(2) or PB5(1)	SPI1_MOSI/ TIM14_CH1	
	16	D10	SPI_A_CS/ TIM_B_PWM3	PD14	SPI1_CS/ TIM4_CH3	
	18	D9	TIMER_B_PWM2	PD15	TIM4_CH4	
	20	D8	I/O	PF12	-	-
CN10	1	AVDD	AVDD	-	Analog VDD	
	3	AGND	AGND	-	Analog ground	
	5	GND	GND	-	ground	
	7	A6	ADC_A_IN	PB1	ADC12_IN9	
	9	A7	ADC_B_IN	PC2	ADC123_IN12	
	11	A8	ADC_C_IN	PF4	ADC3_IN14	
	13	D26	I/O	PB6	I/O	
	15	D27	I/O	PB2	-	
	17	GND	GND	-	ground	
	19	D28	I/O	PD13	I/O	
	21	D29	I/O	PD12		
	23	D30	I/O	PD11		
	25	D31	I/O	PE2(3)		
	27	GND	GND	-	ground	
	29	D32	TIMER_C_PWM1	PA0	TIM2_CH1	
	31	D33	TIMER_D_PWM1	PB0	TIM3_CH3	
	33	D34	TIMER_B_ETR	PE0	TIM4_ETR	
	2	D7	I/O	PF13	-	ARDUINO® support
	4	D6	TIMER_A_PWM1	PE9	TIM1_CH1	
	6	D5	TIMER_A_PWM2	PE11	TIM1_CH2	
	8	D4	I/O	PF14	-	
	10	D3	TIMER_A_PWM3	PE13	TIM1_CH3	
	12	D2	I/O	PF15	-	
	14	D1	USART_A_TX	PG14	USART6	
	16	D0	USART_A_RX	PG9	-	
	18	D42	TIMER_A_PWM1N	PE8	TIM1_CH1N	-

Table 13. NUCLEO-F207ZG pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN10	20	D41	TIMER_A_ETR	PE7	TIM1_ETR	-
	22	GND	GND	-	ground	
	24	D40	TIMER_A_PWM2N	PE10	TIM1_CH2N	
	26	D39	TIMER_A_PWM3N	PE12	TIM1_CH3N	
	28	D38	I/O	PE14	I/O	
	30	D37	TIMER_A_BKIN1	PE15	TIM1_BKIN1	
	32	D36	TIMER_C_PWM2	PB10	TIM2_CH3	
	34	D35	TIMER_C_PWM3	PB11	TIM2_CH4	

1. For more details refer to *Table 12: Solder bridges*.
2. PA7 is used as D11 and connected to CN7 pin 14 by default, if JP6 is ON, it is also connected to both Ethernet PHY as RMII_DV and CN9 pin 15. In this case only one function of the Ethernet or D11 must be used.
3. PE2 is connected to both CN9 pin 14 (I/O) and CN10 pin 25 (I/O). Only one connector pin must be used at one time.
4. PB13 is used as I2S_A_CK and connected to CN7 pin 5 by default, if JP7 is ON, it is also connected to Ethernet PHY as RMII_TXD1. In this case only one function of Ethernet or I2S_A must be used.

Table 14. NUCLEO-F303ZE pin assignments

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
Left connectors						
CN8	1	NC	NC	-	-	ARDUINO® support
	3	IOREF	IOREF	-	3.3 V Ref	
	5	RESET	RESET	NRST	RESET	
	7	+3.3 V	+3.3 V	-	3.3 V input/output	
	9	+5 V	+5 V	-	5 V output	
	11	GND	GND	-	ground	
	13	GND	GND	-	ground	
	15	V_{IN}	V_{IN}	-	Power input	
	2	D43	I/O	PC8	I/O	-
	4	D44	I2S_A_CKIN	PC9	I2S_A	
	6	D45	I/O	PC10	I/O	
	8	D46	I/O	PC11		
	10	D47	I/O	PC12		
	12	D48	I/O	PD2		
	14	D49	I/O	PG2		
	16	D50	I/O	PG3		
CN9	1	A0	ADC	PA3	ADC1_IN4	ARDUINO® support
	3	A1	ADC	PC0	ADC12_IN6	
	5	A2	ADC	PC3	ADC12_IN9	
	7	A3	ADC	PD11	ADC34_IN8	
	9	A4	ADC	PD12 or PB9(1)	ADC34_IN9 (PD12) or I2C1_SDA (PB9)	
	11	A5	ADC	PD13 or PB8(1)	ADC34_IN10 (PD13) or I2C1_SCL (PB8)	
	13	D72	COMP1_INP	PA1	COMP	-
	15	D71	COMP2_INP	PA7(2)	I2C_2	
	17	D70	I2C_B_SMBA	PA8		
	19	D69	I2C_B_SCL	PA9		
	21	D68	I2C_B_SDA	PA10		
	23	GND	GND	-	ground	
	25	D67	CAN_RX	PD0	CAN_1	
	27	D66	CAN_TX	PD1		

Table 14. NUCLEO-F303ZE pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN9	29	D65	I/O	PG0	I/O	-
	2	D51	USART_B_SCLK	PD7	USART_2	
	4	D52	USART_B_RX	PD6		
	6	D53	USART_B_TX	PD5		
	8	D54	USART_B_RTS	PD4		
	10	D55	USART_B_CTS	PD3		
	12	GND	GND	-	ground	
	14	D56	I/O	PE2(3)	I/O	
	16	D57	I/O	PE4		
	18	D58	I/O	PE5		
	20	D59	I/O	PE6		
	22	D60	I/O	PE3		
	24	D61	I/O	PF8		
	26	D62	I/O	PF7		
	28	D63	I/O	PF9		
	30	D64	I/O	PG1		
Right Connectors						
CN7	1	D16	I2S_A_MCK	PC6	I2S_2	-
	3	D17	I2S_A_SD	PB15	-	
	5	D18	I2S_A_CK	PB13		
	7	D19	I2S_A_WS	PB12		
	9	D20	I2S_B_WS	PA15	I2S_3 / SPI3	
	11	D21	I2S_B_MCK	PC7		
	13	D22	I2S_B_SD/ SPI_B_MOSI	PB5		
	15	D23	I2S_B_CK/ SPI_B_SCK	PB3		
	17	D24	SPI_B_NSS	PA4		
	19	D25	SPI_B_MISO	PB4		
	2	D15	I2C_A_SCL	PB8	I2C1_SCL	ARDUINO® support
	4	D14	I2C_A_SDA	PB9	I2C1_SDA	
	6	AREF	AREF	-	AVDD/VREF+	
	8	GND	GND	-	ground	
	10	D13	SPI_A_SCK	PA5	SPI1_SCK	
	12	D12	SPI_A_MISO	PA6	SPI1_MISO	

Table 14. NUCLEO-F303ZE pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN7	14	D11	SPI_A_MOSI/ TIM_E_PWM1	PA7(1)(2) or PB5(1)	SPI1_MOSI/ TIM14_CH1	ARDUINO® support
	16	D10	SPI_A_CS/ TIM_B_PWM3	PD14	SPI1_CS/ TIM4_CH3	
	18	D9	TIMER_B_PWM2	PD15	TIM4_CH4	
	20	D8	I/O	PF12	-	
CN10	1	AVDD	AVDD	-	Analog VDD	-
	3	AGND	AGND	-	Analog ground	
	5	GND	GND	-	ground	
	7	A6	ADC_A_IN	PB1	ADC3_IN1	
	9	A7	ADC_B_IN	PC2	ADC12_IN8	
	11	A8	ADC_C_IN	PF4	ADC3_IN14	
	13	D26	I/O	PB6	I/O	
	15	D27	I/O	PB2		
	17	GND	GND	-	ground	
	19	D28	I/O	PF10	I/O	
	21	D29	I/O	PF5		
	23	D30	I/O	PF3		
	25	D31	I/O	PE2(3)		
	27	GND	GND	-	ground	
	29	D32	TIMER_C_PWM1	PA0	TIM2_CH1	
	31	D33	TIMER_D_PWM1	PB0	TIM3_CH3	
	33	D34	TIMER_B_ETR	PE0	TIM4_ETR	
	2	D7	I/O	PF13	-	ARDUINO® support
	4	D6	TIMER_A_PWM1	PE9	TIM1_CH1	
	6	D5	TIMER_A_PWM2	PE11	TIM1_CH2	
	8	D4	I/O	PF14	-	
	10	D3	TIMER_A_PWM3	PE13	TIM1_CH3	-
	12	D2	I/O	PF15	-	
	14	D1	USART_A_TX	PC4	USART1	
	16	D0	USART_A_RX	PC5		
	18	D42	TIMER_A_PWM1N	PE8	TIM1_CH1N	
	20	D41	TIMER_A_ETR	PE7	TIM1_ETR	
	22	GND	GND	-	ground	

Table 14. NUCLEO-F303ZE pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN10	24	D40	TIMER_A_PWM2N	PE10	TIM1_CH2N	-
	26	D39	TIMER_A_PWM3N	PE12	TIM1_CH3N	
	28	D38	TIMER_A_BKIN2	PE14	TIM1_BKIN2	
	30	D37	TIMER_A_BKIN1	PE15	TIM1_BKIN1	
	32	D36	TIMER_C_PWM2	PB10	TIM2_CH3	
	34	D35	TIMER_C_PWM3	PB11	TIM2_CH4	

1. For more details refer to *Table 12: Solder bridges*.
2. PA7 is used as D11 and connected to CN7 pin 14 by default, if JP6 is ON, it is also connected to CN9 pin 15 as COMP2_INP. In this case only one function of the Comparator input or D11 must be used.
3. PE2 is connected to both CN9 pin 14 (I/O) and CN10 pin 25 (I/O). Only one connector pin must be used at one time.

Table 15. NUCLEO-F412ZG pin assignments

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
Left connectors						
CN8	1	NC	NC	-	-	ARDUINO® compatible
	3	IOREF	IOREF	-	3.3 V Ref	
	5	RESET	RESET	NRST	RESET	
	7	+3.3 V	+3.3 V	-	3.3 V input/output	
	9	+5 V	+5 V	-	5 V output	
	11	GND	GND	-	ground	
	13	GND	GND	-	ground	
	15	V_{IN}	V_{IN}	-	Power input	
	2	D43	SDMMC_D0	PC8	SDMMC/I2S_A	-
	4	D44	SDMMC_D1/ I2S_A_CKIN	PC9		
	6	D45	SDMMC_D2	PC10		
	8	D46	SDMMC_D3	PC11		
	10	D47	SDMMC_CK	PC12		
	12	D48	SDMMC_CMD	PD2		
	14	D49	I/O	PG2	I/O	
	16	D50	I/O	PG3		
CN9	1	A0	ADC	PA3	ADC1_IN3	ARDUINO® compatible
	3	A1	ADC	PC0	ADC1_IN10	
	5	A2	ADC	PC3	ADC1_IN13	
	7	A3	ADC	PC1	ADC1_IN11	
	9	A4	ADC	PC4 or PB9(1)	ADC1_IN14 (PC4) or I2C1_SDA (PB9)	
	11	A5	ADC	PC5 or PB8(1)	ADC1_IN15 (PC5) or I2C1_SCL (PB8)	
	13	D72	NC	-	-	-
	15	D71	NC	-	-	
	17	D70	I2C_B_SMBA	PF2	I2C_2	
	19	D69	I2C_B_SCL	PF1		
	21	D68	I2C_B_SDA	PF0		
	23	GND	GND	-	ground	
	25	D67	CAN_RX	PD0	CAN_1	

Table 15. NUCLEO-F412ZG pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN9	27	D66	CAN_TX	PD1	CAN_1	-
	29	D65	I/O	PG0	I/O	
	2	D51	USART_B_SCLK	PD7	USART_2	
	4	D52	USART_B_RX	PD6		
	6	D53	USART_B_TX	PD5		
	8	D54	USART_B_RTS	PD4		
	10	D55	USART_B_CTS	PD3		
	12	GND	GND	-	ground	
	14	D56	I/O	PE2(2)	I/O	
	16	D57	I/O	PE4		
	18	D58	I/O	PE5		
	20	D59	I/O	PE6		
	22	D60	I/O	PE3	I/O	
	24	D61	I/O	PF8		
	26	D62	I/O	PF7		
	28	D63	I/O	PF9		
	30	D64	I/O	PG1	I/O	
Right Connectors						
CN7	1	D16	I2S_A_MCK	PC6	I2S_2	-
	3	D17	I2S_A_SD	PB15		
	5	D18	I2S_A_CK	PB13		
	7	D19	I2S_A_WS	PB12		
	9	D20	I2S_B_WS	PA15	I2S_3 / SPI3	
	11	D21	I2S_B_MCK	PC7		
	13	D22	I2S_B_SD/ SPI_B_MOSI	PB5		
	15	D23	I2S_B_CK/ SPI_B_SCK	PB3		
	17	D24	SPI_B_NSS	PA4		
	19	D25	SPI_B_MISO	PB4		
	2	D15	I2C_A_SCL	PB8	I2C1_SCL	ARDUINO® compatible
	4	D14	I2C_A_SDA	PB9	I2C1_SDA	
	6	AREF	AREF	-	AVDD/VREF+	
	8	GND	GND	-	ground	
	10	D13	SPI_A_SCK	PA5	SPI1_SCK	

Table 15. NUCLEO-F412ZG pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN7	12	D12	SPI_A_MISO	PA6	SPI1_MISO	ARDUINO® compatible
	14	D11	SPI_A_MOSI/ TIM_E_PWM1	PA7(1)or PB5(1)	SPI1_MOSI/ TIM14_CH1	
	16	D10	SPI_A_CS/ TIM_B_PWM3	PD14	SPI1_CS/ TIM4_CH3	
	18	D9	TIMER_B_PWM2	PD15	TIM4_CH4	
	20	D8	I/O	PF12	-	
CN10	1	AVDD	AVDD	-	Analog VDD	-
	3	AGND	AGND	-	Analog ground	
	5	GND	GND	-	ground	
	7	A6	ADC_A_IN	PB1	ADC1_IN9	
	9	A7	ADC_B_IN	PC2	ADC1_IN12	
	11	A8	ADC_C_IN	PA2	ADC1_IN2	
	13	D26	QSPI_CS	PB6	QSPI_BK1	
	15	D27	QSPI_CLK	PB2	QSPI_CLK	
	17	GND	GND	-	ground	
	19	D28	QSPI_BK1_IO3	PD13	QSPI_BK1	
	21	D29	QSPI_BK1_IO1	PD12		
	23	D30	QSPI_BK1_IO0	PD11		
	25	D31	QSPI_BK1_IO2	PE2(2)		
	27	GND	GND	-	ground	
	29	D32	TIMER_C_PWM1	PA0	TIM2_CH1	
	31	D33	TIMER_D_PWM1	PB0	TIM3_CH3	
	33	D34	TIMER_B_ETR	PE0	TIM4_ETR	
	2	D7	I/O	PF13	-	ARDUINO® compatible
	4	D6	TIMER_A_PWM1	PE9	TIM1_CH1	
	6	D5	TIMER_A_PWM2	PE11	TIM1_CH2	
	8	D4	I/O	PF14	-	
	10	D3	TIMER_A_PWM3	PE13	TIM1_CH3	
	12	D2	I/O	PF15	-	
	14	D1	USART_A_TX	PG14	USART6	
	16	D0	USART_A_RX	PG9		
	18	D42	TIMER_A_PWM1N	PE8	TIM1_CH1N	-
	20	D41	TIMER_A_ETR	PE7	TIM1_ETR	
	22	GND	GND	-	ground	

Table 15. NUCLEO-F412ZG pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN10	24	D40	TIMER_A_PWM2N	PE10	TIM1_CH2N	-
	26	D39	TIMER_A_PWM3N	PE12	TIM1_CH3N	
	28	D38	I/O	PE14	I/O	
	30	D37	TIMER_A_BKIN1	PE15	TIM1_BKIN1	
	32	D36	TIMER_C_PWM2	PB10	TIM2_CH3	
	34	D35	TIMER_C_PWM3	PB11	TIM2_CH4	

1. For more details refer to *Table 12: Solder bridges*.
2. PE2 is connected to both CN9 pin 14 (I/O) and CN10 pin 25 (QSPI_BK1_IO2). Only one pin must be used at one time.

Table 16. NUCLEO-F413ZH pin assignments

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
Left connectors						
CN8	1	NC	NC	-	-	ARDUINO® compatible
	3	IOREF	IOREF	-	3.3 V Ref	
	5	RESET	RESET	NRST	RESET	
	7	+3.3 V	+3.3 V	-	3.3 V input/output	
	9	+5 V	+5 V	-	5 V output	
	11	GND	GND	-	ground	
	13	GND	GND	-	ground	
	15	V_{IN}	V_{IN}	-	Power input	
	2	D43	SDMMC_D0	PC8	SDMMC/I2S_A	-
	4	D44	SDMMC_D1/ I2S_A_CKIN	PC9		
	6	D45	SDMMC_D2	PC10		
	8	D46	SDMMC_D3	PC11		
	10	D47	SDMMC_CK	PC12		
	12	D48	SDMMC_CMD	PD2		
	14	D49	I/O	PG2	I/O	
	16	D50	I/O	PG3		
CN9	1	A0	ADC	PA3	ADC1_IN3	ARDUINO® compatible
	3	A1	ADC	PC0	ADC1_IN10	
	5	A2	ADC	PC3	ADC1_IN13	

Table 16. NUCLEO-F413ZH pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN9	7	A3	ADC	PC1	ADC1_IN11	ARDUINO® compatible
	9	A4	ADC	PC4 or PB9(1)	ADC1_IN14 (PC4) or I2C1_SDA (PB9)	
	11	A5	ADC	PC5 or PB8(1)	ADC1_IN15 (PC5) or I2C1_SCL (PB8)	
	13	D72	NC	-	-	-
	15	D71	NC	-	-	
	17	D70	I2C_B_SMBA	PF2	I2C_2	
	19	D69	I2C_B_SCL	PF1		
	21	D68	I2C_B_SDA	PF0		
	23	GND	GND	-	ground	
	25	D67	CAN_RX	PD0	CAN_1	
	27	D66	CAN_TX	PD1		
	29	D65	I/O	PG0	I/O	
	2	D51	USART_B_SCLK	PD7	USART_2	
	4	D52	USART_B_RX	PD6		
	6	D53	USART_B_TX	PD5		
	8	D54	USART_B_RTS	PD4		
	10	D55	USART_B_CTS	PD3		
	12	GND	GND	-	ground	
	14	D56	SAI_A_MCLK	PE2(2)	SAI_1_A	
	16	D57	SAI_A_SD	PE4(3)		
	18	D58	SAI_A_SCK	PE5		
	20	D59	SAI_A_FS	PE6(3)		
	22	D60	SAI_B_SD	PE3	SAI_1_B	
	24	D61	SAI_B_SCK	PF8		
	26	D62	SAI_B_MCLK	PF7		
	28	D63	SAI_B_FS	PF9		
	30	D64	I/O	PG1	I/O	
Right Connectors						
CN7	1	D16	I2S_A_MCK	PC6	I2S_2	-
	3	D17	I2S_A_SD	PB15		
	5	D18	I2S_A_CK	PB13		
	7	D19	I2S_A_WS	PB12		
	9	D20	I2S_B_WS	PA15	I2S_3 / SPI3	
	11	D21	I2S_B_MCK	PC7		
	13	D22	I2S_B_SD/ SPI_B_MOSI	PB5		

Table 16. NUCLEO-F413ZH pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN7	15	D23	I2S_B_CK/ SPI_B_SCK	PB3	I2S_3 / SPI3	–
	17	D24	SPI_B_NSS	PA4		
	19	D25	SPI_B_MISO	PB4		
	2	D15	I2C_A_SCL	PB8	I2C1_SCL	ARDUINO® compatible
	4	D14	I2C_A_SDA	PB9	I2C1_SDA	
	6	AREF	AREF	-	AVDD/VREF+	
	8	GND	GND	-	ground	
	10	D13	SPI_A_SCK	PA5	SPI1_SCK	
	12	D12	SPI_A_MISO	PA6	SPI1_MISO	
	14	D11	SPI_A_MOSI/ TIM_E_PWM1	PA7(1) or PB5(1)	SPI1_MOSI/ TIM14_CH1	
	16	D10	SPI_A_CS/ TIM_B_PWM3	PD14	SPI1_CS/ TIM4_CH3	
	18	D9	TIMER_B_PWM2	PD15	TIM4_CH4	
	20	D8	I/O	PF12	-	
CN10	1	AVDD	AVDD	-	Analog VDD	-
	3	AGND	AGND	-	Analog ground	
	5	GND	GND	-	ground	
	7	A6	ADC_A_IN	PB1	ADC1_IN9	
	9	A7	ADC_B_IN	PC2	ADC1_IN12	
	11	A8	ADC_C_IN	PA2	ADC1_IN2	
	13	D26	QSPI_CS	PB6	QSPI_BK1	
	15	D27	QSPI_CLK	PB2	QSPI_CLK	
	17	GND	GND	-	ground	
	19	D28	QSPI_BK1_IO3	PD13	QSPI_BK1	
	21	D29	QSPI_BK1_IO1	PD12		
	23	D30	QSPI_BK1_IO0	PD11		
	25	D31	QSPI_BK1_IO2	PE2(2)		
	27	GND	GND	-	ground	
	29	D32	TIMER_C_PWM1	PA0	TIM2_CH1	
	31	D33	TIMER_D_PWM1	PB0	TIM3_CH3	
	33	D34	TIMER_B_ETR	PE0	TIM4_ETR	
	2	D7	I/O	PF13	-	ARDUINO® compatible
	4	D6	TIMER_A_PWM1	PE9	TIM1_CH1	
	6	D5	TIMER_A_PWM2	PE11	TIM1_CH2	
	8	D4	I/O	PF14	-	
	10	D3	TIMER_A_PWM3	PE13	TIM1_CH3	
	12	D2	I/O	PF15	-	
	14	D1	USART_A_TX	PG14	USART6	

Table 16. NUCLEO-F413ZH pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN10	16	D0	USART_A_RX	PG9		ARDUINO® compatible
	18	D42	TIMER_A_PWM1N	PE8	TIM1_CH1N	
	20	D41	TIMER_A_ETR	PE7	TIM1_ETR	
	22	GND	GND	-	ground	
	24	D40	TIMER_A_PWM2N	PE10	TIM1_CH2N	
	26	D39	TIMER_A_PWM3N	PE12	TIM1_CH3N	
	28	D38	I/O	PE14	I/O	
	30	D37	TIMER_A_BKIN1	PE15	TIM1_BKIN1	
	32	D36	TIMER_C_PWM2	PB10	TIM2_CH3	
	34	D35	TIMER_C_PWM3	PB11	TIM2_CH4	

1. For more details refer to *Table 12: Solder bridges*.
2. PE2 is connected to both CN9 pin14 (SAI_A_MCLK) and CN10 pin25 (QSPI_BK1_IO2). Only one connector pin can be used at one time.
3. Limitation: SAI_A_SD (PE4) is swapped with SAI_A_FS (PE6). These two pins on CN10 of NUCLEO-F413ZH are not compatible with other STM32 Nucleo-144 boards.

Table 17. NUCLEO-F429ZI and NUCLEO-F439ZI pin assignments

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
Left connectors						
CN8	1	NC	NC	-	-	ARDUINO® support
	3	IOREF	IOREF		3.3 V Ref	
	5	RESET	RESET	NRST	RESET	
	7	+3.3 V	+3.3 V	-	3.3 V input/output	
	9	+5 V	+5 V		5 V output	
	11	GND	GND		ground	
	13	GND	GND			
	15	V_{IN}	V_{IN}		Power input	
	2	D43	SDMMC_D0	PC8	SDMMC/I2S_A	-
	4	D44	SDMMC_D1/ I2S_A_CKIN	PC9	I/O	
	6	D45	SDMMC_D2	PC10		
	8	D46	SDMMC_D3	PC11		
	10	D47	SDMMC_CK	PC12		
	12	D48	SDMMC_CMD	PD2		
	14	D49	I/O	PG2		
	16	D50	I/O	PG3		
CN9	1	A0	ADC	PA3	ADC123_IN3	ARDUINO® support
	3	A1	ADC	PC0	ADC123_IN10	
	5	A2	ADC	PC3	ADC123_IN13	
	7	A3	ADC	PF3	ADC3_IN9	
	9	A4	ADC	PF5 or PB9(1)	ADC3_IN15 (PF5) or I2C1_SDA (PB9)	
	11	A5	ADC	PF10 or PB8(1)	ADC3_IN8 (PF10) or I2C1_SCL (PB8)	
	13	D72	NC	-	-	-
	15	D71	I/O	PA7(2)	I/O	
	17	D70	I2C_B_SMBA	PF2	I2C_2	
	19	D69	I2C_B_SCL	PF1		

Table 17. NUCLEO-F429ZI and NUCLEO-F439ZI pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN9	21	D68	I2C_B_SDA	PF0	I2C_2	-
	23	GND	GND	-	ground	
	25	D67	CAN_RX	PD0	CAN_1	
	27	D66	CAN_TX	PD1		
	29	D65	I/O	PG0	I/O	
	2	D51	USART_B_SCLK	PD7	USART_2	
	4	D52	USART_B_RX	PD6		
	6	D53	USART_B_TX	PD5		
	8	D54	USART_B_RTS	PD4		
	10	D55	USART_B_CTS	PD3		
	12	GND	GND	-	ground	
	14	D56	SAI_A_MCLK	PE2(3)	SAI_1_A	
	16	D57	SAI_A_FS	PE4		
	18	D58	SAI_A_SCK	PE5		
	20	D59	SAI_A_SD	PE6		
	22	D60	SAI_B_SD	PE3	SAI_1_B	
	24	D61	SAI_B_SCK	PF8		
	26	D62	SAI_B_MCLK	PF7		
	28	D63	SAI_B_FS	PF9		
	30	D64	I/O	PG1	I/O	
Right Connectors						
CN7	1	D16	I2S_A_MCK	PC6	I2S_2	-
	3	D17	I2S_A_SD	PB15		
	5	D18	I2S_A_CK	PB13(4)		
	7	D19	I2S_A_WS	PB12		
	9	D20	I2S_B_WS	PA15	I2S_3 / SPI3	
	11	D21	I2S_B_MCK	PC7		
	13	D22	I2S_B_SD/ SPI_B_MOSI	PB5		
	15	D23	I2S_B_CK/ SPI_B_SCK	PB3		
	17	D24	SPI_B_NSS	PA4		

Table 17. NUCLEO-F429ZI and NUCLEO-F439ZI pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN7	19	D25	SPI_B_MISO	PB4	I2S_3 / SPI3	-
	2	D15	I2C_A_SCL	PB8	I2C1_SCL	ARDUINO® support
	4	D14	I2C_A_SDA	PB9	I2C1_SDA	
	6	AREF	AREF	-	AVDD/VREF+	
	8	GND	GND		ground	
	10	D13	SPI_A_SCK	PA5	SPI1_SCK	
	12	D12	SPI_A_MISO	PA6	SPI1_MISO	
	14	D11	SPI_A_MOSI/ TIM_E_PWM1	PA7(1)(2) or PB5(1)	SPI1_MOSI/ TIM14_CH1	
	16	D10	SPI_A_CS/ TIM_B_PWM3	PD14	SPI1_CS/ TIM4_CH3	
	18	D9	TIMER_B_PWM2	PD15	TIM4_CH4	
	20	D8	I/O	PF12	-	
CN10	1	AVDD	AVDD	-	Analog VDD	-
	3	AGND	AGND		Analog ground	
	5	GND	GND		ground	
	7	A6	ADC_A_IN	PB1	ADC12_IN9	
	9	A7	ADC_B_IN	PC2	ADC123_IN12	
	11	A8	ADC_C_IN	PF4	ADC3_IN14	
	13	D26	I/O	PB6	I/O	
	15	D27	I/O	PB2		
	17	GND	GND	-	ground	
	19	D28	I/O	PD13	I/O	
	21	D29	I/O	PD12		
	23	D30	I/O	PD11		
	25	D31	I/O	PE2(3)		
	27	GND	GND	-	ground	
	29	D32	TIMER_C_PWM1	PA0	TIM2_CH1	
	31	D33	TIMER_D_PWM1	PB0	TIM3_CH3	
	33	D34	TIMER_B_ETR	PE0	TIM4_ETR	
	2	D7	I/O	PF13	-	ARDUINO® support

Table 17. NUCLEO-F429ZI and NUCLEO-F439ZI pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN10	4	D6	TIMER_A_PWM1	PE9	TIM1_CH1	ARDUINO® support
	6	D5	TIMER_A_PWM2	PE11	TIM1_CH2	
	8	D4	I/O	PF14	-	
	10	D3	TIMER_A_PWM3	PE13	TIM1_CH3	
	12	D2	I/O	PF15	-	
	14	D1	USART_A_TX	PG14	USART6	
	16	D0	USART_A_RX	PG9		
	18	D42	TIMER_A_PWM1N	PE8	TIM1_CH1N	-
	20	D41	TIMER_A_ETR	PE7	TIM1_ETR	
	22	GND	GND	-	ground	
	24	D40	TIMER_A_PWM2N	PE10	TIM1_CH2N	
	26	D39	TIMER_A_PWM3N	PE12	TIM1_CH3N	
	28	D38	I/O	PE14	I/O	
	30	D37	TIMER_A_BKIN1	PE15	TIM1_BKIN1	
	32	D36	TIMER_C_PWM2	PB10	TIM2_CH3	
	34	D35	TIMER_C_PWM3	PB11	TIM2_CH4	

1. For more details refer to *Table 12: Solder bridges*.
2. PA7 is used as D11 and connected to CN7 pin 14 by default. If JP6 is ON, it is also connected to both Ethernet PHY as RMII_DV and CN9 pin 15. In this case only one function of the Ethernet or D11 must be used.
3. PE2 is connected to both CN9 pin 14 (SAI_A_MCLK) and CN10 pin 25 (I/O). Only one function must be used at one time.
4. PB13 is used as I2S_A_CK and connected to CN7 pin 5 by default. If JP7 is ON, it is also connected to the Ethernet PHY as RMII_TXD1. In this case only one function of the Ethernet or I2S_A must be used.

Table 18. NUCLEO-F446ZE and NUCLEO-F722ZE pin assignments

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
Left connectors						
CN8	1	NC	NC	-	-	ARDUINO® support
	3	IOREF	IOREF	-	3.3 V Ref	
	5	RESET	RESET	NRST	RESET	
	7	+3.3 V	+3.3 V	-	3.3 V input/output	
	9	+5 V	+5 V	-	5 V output	
	11	GND	GND	-	ground	
	13	GND	GND	-	ground	
	15	V_{IN}	V_{IN}	-	Power input	
	2	D43	SDMMC_D0	PC8	SDMMC/I2S_A (SDMMC1 for NUCLEO-F7222ZE)	-
	4	D44	SDMMC_D1/ I2S_A_CKIN	PC9		
	6	D45	SDMMC_D2	PC10		
	8	D46	SDMMC_D3	PC11		
	10	D47	SDMMC_CK	PC12		
	12	D48	SDMMC_CMD	PD2		
	14	D49	I/O	PG2	I/O	
	16	D50	I/O	PG3		
CN9	1	A0	ADC	PA3	ADC123_IN3	ARDUINO® support
	3	A1	ADC	PC0	ADC123_IN10	
	5	A2	ADC	PC3	ADC123_IN13	
	7	A3	ADC	PF3	ADC3_IN9	
	9	A4	ADC	PF5 or PB9(1)	ADC3_IN15 (PF5) or I2C1_SDA (PB9)	
	11	A5	ADC	PF10 or PB8(1)	ADC3_IN8 (PF10) or I2C1_SCL (PB8)	
	13	D72	NC	-	-	-
	15	D71	NC	-	I2C_2	
	17	D70	I2C_B_SMBA	PF2		
	19	D69	I2C_B_SCL	PF1		
	21	D68	I2C_B_SDA	PF0		
	23	GND	GND	-	ground	
	25	D67	CAN_RX	PD0	CAN_1	

Table 18. NUCLEO-F446ZE and NUCLEO-F722ZE pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN9	27	D66	CAN_TX	PD1	CAN_1	-
	29	D65	I/O	PG0	I/O	
	2	D51	USART_B_SCLK	PD7	USART_2	
	4	D52	USART_B_RX	PD6		
	6	D53	USART_B_TX	PD5		
	8	D54	USART_B_RTS	PD4		
	10	D55	USART_B_CTS	PD3		
	12	GND	GND	-	ground	
	14	D56	SAI_A_MCLK	PE2(2)	SAI_1_A	
	16	D57	SAI_A_FS	PE4		
	18	D58	SAI_A_SCK	PE5		
	20	D59	SAI_A_SD	PE6		
	22	D60	SAI_B_SD	PE3	SAI_1_B	
	24	D61	SAI_B_SCK	PF8		
	26	D62	SAI_B_MCLK	PF7		
	28	D63	SAI_B_FS	PF9		
	30	D64	I/O	PG1	I/O	
Right Connectors						
CN7	1	D16	I2S_A_MCK	PC6	I2S_2	-
	3	D17	I2S_A_SD	PB15		
	3	D17	I2S_A_SD	PB15		
	5	D18	I2S_A_CK	PB13	I2S_3 / SPI3	
	7	D19	I2S_A_WS	PB12		
	9	D20	I2S_B_WS	PA15		
	11	D21	I2S_B_MCK	PC7		
	13	D22	I2S_B_SD/ SPI_B_MOSI	PB5		
	15	D23	I2S_B_CK/ SPI_B_SCK	PB3		
	17	D24	SPI_B_NSS	PA4		
	19	D25	SPI_B_MISO	PB4		
	2	D15	I2C_A_SCL	PB8	I2C1_SCL	ARDUINO® support
	4	D14	I2C_A_SDA	PB9	I2C1_SDA	
	6	AREF	AREF	-	AVDD/VREF+	
	8	GND	GND	-	ground	

Table 18. NUCLEO-F446ZE and NUCLEO-F722ZE pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN7	10	D13	SPI_A_SCK	PA5	SPI1_SCK	ARDUINO® support
	12	D12	SPI_A_MISO	PA6	SPI1_MISO	
	14	D11	SPI_A_MOSI/ TIM_E_PWM1	PA7(1) or PB5(1)	SPI1_MOSI/ TIM14_CH1	
	16	D10	SPI_A_CS/ TIM_B_PWM3	PD14	SPI1_CS/ TIM4_CH3	
	18	D9	TIMER_B_PWM2	PD15	TIM4_CH4	
	20	D8	I/O	PF12	-	
CN10	1	AVDD	AVDD	-	Analog VDD	-
	3	AGND	AGND	-	Analog ground	
	5	GND	GND	-	ground	
	7	A6	ADC_A_IN	PB1	ADC12_IN9	
	9	A7	ADC_B_IN	PC2	ADC123_IN12	
	11	A8	ADC_C_IN	PF4	ADC3_IN14	
	13	D26	QSPI_CS	PB6	QSPI_BK1	
	15	D27	QSPI_CLK	PB2	QSPI_CLK	
	17	GND	GND	-	ground	
	19	D28	QSPI_BK1_IO3	PD13	QSPI_BK1	
	21	D29	QSPI_BK1_IO1	PD12	-	
	23	D30	QSPI_BK1_IO0	PD11		
	25	D31	QSPI_BK1_IO2	PE2(2)		
	27	GND	GND	-	ground	
	29	D32	TIMER_C_PWM1	PA0	TIM2_CH1	
	31	D33	TIMER_D_PWM1	PB0	TIM3_CH3	
	33	D34	TIMER_B_ETR	PE0	TIM4_ETR	
	2	D7	I/O	PF13	-	ARDUINO® support
	4	D6	TIMER_A_PWM1	PE9	TIM1_CH1	
	6	D5	TIMER_A_PWM2	PE11	TIM1_CH2	
	8	D4	I/O	PF14	-	
	10	D3	TIMER_A_PWM3	PE13	TIM1_CH3	
	12	D2	I/O	PF15	-	
	14	D1	USART_A_TX	PG14	USART6	
	16	D0	USART_A_RX	PG9		

Table 18. NUCLEO-F446ZE and NUCLEO-F722ZE pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN10	18	D42	TIMER_A_PWM1N	PE8	TIM1_CH1N	-
	20	D41	TIMER_A_ETR	PE7	TIM1_ETR	
	22	GND	GND	-	ground	
	24	D40	TIMER_A_PWM2N	PE10	TIM1_CH2N	
	26	D39	TIMER_A_PWM3N	PE12	TIM1_CH3N	
	28	D38	I/O	PE14	I/O	
	30	D37	TIMER_A_BKIN1	PE15	TIM1_BKIN1	
	32	D36	TIMER_C_PWM2	PB10	TIM2_CH3	
	34	D35	TIMER_C_PWM3	PB11	TIM2_CH4	

1. For more details refer to *Table 12: Solder bridges*.
2. PE2 is connected to both CN9 pin 14 (SAI_A_MCLK) and CN10 pin 25 (QSPI_BK1_IO2). Only one function must be used at one time.

Table 19. NUCLEO-F746ZG, NUCLEO-F756ZG and NUCLEO-F767ZI pin assignments

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
Left connectors						
CN8	1	NC	NC	-	-	ARDUINO® support
	3	IOREF	IOREF		3.3 V Ref	
	5	RESET	RESET	NRST	RESET	
	7	+3.3 V	+3.3 V	-	3.3 V input/output	
	9	+5 V	+5 V		5 V output	
	11	GND	GND		ground	
	13	GND	GND		ground	
	15	V_{IN}	V_{IN}		Power input	
	2	D43	SDMMC_D0	PC8	SDMMC/I2S_A	-
	4	D44	SDMMC_D1/ I2S_A_CKIN	PC9		
	6	D45	SDMMC_D2	PC10		
	8	D46	SDMMC_D3	PC11		
	10	D47	SDMMC_CK	PC12		
	12	D48	SDMMC_CMD	PD2		
	14	D49	I/O	PG2	I/O	
	16	D50	I/O	PG3		
CN9	1	A0	ADC	PA3	ADC123_IN3	ARDUINO® support
	3	A1	ADC	PC0	ADC123_IN10	
	5	A2	ADC	PC3	ADC123_IN13	
	7	A3	ADC	PF3	ADC3_IN9	
	9	A4	ADC	PF5 or PB9(1)	ADC3_IN15 (PF5) or I2C1_SDA (PB9)	
	11	A5	ADC	PF10 or PB8(1)	ADC3_IN8 (PF10) or I2C1_SCL (PB8)	
	13	D72	NC	-	-	-
	15	D71	I/O	PA7(2)	I/O	
	17	D70	I2C_B_SMBA	PF2	I2C_2	
	19	D69	I2C_B_SCL	PF1		
	21	D68	I2C_B_SDA	PF0		
	23	GND	GND	-	ground	
	25	D67	CAN_RX	PD0	CAN_1	

Table 19. NUCLEO-F746ZG, NUCLEO-F756ZG and NUCLEO-F767ZI pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN9	27	D66	CAN_TX	PD1	CAN_1	-
	29	D65	I/O	PG0	I/O	
	2	D51	USART_B_SCLK	PD7	USART_2	
	4	D52	USART_B_RX	PD6		
	6	D53	USART_B_TX	PD5		
	8	D54	USART_B_RTS	PD4		
	10	D55	USART_B_CTS	PD3		
	12	GND	GND	-	ground	
	14	D56	SAI_A_MCLK	PE2(3)	SAI_1_A	
	16	D57	SAI_A_FS	PE4		
	18	D58	SAI_A_SCK	PE5		
	20	D59	SAI_A_SD	PE6		
	22	D60	SAI_B_SD	PE3	SAI_1_B	
	24	D61	SAI_B_SCK	PF8		
	26	D62	SAI_B_MCLK	PF7		
	28	D63	SAI_B_FS	PF9		
	30	D64	I/O	PG1	I/O	

Table 19. NUCLEO-F746ZG, NUCLEO-F756ZG and NUCLEO-F767ZI pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
Right Connectors						
CN7	1	D16	I2S_A_MCK	PC6	I2S_2	-
	3	D17	I2S_A_SD	PB15		
	5	D18	I2S_A_CK	PB13(4)		
	7	D19	I2S_A_WS	PB12		
	9	D20	I2S_B_WS	PA15	I2S_3 / SPI3	
	11	D21	I2S_B_MCK	PC7		
	13	D22	I2S_B_SD/ SPI_B_MOSI	PB5		
	15	D23	I2S_B_CK/ SPI_B_SCK	PB3		
	17	D24	SPI_B_NSS	PA4		
	19	D25	SPI_B_MISO	PB4		
	2	D15	I2C_A_SCL	PB8	I2C1_SCL	ARDUINO® support
	4	D14	I2C_A_SDA	PB9	I2C1_SDA	-
	6	AREF	AREF	-	AVDD/VREF+	
	8	GND	GND		ground	

Table 19. NUCLEO-F746ZG, NUCLEO-F756ZG and NUCLEO-F767ZI pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN7	10	D13	SPI_A_SCK	PA5	SPI1_SCK	-
	12	D12	SPI_A_MISO	PA6	SPI1_MISO	
	14	D11	SPI_A_MOSI/ TIM_E_PWM1	PA7(1)(2) or PB5(1)	SPI1_MOSI/ TIM14_CH1	
	16	D10	SPI_A_CS/ TIM_B_PWM3	PD14	SPI1_CS/ TIM4_CH3	
	18	D9	TIMER_B_PWM2	PD15	TIM4_CH4	
	20	D8	I/O	PF12	-	
CN10	1	AVDD	AVDD	-	Analog VDD	
	3	AGND	AGND	-	Analog ground	
	5	GND	GND	-	ground	
	7	A6	ADC_A_IN	PB1	ADC12_IN9	
	9	A7	ADC_B_IN	PC2	ADC123_IN12	
	11	A8	ADC_C_IN	PF4	ADC3_IN14	
	13	D26	QSPI_CS	PB6	QSPI_BK1	
	15	D27	QSPI_CLK	PB2	QSPI_CLK	
	17	GND	GND	-	ground	
	19	D28	QSPI_BK1_IO3	PD13	QSPI_BK1	
	21	D29	QSPI_BK1_IO1	PD12		
	23	D30	QSPI_BK1_IO0	PD11		
	25	D31	QSPI_BK1_IO2	PE2(3)		
	27	GND	GND	-	ground	
	29	D32	TIMER_C_PWM1	PA0	TIM2_CH1	
	31	D33	TIMER_D_PWM1	PB0	TIM3_CH3	
	33	D34	TIMER_B_ETR	PE0	TIM4_ETR	
	2	D7	I/O	PF13	-	ARDUINO® support
	4	D6	TIMER_A_PWM1	PE9	TIM1_CH1	
	6	D5	TIMER_A_PWM2	PE11	TIM1_CH2	
	8	D4	I/O	PF14	-	
	10	D3	TIMER_A_PWM3	PE13	TIM1_CH3	
	12	D2	I/O	PF15	-	
	14	D1	USART_A_TX	PG14	USART6	
	16	D0	USART_A_RX	PG9		
	18	D42	TIMER_A_PWM1N	PE8	TIM1_CH1N	-
	20	D41	TIMER_A_ETR	PE7	TIM1_ETR	

Table 19. NUCLEO-F746ZG, NUCLEO-F756ZG and NUCLEO-F767ZI pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN10	22	GND	GND	-	ground	-
	24	D40	TIMER_A_PWM2N	PE10	TIM1_CH2N	
	26	D39	TIMER_A_PWM3N	PE12	TIM1_CH3N	
	28	D38	I/O	PE14	I/O	
	30	D37	TIMER_A_BKIN1	PE15	TIM1_BKIN1	
	32	D36	TIMER_C_PWM2	PB10	TIM2_CH3	
	34	D35	TIMER_C_PWM3	PB11	TIM2_CH4	

1. For more details refer to *Table 12: Solder bridges*.
2. PA7 is used as D11 and connected to CN7 pin 14 by default, if JP6 is ON, it is also connected to both Ethernet PHY as RMII_DV and CN9 pin 15. In this case only one function of the Ethernet or D11 must be used.
3. PE2 is connected to both CN9 pin 14 (SAI_A_MCLK) and CN10 pin 25 (QSPI_BK1_IO2). Only one function must be used at one time.
4. PB13 is used as I2S_A_CK and connected to CN7 pin 5 by default, if JP7 is ON, it is also connected to Ethernet PHY as RMII_TXD1. In this case only one function of the Ethernet or I2S_A must be used.

Table 20. NUCLEO-H743ZI pin assignments

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
Left connectors						
CN8	1	NC	NC	-	-	ARDUINO® compatible-
	3	IOREF	IOREF	-	3.3 V Ref	
	5	RESET	RESET	NRST	RESET	
	7	+3.3 V	+3.3 V	-	3.3 V input/output	
	9	+5 V	+5 V	-	5 V output	
	11	GND	GND	-	Ground	
	13	GND	GND	-	Ground	
	15	V_{IN}	V_{IN}	-	Power input	
	2	D43	SDMMC1_D0	PC8	SDMMC/I2S_A	-
	4	D44	SDMMC1_D1/ I2S_A_CKIN	PC9		
	6	D45	SDMMC1_D2	PC10		
	8	D46	SDMMC1_D3	PC11		
	10	D47	SDMMC1_CK	PC12		
	12	D48	SDMMC1_CMD	PD2		
	14	D49	I/O	PG2	I/O	
	16	D50	I/O	PG3		
CN9	1	A0	ADC	PA3	ADC12_IN15	ARDUINO® compatible
	3	A1	ADC	PC0	ADC123_IN10	
	5	A2	ADC	PC3	ADC123_IN13	
	7	A3	ADC	PF3	ADC3_IN5	
	9	A4	ADC	PF5 or PB9(1)	ADC3_IN4 (PF5) or I2C1_SDA (PB9)	
	11	A5	ADC	PF10 or PB8(1)	ADC3_IN6 (PF10) or I2C1_SCL (PB8)	
	13	D72	NC	-	-	-
	15	D71	I/O	PA7(2)	I/O	
	17	D70	I2C_B_SMBA	PF2	I2C_2	
	19	D69	I2C_B_SCL	PF1		
	21	D68	I2C_B_SDA	PF0		
	23	GND	GND	-	Ground	

Table 20. NUCLEO-H743ZI pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN9	25	D67	CAN_RX	PD0	CAN_1	-
	27	D66	CAN_TX	PD1		
	29	D65	I/O	PG0	I/O	
	2	D51	USART_B_SCLK	PD7	USART_2	
	4	D52	USART_B_RX	PD6		
	6	D53	USART_B_TX	PD5		
	8	D54	USART_B_RTS	PD4		
	10	D55	USART_B_CTS	PD3		
	12	GND	GND	-	Ground	
	14	D56	SAI_A_MCLK	PE2(3)	SAI_1_A	
	16	D57	SAI_A_FS	PE4		
	18	D58	SAI_A_SCK	PE5		
	20	D59	SAI_A_SD	PE6		
	22	D60	SAI_B_SD	PE3	SAI_1_B	
	24	D61	SAI_B_SCK	PF8		
	26	D62	SAI_B_MCLK	PF7		
	28	D63	SAI_B_FS	PF9		
	30	D64	I/O	PG1	I/O	
Right Connectors						
CN7	1	D16	I2S_A_MCK	PC6	I2S_2	-
	3	D17	I2S_A_SD	PB15		
	5	D18	I2S_A_CK	PB13(4)		
	7	D19	I2S_A_WS	PB12		
	9	D20	I2S_B_WS	PA15	I2S_3 / SPI3	
	11	D21	I2S_B_MCK	PC7		
	13	D22	I2S_B_SD/ SPI_B_MOSI	PB5		
	15	D23	I2S_B_CK/ SPI_B_SCK	PB3		
	17	D24	SPI_B_NSS	PA4		
	19	D25	SPI_B_MISO	PB4		
	2	D15	I2C_A_SCL	PB8	I2C1_SCL	ARDUINO® compatible
	4	D14	I2C_A_SDA	PB9	I2C1_SDA	
	6	AREF	AREF	-	AVDD/VREF+	
	8	GND	GND	-	Ground	

Table 20. NUCLEO-H743ZI pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN7	10	D13	SPI_A_SCK	PA5	SPI1_SCK	ARDUINO® compatible
	12	D12	SPI_A_MISO	PA6	SPI1_MISO	
	14	D11	SPI_A_MOSI/ TIM_E_PWM1	PA7(1) (2)or PB5(1)	SPI1_MOSI/ TIM14_CH1	
	16	D10	SPI_A_CS/ TIM_B_PWM3	PD14	SPI1_CS/ TIM4_CH3	
	18	D9	TIMER_B_PWM2	PD15	TIM4_CH4	
	20	D8	I/O	PF12	-	
CN10	1	AVDD	AVDD	-	Analog VDD	-
	3	AGND	AGND	-	Analog Ground	
	5	GND	GND	-	Ground	
	7	A6	ADC_A_IN	PB1	ADC12_IN5	
	9	A7	ADC_B_IN	PC2	ADC123_IN12	
	11	A8	ADC_C_IN	PF4	ADC3_IN9	
	13	D26	QSPI_CS	PB6	QSPI_BK1	
	15	D27	QSPI_CLK	PB2	QSPI_CLK	
	17	GND	GND	-	Ground	
	19	D28	QSPI_BK1_IO3	PD13	QSPI_BK1	
	21	D29	QSPI_BK1_IO1	PD12		
	23	D30	QSPI_BK1_IO0	PD11		
	25	D31	QSPI_BK1_IO2	PE2(3)		
	27	GND	GND	-	Ground	
	29	D32	TIMER_C_PWM1	PA0	TIM2_CH1	
	31	D33	TIMER_D_PWM1	PB0	TIM3_CH3	
	33	D34	TIMER_B_ETR	PE0	TIM4_ETR	
	2	D7	I/O	PF13	-	ARDUINO® compatible
	4	D6	TIMER_A_PWM1	PE9	TIM1_CH1	
	6	D5	TIMER_A_PWM2	PE11	TIM1_CH2	
	8	D4	I/O	PF14	-	
	10	D3	TIMER_A_PWM3	PE13	TIM1_CH3	
	12	D2	I/O	PF15	-	
	14	D1	USART_A_TX	PG14	USART6	
	16	D0	USART_A_RX	PG9		
	18	D42	TIMER_A_PWM1N	PE8	TIM1_CH1N	-
	20	D41	TIMER_A_ETR	PE7	TIM1_ETR	

Table 20. NUCLEO-H743ZI pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN10	22	GND	GND	-	Ground	–
	24	D40	TIMER_A_PWM2N	PE10	TIM1_CH2N	
	26	D39	TIMER_A_PWM3N	PE12	TIM1_CH3N	
	28	D38	I/O	PE14	I/O	
	30	D37	TIMER_A_BKIN1	PE15	TIM1_BKIN1	
	32	D36	TIMER_C_PWM2	PB10	TIM2_CH3	
	34	D35	TIMER_C_PWM3	PB11	TIM2_CH4	

1. For more details refer to *Table 12: Solder bridges*.
2. PA7 is used as D11 and connected to CN7 pin14 by default, if JP6 is ON, it is also connected to both Ethernet PHY as RMII_DV and CN9 pin15. In this case only one function of Ethernet or D11 could be used.
3. PE2 is connected to both CN9 pin14 (SAI_A_MCLK) and CN10 pin 25 (QSPI_BK1_IO2). Only one function can be used at one time.
4. PB13 is used as I2S_A_CK and connected to CN7 pin 5 by default. If JP7 is ON, it is also connected to the Ethernet PHY as RMII_TXD1. In this case only one function of the Ethernet or I2S_A must be used.

6.15 ST morpho connector

The ST morpho connector consists in male pin header footprints CN11 and CN12 (OFF by default). They are used to connect the STM32 Nucleo-144 board to an extension board or a prototype/wrapping board placed on top of the STM32 Nucleo-144 board. All signals and power pins of the STM32 are available on the ST morpho connector. This connector can also be probed by an oscilloscope, logical analyzer or voltmeter.

Table 21 and *Table 22* show the pin assignments of each STM32 on the ST morpho connector.

Table 21. ST morpho connector for NUCLEO-F207ZG, NUCLEO-F412ZG, NUCLEO-F413ZH, NUCLEO-F429ZI, NUCLEO-F439ZI, NUCLEO-F446ZE, NUCLEO-F722ZE, NUCLEO-F746ZG, NUCLEO-F756ZG, NUCLEO-F767ZI and NUCLEO-H743ZI

CN11 odd pins		CN11 even pins		CN12 odd pins		CN12 even pins	
Pin	Pin name	Pin	Pin name	Pin	Pin name	Pin	Pin name
1	PC10	2	PC11	1	PC9	2	PC8
3	PC12	4	PD2	3	PB8	4	PC6
5	VDD	6	E5V	5	PB9	6	PC5
7	BOOT0(1)	8	GND	7	AVDD	8	U5V(2)
9	PF6	10	-	9	GND	10	PD8
11	PF7	12	IOREF	11	PA5	12	PA12
13	PA13(3)	14	RESET	13	PA6	14	PA11
15	PA14(3)	16	+3.3 V	15	PA7	16	PB12
17	PA15	18	+5 V	17	PB6	18	PB11
19	GND	20	GND	19	PC7	20	GND
21	PB7	22	GND	21	PA9	22	PB2
23	PC13	24	V_{IN}	23	PA8	24	PB1
25	PC14	26	-	25	PB10	26	PB15
27	PC15	28	PA0	27	PB4	28	PB14
29	PH0	30	PA1	29	PB5	30	PB13
31	PH1	32	PA4	31	PB3	32	AGND
33	V_{BAT}	34	PB0	33	PA10	34	PC4
35	PC2	36	PC1	35	PA2	36	PF5
37	PC3	38	PC0	37	PA3	38	PF4
39	PD4	40	PD3	39	GND	40	PE8
41	PD5	42	PG2	41	PD13	42	PF10
43	PD6	44	PG3	43	PD12	44	PE7
45	PD7	46	PE2	45	PD11	46	PD14
47	PE3	48	PE4	47	PE10	48	PD15
49	GND	50	PE5	49	PE12	50	PF14
51	PF1	52	PF2	51	PE14	52	PE9
53	PF0	54	PF8	53	PE15	54	GND
55	PD1	56	PF9	55	PE13	56	PE11
57	PD0	58	PG1	57	PF13	58	PF3
59	PG0	60	GND	59	PF12	60	PF15
61	PE1	62	PE6	61	PG14	62	PF11

Table 21. ST morpho connector for NUCLEO-F207ZG, NUCLEO-F412ZG, NUCLEO-F413ZH, NUCLEO-F429ZI, NUCLEO-F439ZI, NUCLEO-F446ZE, NUCLEO-F722ZE, NUCLEO-F746ZG, NUCLEO-F756ZG, NUCLEO-F767ZI and NUCLEO-H743ZI (continued)

CN11 odd pins		CN11 even pins		CN12 odd pins		CN12 even pins	
Pin	Pin name	Pin	Pin name	Pin	Pin name	Pin	Pin name
63	PG9	64	PG15	63	GND	64	PE0
65	PG12	66	PG10	65	PD10	66	PG8
67	-	68	PG13	67	PG7	68	PG5
69	PD9	70	PG11	69	PG4	70	PG6

1. Default state of BOOT0 is 0. It can be set to 1 when a jumper is plugged on the pins 5-7 of CN11.
2. U5V is the 5 V power coming from the ST-LINKV2-1 USB connector that rises before and it rises before the +5 V rising on the board.
3. PA13 and PA14 are shared with SWD signals connected to ST-LINK/V2-1. If ST-LINK part is not cut, it is not recommended to use them as I/O pins.

Table 22. ST morpho connector for NUCLEO-F303ZE

CN11 odd pins		CN11 even pins		CN12 odd pins		CN12 even pins	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	PC10	2	PC11	1	PC9	2	PC8
3	PC12	4	PD2	3	PB8	4	PC6
5	VDD	6	E5V	5	PB9	6	PC5
7	BOOT0(1)	8	GND	7	AVDD	8	U5V(2)
9	PF6	10	-	9	GND	10	PD8
11	PF7	12	IOREF	11	PA5	12	PA12
13	PA13(3)	14	RESET	13	PA6	14	PA11
15	PA14(3)	16	+3.3 V	15	PA7	16	PB12
17	PA15	18	+5 V	17	PB6	18	PB11
19	GND	20	GND	19	PC7	20	GND
21	PB7	22	GND	21	PA9	22	PB2
23	PC13	24	V_{IN}	23	PA8	24	PB1
25	PC14	26	-	25	PB10	26	PB15
27	PC15	28	PA0	27	PB4	28	PB14
29	PF0	30	PA1	29	PB5	30	PB13
31	PF1	32	PA4	31	PB3	32	AGND
33	V_{BAT}	34	PB0	33	PA10	34	PC4
35	PC2	36	PC1	35	PA2	36	PF5
37	PC3	38	PC0	37	PA3	38	PF4
39	PD4	40	PD3	39	GND	40	PE8

Table 22. ST morpho connector for NUCLEO-F303ZE (continued)

CN11 odd pins		CN11 even pins		CN12 odd pins		CN12 even pins	
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**
41	PD5	42	PG2	41	PD13	42	PF10
43	PD6	44	PG3	43	PD12	44	PE7
45	PD7	46	PE2	45	PD11	46	PD14
47	PE3	48	PE4	47	PE10	48	PD15
49	GND	50	PE5	49	PE12	50	PF14
51	PH1	52	PF2	51	PE14	52	PE9
53	PH0	54	PF8	53	PE15	54	GND
55	PD1	56	PF9	55	PE13	56	PE11
57	PD0	58	PG1	57	PF13	58	PF3
59	PG0	60	GND	59	PF12	60	PF15
61	PE1	62	PE6	61	PG14	62	PF11
63	PG9	64	PG15	63	GND	64	PE0
65	PG12	66	PG10	65	PD10	66	PG8
67	PH2	68	PG13	67	PG7	68	PG5
69	PD9	70	PG11	69	PG4	70	PG6

1. Default state of BOOT0 is 0. It can be set to 1 when a jumper is plugged on the pins 5-7 of CN11.
2. U5V is the 5 V power coming from the ST-LINK/V2-1 USB connector that rises before and it rises before the +5 V rising on the board.
3. PA13 and PA14 are shared with the SWD signals connected to ST-LINK/V2-1. If ST-LINK part is not cut, it is not recommended to use them as I/O pins.

7 Nucleo-144 (MB1137) information

7.1 Product marking

The stickers located on the top or bottom side of all PCBs provide product information:

- First sticker: product order code and product identification, generally placed on the main board featuring the target device.
  Example:

  Product order code
  Product identification

- Second sticker: board reference with revision and serial number, available on each PCB.
  Example:

  MBxxxx-Variant-yzz
  syywwxxxxx

On the first sticker, the first line provides the product order code, and the second line the product identification.

On the second sticker, the first line has the following format: *“MBxxxx-Variant-yzz”*, where *“MBxxxx”* is the board reference, *“Variant”* (optional) identifies the mounting variant when several exist, *"y"* is the PCB revision and *"zz"* is the assembly revision, for example B01. The second line shows the board serial number used for traceability.

Parts marked as *"ES"* or *"E"* are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

"E" or *"ES"* marking examples of location:

- On the targeted STM32 that is soldered on the board (for an illustration of STM32 marking, refer to the STM32 datasheet *Package information* paragraph at the *www.st.com* website).
- Next to the evaluation tool ordering part number that is stuck or silk-screen printed on the board.

Some boards feature a specific STM32 device version, which allows the operation of any bundled commercial stack/library available. This STM32 device shows a *"U"* marking option at the end of the standard part number and is not available for sales.

To use the same commercial stack in their applications, the developers might need to purchase a part number specific to this stack/library. The price of those part numbers includes the stack/library royalties.

7.2 Nucleo-144 (MB1137) product history

Table 23. Product history

Order code	Product identification	Product details	Product change description	Product limitations
NUCLEO-F207ZG	NUCLEOF207ZG/	MCU: – STM32F207ZGT6 revision “2” or “3”	Initial revision	No limitation
		MCU errata sheet: – *STM32F205/207xx and STM32F215/217xx device limitations* (ES0005)		
		Board: – MB1137-F207ZG-B01 (main board)		
	NUF207ZG$AU1	MCU: – STM32F207ZGT6 revision “2” or “3”	Packaging: plastic blister replaced by a carton box	No limitation
		MCU errata sheet: – *STM32F205/207xx and STM32F215/217xx device limitations* (ES0005)		
		Board: – MB1137-F207ZG-B01 (main board)		

Table 23. Product history (continued)

Order code	Product identification	Product details	Product change description	Product limitations
NUCLEO-F303ZE	NUCLEOF303ZE/	MCU: – STM32F303ZET6 revision “Y”	Initial revision	No limitation
		MCU errata sheet: – *STM32F303xD STM32F303xE Rev Y device limitations* (ES0261)		
		Board: – MB1137-F303ZE-B01 (main board)		
	NUF303ZE$AU1	MCU: – STM32F303ZET6 revision “Y”	Packaging: plastic blister replaced by a carton box	No limitation
		MCU errata sheet: – *STM32F303xD STM32F303xE Rev Y device limitations* (ES0261)		
		Board: – MB1137-F303ZE-B01 (main board)		
NUCLEO-F412ZG	NUCLEOF412ZG/	MCU: – STM32F412ZGT6 revision “C”	Initial revision	No limitation
		MCU errata sheet: – *STM32F412xE/xG device limitations* (ES0305)		
		Board: – MB1137-F412ZG-B01 (main board)		
	NUF412ZG$AU1	MCU: – STM32F412ZGT6 revision “C”	Packaging: plastic blister replaced by a carton box	No limitation
		MCU errata sheet: – *STM32F412xE/xG device limitations* (ES0305)		
		Board: – MB1137-F412ZG-B01 (main board)		

Table 23. Product history (continued)

Order code	Product identification	Product details	Product change description	Product limitations
NUCLEO-F413ZH	NUCLEOF413ZH/	MCU: – STM32F413ZHT6 revision “A”	Initial revision	No limitation
		MCU errata sheet: – *STM32F413xG/xH and STM32F423xH device limitations* (ES0372)		
		Board: – MB1137-F413ZH-B01 (main board)		
	NUF413ZH$AU1	MCU: – STM32F413ZHT6 revision “A”	Packaging: plastic blister replaced by a carton box	No limitation
		MCU errata sheet: – *STM32F413xG/xH and STM32F423xH device limitations* (ES0372)		
		Board: – MB1137-F413ZH-B01 (main board)		
NUCLEO-F429ZI	NUCLEOF429ZI/	MCU: – STM32F429ZIT6 revision “3”	Initial revision	No limitation
		MCU errata sheet: – *STM32F427/437 and STM32F429/439 line limitations (ES0206)*		
		Board: – MB1137-F429ZI-B01 (main board)		
	NUF429ZI$AU1	MCU: – STM32F429ZIT6 revision “3”	Packaging: plastic blister replaced by a carton box	No limitation
		MCU errata sheet: – *STM32F427/437 and STM32F429/439 line limitations (ES0206)*		
		Board: – MB1137-F429ZI-B01 (main board)		

Table 23. Product history (continued)

Order code	Product identification	Product details	Product change description	Product limitations
NUCLEO-F439ZI	NUF439ZI$AU1	MCU: – STM32F439ZIT6 revision “4” or “B”	Initial revision	No limitation
		MCU errata sheet: – *STM32F427/437 and STM32F429/439 line limitations (ES0206)*		
		Board: – MB1137-F439ZI-B01 (main board)		
	NUF439ZI$AU2	MCU: – STM32F439ZIT6 revision “4” or “B”	Packaging: plastic blister replaced by a carton box	No limitation
		MCU errata sheet: – *STM32F427/437 and STM32F429/439 line limitations (ES0206)*		
		Board: – MB1137-F439ZI-B01 (main board)		
NUCLEO-F446ZE	NUCLEOF446ZE/	MCU: – STM32F446ZET6 revision “A”	Initial revision	No limitation
		MCU errata sheet: – *STM32F446xC/xE device limitations* (ES0298)		
		Board: – MB1137-F446ZE-B01 (main board)		
	NUF446ZE$AU1	MCU: – STM32F446ZET6 revision “A”	Packaging: plastic blister replaced by a carton box	No limitation
		MCU errata sheet: – *STM32F446xC/xE device limitations* (ES0298)		
		Board: – MB1137-F446ZE-B01 (main board)		

Table 23. Product history (continued)

Order code	Product identification	Product details	Product change description	Product limitations
NUCLEO-F722ZE	NUCLEOF722ZE/	MCU: – STM32F722ZET6 revision “A”	Initial revision	No limitation
		MCU errata sheet: – *STM32F72xxx and STM32F73xxx device limitations* (ES0360)		
		Board: – MB1137-F722ZE-B01 (main board)		
	NUF722ZE$AU1	MCU: – STM32F722ZET6 revision “A”	Packaging: plastic blister replaced by a carton box	No limitation
		MCU errata sheet: – *STM32F72xxx and STM32F73xxx device limitations* (ES0360)		
		Board: – MB1137-F722ZE-B01 (main board)		
NUCLEO-F746ZG	NUCLEOF746ZG/	MCU: – STM32F746ZGT6 revision “Z”	Initial revision	No limitation
		MCU errata sheet: – *STM32F74xxx and STM32F75xxx device limitations* (ES0290)		
		Board: – MB1137-F746ZG-B01 (main board)		
	NUF746ZG$AU1	MCU: – STM32F746ZGT6 revision “Z”	Packaging: plastic blister replaced by a carton box	No limitation
		MCU errata sheet: – *STM32F74xxx and STM32F75xxx device limitations* (ES0290)		
		Board: – MB1137-F746ZG-B01 (main board)		

Table 23. Product history (continued)

Order code	Product identification	Product details	Product change description	Product limitations
NUCLEO-F756ZG	NUF756ZG$AU1	MCU: – STM32F756ZGT6 revision “Z”	Initial revision	No limitation
		MCU errata sheet: – *STM32F74xxx and STM32F75xxx device limitations* (ES0290)		
		Board: – MB1137-F756ZG-B01 (main board)		
	NUF756ZG$AU2	MCU: – STM32F756ZGT6 revision “Z”	Packaging: plastic blister replaced by a carton box	No limitation
		MCU errata sheet: – *STM32F74xxx and STM32F75xxx device limitations* (ES0290)		
		Board: – MB1137-F756ZG-B01 (main board)		
NUCLEO-F767ZI	NUCLEOF767ZI/	MCU: – STM32F767ZIT6 revision “Z” or “1”	Initial revision	No limitation
		MCU errata sheet: – *STM32F76xxx and STM32F77xxx device errata* (ES0334)		
		Board: – MB1137-F767ZI-B01 (main board)		
	NUF767ZI$AU1	MCU: – STM32F767ZIT6 revision “Z” or “1”	Packaging: plastic blister replaced by a carton box	No limitation
		MCU errata sheet: – *STM32F76xxx and STM32F77xxx device errata* (ES0334)		
		Board: – MB1137-F767ZI-B01 (main board)		

Table 23. Product history (continued)

Order code	Product identification	Product details	Product change description	Product limitations
NUCLEO-H743ZI[1]	NUCLEOH743ZI/	MCU: – STM32H743ZIT6 revision “Y”	Initial revision	No limitation
		MCU errata sheet: – *STM32H742xI/G and STM32H743xI/G device limitations* (ES0392)		
		Board: – MB1137-H743ZI-B01 (main board)		

1. This product is replaced by NUCLEO-H743ZI2 with board reference MB1364.

7.3 Board revision history

Table 24. Board revision history

Board reference	Board variant and revision	Board change description	Board limitations
MB1137 (main board)	F207ZG-B01 F303ZE-B01 F412ZG-B01 F413ZH-B01 F429ZI-B01 F439ZI-B01 F446ZE-B01 F722ZE-B01 F746ZG-B01 F756ZG-B01 F767ZI-B01 H743ZI-B01	Initial revision	No limitation

8 Federal Communications Commission (FCC) and ISED Canada Compliance Statements

8.1 FCC Compliance Statement

8.1.1 Part 15.19

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

8.1.2 Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

8.1.3 Part 15.105

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Note: Use only shielded cables.

Responsible party (in the USA)

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8.2 ISED Compliance Statement

Compliance Statement

ISED Canada ICES-003 Compliance Label: *CAN ICES-3 (B) / NMB-3 (B)*.

Déclaration de conformité

Étiquette de conformité à la NMB-003 d'ISDE Canada : *CAN ICES-3 (B) / NMB-3 (B)*.

Revision history

Table 25. Document revision history

Date	Revision	Changes
21-Dec-2015	1	Initial version.
20-May-2016	2	Updated *Introduction*, *Section 6.13: Extension connectors*, *Section 6.14: ST Zio connectors* to add NUCLEO-F767ZI.
08-Jul-2016	3	Updated *Introduction*, *Section 3: Ordering information*, *Section 6.11: Ethernet*, *Section 6.12: Solder bridges*, *Section 6.13: Extension connectors*, *Section 6.14: ST Zio connectors*, *Section 6.15: ST morpho connector* to add NUCLEO-F412ZG.
28-Nov-2016	4	Updated *Introduction*, *Section 3: Ordering information*, *Section 6.11: Ethernet*, *Section 6.12: Solder bridges*, *Section 6.13: Extension connectors*, *Section 6.14: ST Zio connectors*, *Section 6.15: ST morpho connector* to add NUCLEO-F413ZH.
19-Jan-2017	5	Updated *Introduction*, *Section 3: Ordering information*, *Section 6.11: Ethernet*, *Section 6.12: Solder bridges*, *Section 6.13: Extension connectors*, *Section 6.14: ST Zio connectors*, *Section 6.15: ST morpho connector* to add NUCLEO-F722ZE.
14-Apr-2017	6	Updated *Introduction*, *Section 3: Ordering information* and *Table 12: Solder bridges* to add NUCLEO-H743ZI.
15-Dec-2017	7	Expanded document scope to the NUCLEO-F439ZI and NUCLEO-F756ZG products: – Updated *Introduction*, *Features*, *Product marking* and *Ordering information* – Updated *Figure 11*, *Table 13*, *Table 17* and *Table 21*
28-Aug-2020	8	Removed *Electrical schematics*. Added *Appendix B: CE conformity* and updated *Appendix A: Federal Communications Commission (FCC) and ISED Canada Compliance Statements*. Updated *Figure 3.* Reorganized *Section 6.13: Extension connectors*. Revised the beginning of the document: – Updated the document title – Updated *Section 1: Features*, *Section 2: Ordering information*, *Section 3.2: Development toolchains* and *Section 3.3: Demonstration software* – Added *Section 2.1: Product marking* and *Section 2.2: Codification*

Table 25. Document revision history (continued)

Date	Revision	Changes
11-Jan-2023	9	Updated the USART3 default configuration in *Table 9*. Added *Chapter 7: Nucleo-144 (MB1137) information*. Updated *Chapter 1: Features*, *Chapter 2: Ordering information*, and *Chapter 3: Development environment*. Updated *Section 8.2: ISED Compliance Statement*. Updated *Figure 4*, *Figure 5*, *Figure 9*, and *Figure 10*. Removed the references to Arm® Mbed™.
4-Aug-2023	10	Updated the USART3 description in *Section 6.9: USART communication* and in *Table 9*. Removed *Chapter 9: CE conformity*.