[System Name] Documentation

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Version 1.0
Last Updated 2025/03/10
Date Created 2024/12/10

Date	Changes Made	Made By
2024/12/04	Create initial document	Matthew Ricci

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Introduction

Document descriptions at $10{,}000$ ft [1] and $30{,}000$ ft [1], [2], [3].

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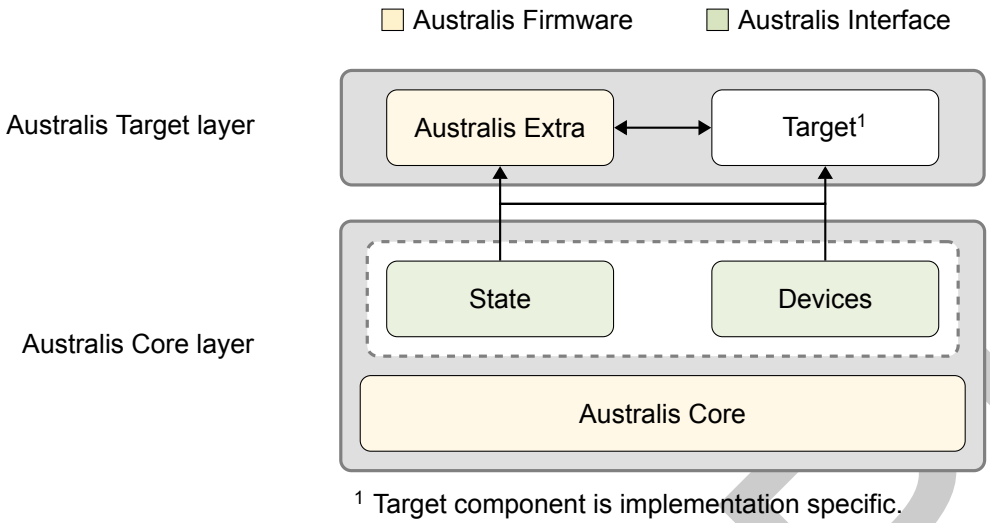
2 Firmware Architecture



[1] Target component is implementation specific.

Figure 2.1: Australis Firmware system architecture

3 Memory and Bus Architecture

3.1 System Architecture

In STM32F405xx/07xx and STM32F415xx/17xx, the main system consists of 32-bit multilayer AHB bus matrix that interconnects:

- Eight masters:
  - Cortex®-M4 with FPU core I-bus, D-bus, and S-bus
  - DMA1 memory bus
  - DMA2 memory bus
  - DMA2 peripheral bus
  - Ethernet DMA bus
  - USB OTG HS DMA bus
- Seven slaves:
  - Internal flash memory ICode bus
  - Internal flash memory DCode bus
  - Main internal SRAM1 (112 KB)
  - Auxiliary internal SRAM2 (16 KB)
  - AHB1 peripherals including AHB to APB bridges and APB peripherals
  - AHB2 peripherals
  - FSMC

The bus matrix provides access from a master to a slave, enabling concurrent access and efficient operation even when several high-speed peripherals work simultaneously. The 64-Kbyte CCM (core coupled memory) data RAM is not part of the bus matrix and can be accessed only through the CPU. This architecture is shown in Figure 1.

EXAMPLE DOCUMENT
(totally not stolen from RM0090)

4 References

[1] M. Ricci, *How to tame an avionics engineer.* Enguhneering-Blog. Accessed: Dec. 10, 2024. [Online]. Available: https://silkroad.market.

[2] B. Alexander, *How not to land a rocket.* RIP Omega. Accessed: Aug. 24, 2024. [Online]. Available: https://whitecliffs.gg.

[3] H. Begg, “Leaving team chats,” *Journal of Absolute Bozos*, vol. 10, no. 4, pp. 1111–2222, Jan. 1970.

5 Appendix

Appendix A: Appendix Item

Appendix B: Appendix Item