

# EXAMPLE

## Introduction

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## Related Documents

Available from <https://www.github.com/repo-name>:

- Technical reference
- Hardware manual
- Design review
- Test criteria and evaluation
- The Holy Bible

## Acknowledgements

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# Example System Documentation

## Document Title

2025 Example Organisation

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## Important Terms

<b>Australis</b>	Student developed flight computer hardware platform for high power rockets.
<b>Australis Core</b>	An internal component providing the base API and critical logic; stylised core.
<b>Australis Extra</b>	An internal component providing modular systems that may be optionally included to extend core functionality; stylised extra.
<b>Australis Firmware</b>	Flight computer firmware system for high power rockets; designed for, but not limited to, deployment on Australis targets.
<b>Component</b>	A collection of semantically related code groups and files within the Australis Firmware ecosystem.
<b>Device</b>	A hardware element external to the controller that provides additional functionality via a connected interface.
<b>Driver</b>	Software implementation of a device or peripheral interface.
<b>Peripheral</b>	A hardware element internal to the controller that provides important extensions to the feature set of its core processor.
<b>Submodule</b>	An isolated system packaged within extra that extends system functionality to target source code. Submodules may only depend on the core API.
<b>Target</b>	A hardware platform on which the Australis Firmware operates.

## Abbreviations

<b>A3<sup>1</sup></b>	Aurora 3
<b>API</b>	Application Programming Interface
<b>AV2</b>	Australis Version 2

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<sup>1</sup>Also refers to version 1 of the Australis flight computer hardware.

# 1 Section

**Note** This is a dark box

## 1.1 Subsection

**Note** Footnotes do not work correctly in most environments, like here. To get around this we use \footnotemark to define the location of the footnote marker, and \footnotetext{text} later outside of the environment.<sup>2</sup>

Footnotes can be created normally with \footnote{text} when called outside of an environment.<sup>3</sup>

Citations are created in IEEE style with Biblatex.[1]

### 1.1.1 Subsubsection

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Table 1: Left aligned table with no row colouring

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Table 2: Center aligned table with row colouring

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Table 3: Full headwidth table extending past margins

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<sup>2</sup>This is a footnote.

<sup>3</sup>This is another footnote.

## 2 Memory and Bus Architecture

### 2.1 System Architecture

In STM32F405xx/07xx and STM32F415xx/17xx, the main system consists of 32-bit multilayer AHB bus matrix that interconnects:

- Eight masters:
  - Cortex®-M4 with FPU core I-bus, D-bus, and S-bus
  - DMA1 memory bus
  - DMA2 memory bus
  - DMA2 peripheral bus
  - Ethernet DMA bus
  - USB OTG HS DMA bus
- Seven slaves:
  - Internal flash memory ICode bus
  - Internal flash memory DCode bus
  - Main internal SRAM1 (112 KB)
  - Auxiliary internal SRAM2 (16 KB)
  - AHB1 peripherals including AHB to APB bridges and APB peripherals
  - AHB2 peripherals
  - FSMC

The bus matrix provides access from a master to a slave, enabling concurrent access and efficient operation even when several high-speed peripherals work simultaneously. The 64-Kbyte CCM (core coupled memory) data RAM is not part of the bus matrix and can be accessed only through the CPU. This architecture is shown in Figure 1.

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(totally not stolen from RM0090)

### 3 References

- [1] B. Alexander, *How not to land a rocket*. RIP Omega. Accessed: Aug. 24, 2024. [Online]. Available: <https://whitecliffs.gg>.

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## 4 Document History

date	changes made	made by
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2025/03/11	create initial document	jim bob
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# Appendix

## Appendix A: Appendix Item

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