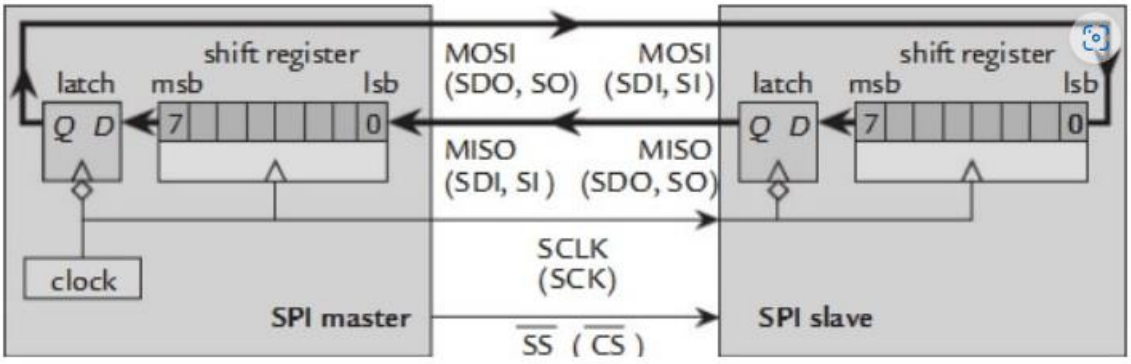
SPI Communication Introduction

- It is a serial and synchronous interface. The synchronous interface means it requires a clock signal to transfer and receive data and the clock signal is synchronized between both master and slave.
- Unlike UART communication which is asynchronous.
- The clock signal controls when data is to be sent to the slave and when it should be ready to read.
- The only master device can control the clock and provide a clock signal to all slave devices.
- Data can not be transferred without a clock signal.
- Both master and slave can exchange data with each other.
- No address decoding is done.

SPI Connection Between Two Devices

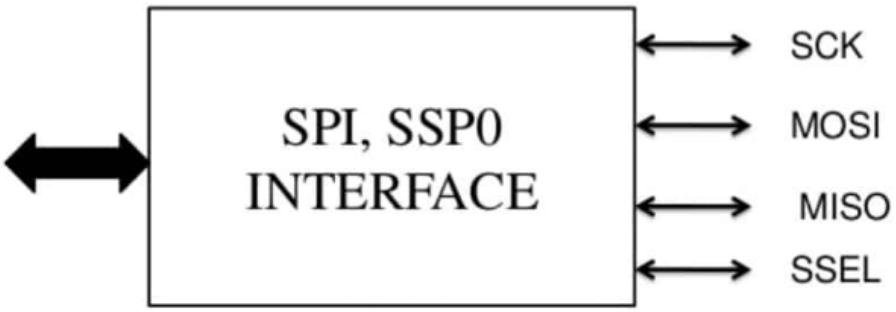
It is Full duplex synchronous communication. Both Master and Slave can exchange data with each other on the rising and falling edge of the clock signal. The Block diagram below shows interfacing with one Master and one Slave. SPI interface consists of either three or four signals. But in this article, We will see a general 4 wire interface.



- SCLK or SCK pin : This signal provides a clock to Slaves and only Master can control clock signal. Note that this pin remains in idle state .i.e. inactive or tri-state when no operation is carried out.
- SS or CS : This is known as a chip select or Slave select pin. This line selects the slave to which Master want to transfer data.
- MOSI : It is a unidirectional pin. This stands for Master output and Slave input pin. As its name suggests, this line used to send data from master to slave.
- MISO: This is known as Master input and a Slave output. This line is used to send data from the slave to the Master.

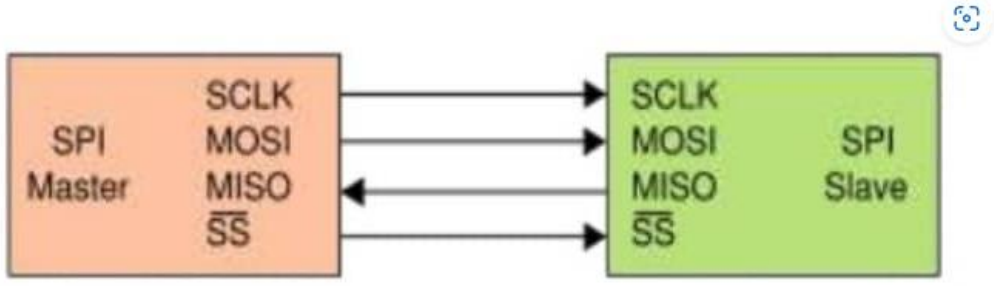
In short, in this communication protocol, devices exchange data in master/slave mode. The master device is mainly responsible for the initiation of the data frame. The master device also selects the slave device to which data need to be transferred. Chip select line is usually used to identify or select a particular slave device.

Whenever a master device read to transmit data to slave or want to receive data from the slave, the master does so by activating the clock signal. Every master device sends data on the MOSI line and receives data through another line that is MISO.



SPI Working Operation

As we mentioned earlier, the SPI bus consists of a single master and multiple slave devices. But SPI bus can be used in different configurations like a single master and a single slave as shown in the diagram below.

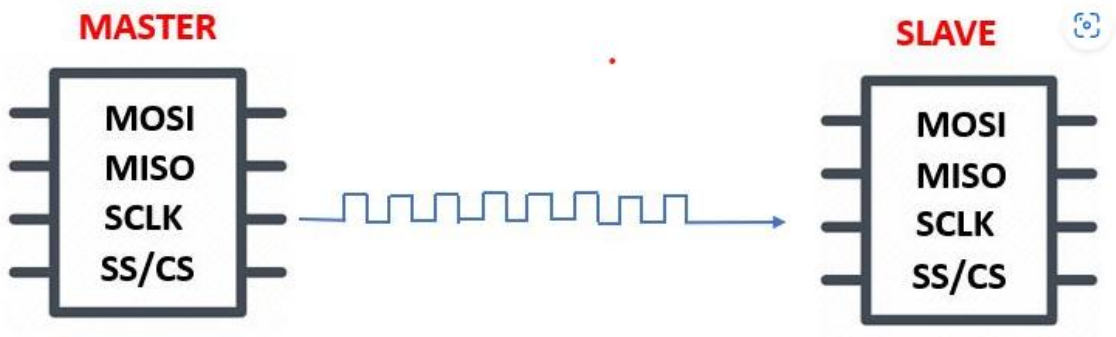


For some SPI devices, if only a single slave is used, a chip select pin can be connected with active low signal, but this feature varies for different SPI based devices.

SPI Protocol Data Transmission

Now let us discuss the transmission of data through SPI protocol in a step by step manner.

- Firstly, the master outputs the clock signal as you can view in the figure below:



- Now to activate the slave, the master switches the SS/CS pin to a low voltage state.

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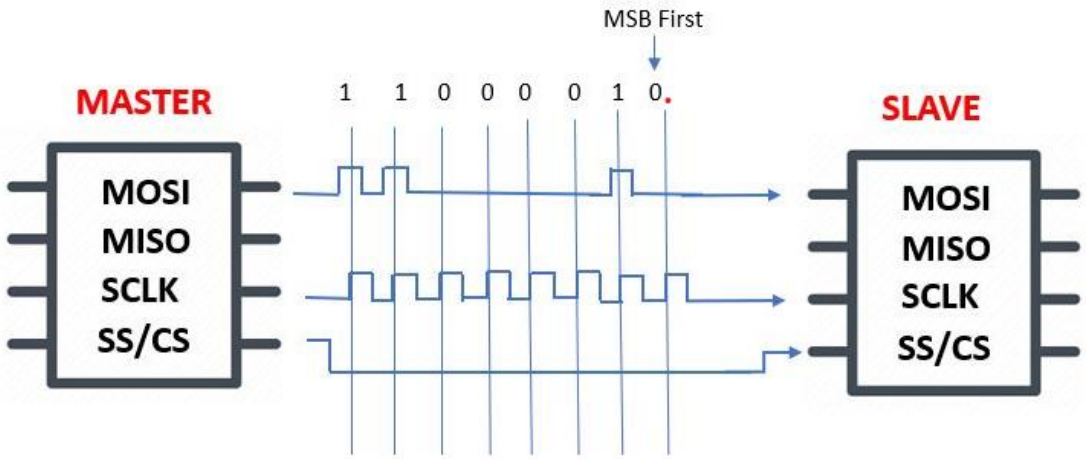
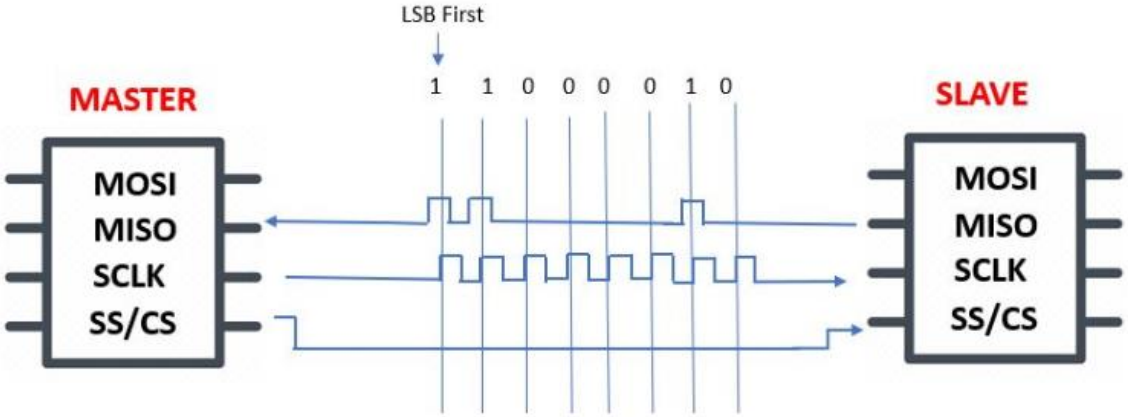
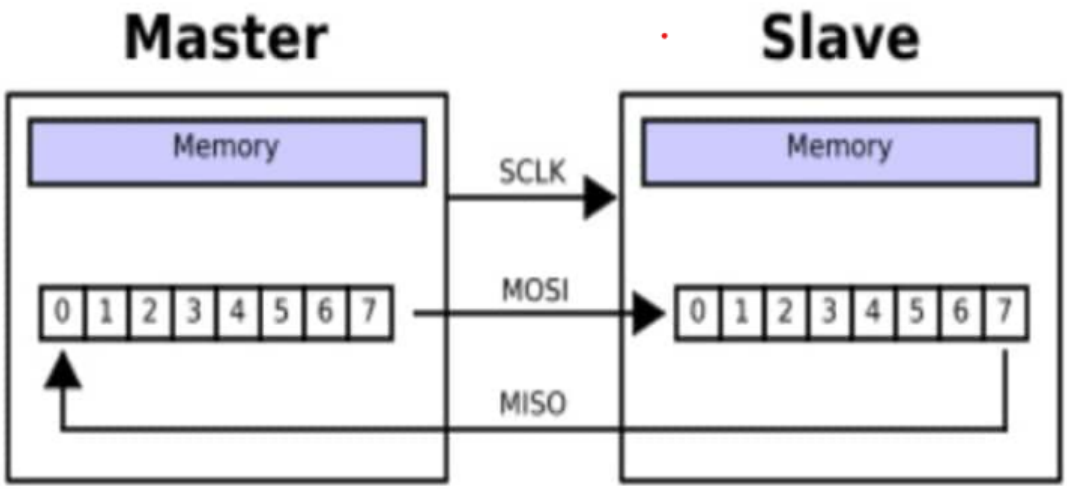


- If the master requires a response, the slave sends data to the master one bit at a time via the MISO line. The master reads the bits as they are received.



SPI Module Internal Structure

The data transmission between a master and a slave device generally consists of two shift registers as shown in the diagram here. These shift registers are usually of 8 bits size for both the master and the slave device.



- It usually forms a circular buffer consists of two shift registers.
- In order to transfer data, a master device initiates the active high clock signal to a slave device and the frequency of the clock signal is less than or equal to the operating frequency of a slave device.
- The frequency range is between 1-70MHz for maximum SPI devices.
- After that, the master device makes the chip select signal active high to select a particular slave device to which it wants to transfer data commands.
- Each SPI clock transfers data in full-duplex mode.
- After selecting a slave, the master sends a start bit to the slave device over a MOSI line and slave reads this bit with the same line.
- The master device share date with the slave device using the shift register. After reading data, the slave device store the data from the shift register into memory and similar operation happen when the master wants to receive data from the slave.