→Testbench:-

```
1.  module tb;
2.
3.
4.  integer i = 0;
5.
6.  reg clk = 0,sys_rst = 0;
7.  reg [15:0] din = 0;
8.  wire [15:0] dout;
9.
10.
11. top dut(clk, sys_rst, din, dout);
12.
13. always #5 clk = ~clk;
14.
15. initial begin
16. sys_rst = 1'b1;
17. repeat(5) @(posedge clk);
18. sys_rst = 1'b0;
19. #800;
20. $stop;
21. end
22.
23. endmodule
```