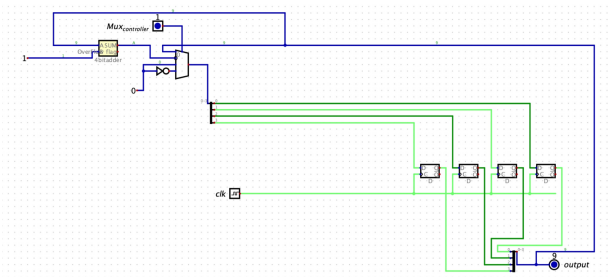
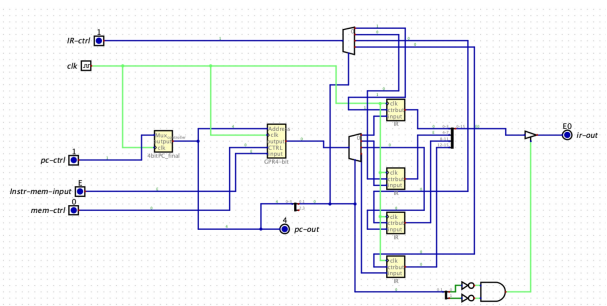
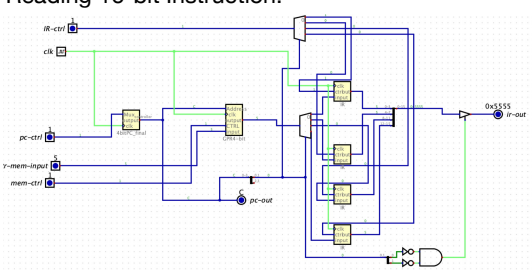
2.1 Program Counter
Incrementing



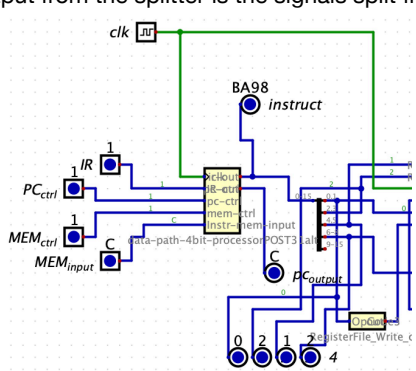
2.2 Instruction Memory
Writing and then reading a instruction from the memory using the PC



2.3 Extended Instruction Register
Reading 16-bit Instruction.



2.4 Instruction Decoder
Output from the splitter is the signals split from the instruction.



2.5 Register File and ALU
Testing arithmetic

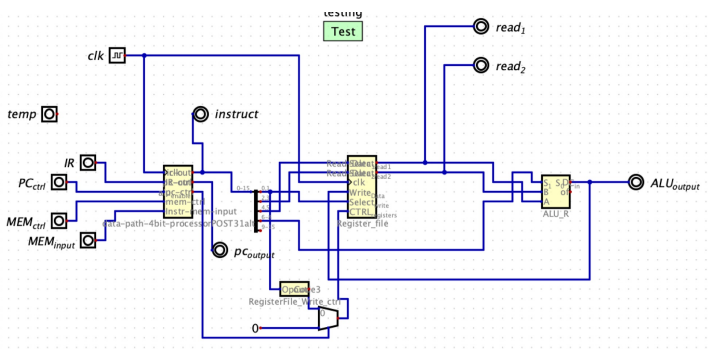
	clk	IR	MEM_ctrl	MEM_input	PC_ctrl	pc_output	instruct	read_1	read_2	ALU_output
L2	0	0	1	0	1	1	Z	0	0	1
L3	0	0	1	4	1	2	Z	0	0	1
L4	0	0	1	1	1	3	Z	0	0	1
L5	0	0	1	0	1	4	0	1	1	2
L7	0	0	1	0	1	5	Z	0	0	0
L8	0	0	1	4	1	6	Z	0	0	0
L9	0	0	1	1	1	7	Z	0	0	0
L10	0	0	1	0	1	8	0	0	0	0

3.Integrating the complete processor.
Processor Test Simulation

testing passed

	clk	IR	MEM_ctrl	MEM_input	PC_ctrl	pc_output	instruct	read_1	read_2	ALU_output
L2	0	0	1	0	1	1	Z	0	0	0
L3	0	0	1	4	1	2	Z	0	0	0
L4	0	0	1	1	1	3	Z	0	0	0
L5	0	0	1	0	1	4	0	0	0	0
L7	0	0	1	0	1	5	Z	0	0	0
L8	0	0	1	4	1	6	Z	0	0	0
L9	0	0	1	1	1	7	Z	0	0	0
L10	0	0	1	0	1	8	0	0	0	0
L12	0	0	1	1	1	9	Z	0	0	0
L13	0	0	1	5	1	A	Z	0	0	0
L14	0	0	1	1	1	B	Z	0	0	0
L15	0	0	1	0	1	C	0	0	0	0
L17	0	0	1	6	1	D	Z	0	0	1
L18	0	0	1	0	1	E	Z	0	0	1
L19	0	0	1	0	1	F	Z	0	0	1
L20	0	0	1	0	1	0	0	0	0	0
L23	0	1	0	2	1	1	Z	1	1	2
L24	0	1	0	2	1	2	Z	2	2	2
L25	0	1	0	2	1	3	Z	2	2	2
L26	0	1	0	2	1	4	0x140	2	2	3
L27	0	1	0	2	1	5	Z	0	0	E
L28	0	1	0	2	1	6	Z	0	0	E
L29	0	1	0	2	1	7	Z	0	0	E
L30	0	1	0	2	1	8	0x140	2	2	3
L31	0	1	0	2	1	9	Z	0	1	E
L32	0	1	0	2	1	A	Z	2	2	1
L33	0	1	0	2	1	B	Z	1	2	E
L34	0	1	0	1	1	C	0x151	0	2	1
L35	0	1	0	1	1	D	Z	0	0	1
L36	0	1	0	1	1	E	Z	0	0	1
L37	0	1	0	1	1	F	Z	0	0	1
L38	0	1	0	1	1	0	6	2	0	2
L39	0	1	0	1	1	1	Z	0	1	E

Full Processor Image



4.
The PC is a simple program counter that is fed into the GPR Address input, determining which address is written to. The GPR output is then fed into the input of 4 instruction registers with the PC determining which IR is written to. Then the output of each IR is fed into a merger which merges them into one 16 bit integer, this is later reffered to as the instruction.
The output of the IR's merged is then led into another splitter which decodes the signal produced by using the 2 least significant bits as the selector for which register is written to in the register file. The next 4 bits are used to determine which registers are read, and the next two bits are used as the arithmetic operand for the ALU. the ALU uses the two read values from the register file to complete an operation.

Github Link: https://github.com/RMm32/assignment3
Group Members
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