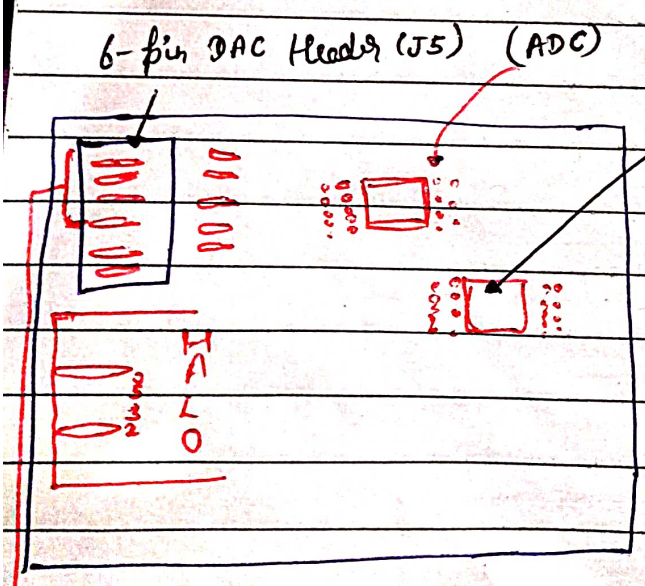
# Serial Peripheral Interface (SPI) Date .....

## DAC (Digital to Analog) Interfacing with FPGA (SPARTAN 3E)

- Hardware used :-
- Digital to Analog converter (DAC) :
  Onboard SPI controlled DAC, LTC2624
  ↳ it supports SPI protocol.

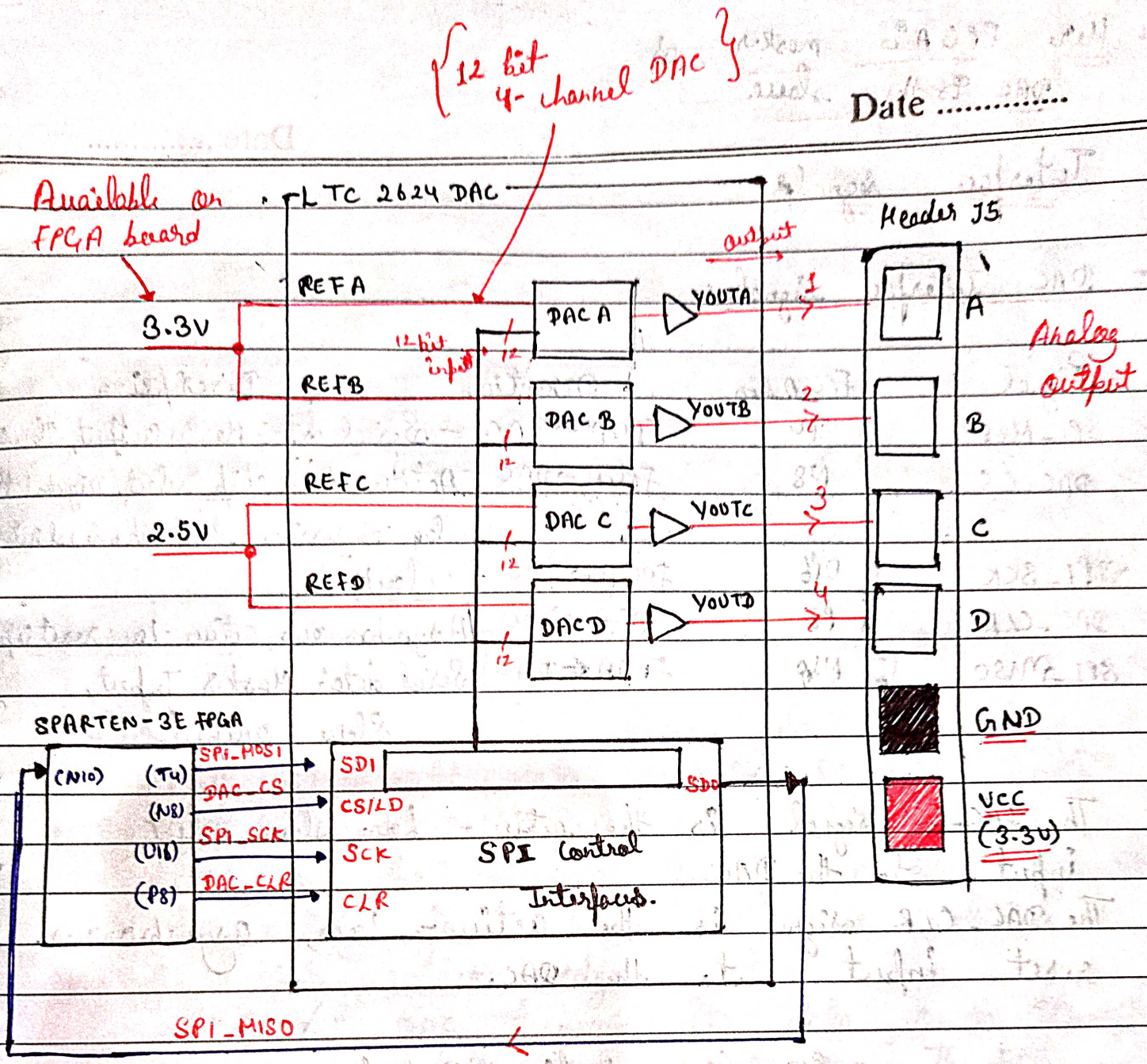
- The Spartan-3E FPGA Starter Kit board includes an SPI-compatible, four-channel, serial Digital to Analog Converter (DAC). The DAC device is Linear Technology LTC2624 quad DAC with 12-bit unsigned resolution. The four output from the DAC appear on the J5 header, which uses the Digilent 6-pin Peripheral Module, format. The DAC and the header are located immediately above the Ethernet RJ-45 connector, as shown in figure :-




→ from here we get different Analog voltage at different pin.
DACKA, DACKB, DACKC, DACKD

Spiral

Date .....




- Digital - to - Analog Connection Schematics.

- **Master** :- which initiates the communication process as which can produce the clock signal.
  Here, all the signal is controlled by SPARTAN-3E FPGA. So the FPGA chip is the master.

- **Slave**:- It respond to the controlling signal of the master.
  Here, DAC is the slave.

- Here FPGA is master & DAC is the slave.

Date .....

- Interface signals:

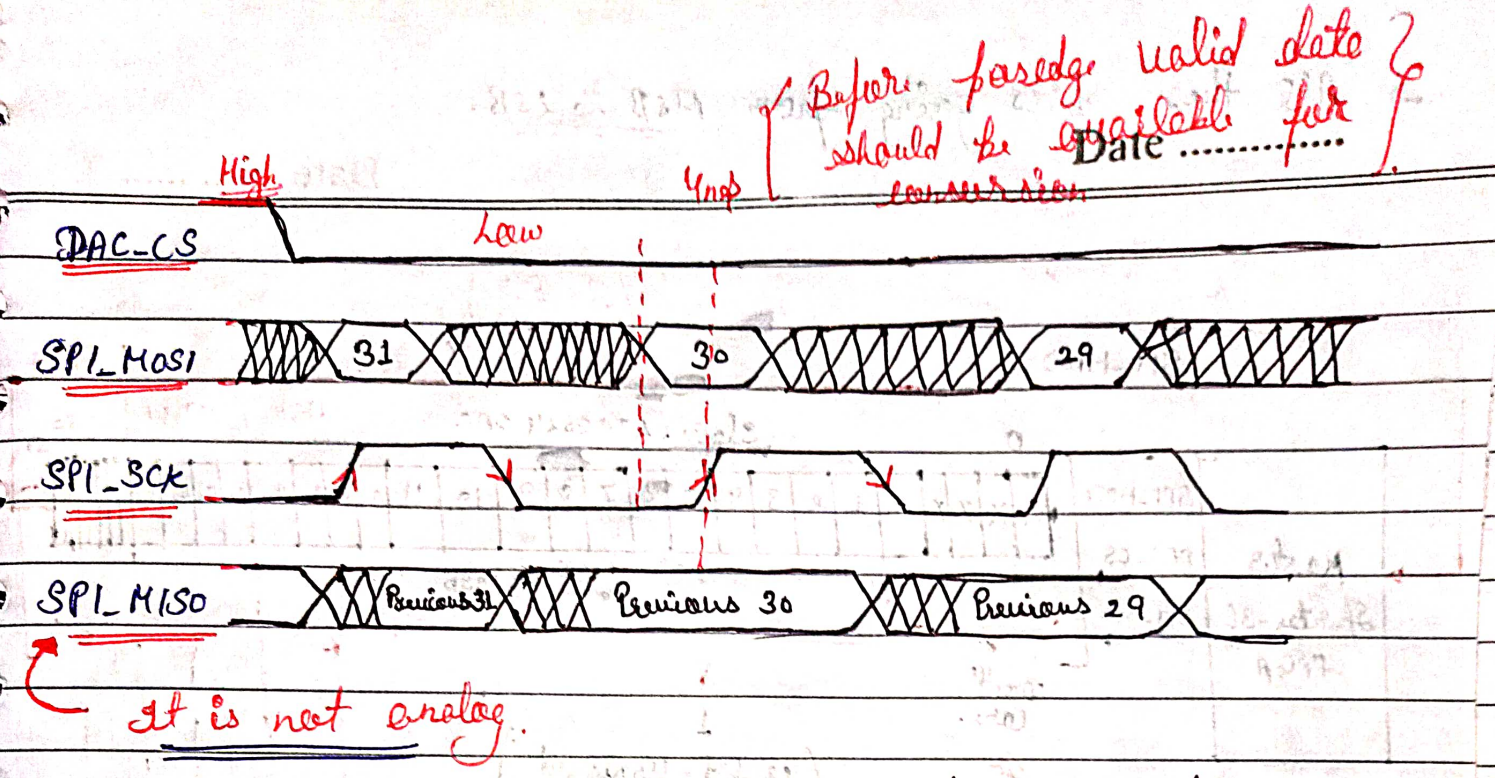
- DAC Interface signals:-

| Signal | FPGA Pin | Direction | Description |
|---|---|---|---|
| SPI_MOSI | T4 | FPGA → DAC | Serial data: Master output, Slave input |
| DAC_CS | N8 | FPGA → DAC | Active-Low chip select, Digital to analog conversion start when signal returns High |
| SPI_SCK | U16 | FPGA → DAC | Clock |
| DAC_CLR | P8 | FPGA → DAC | Asynchronous, active-Low reset input |
| SPI_MISO | N10 | FPGA ← DAC | Serial data: Master Input, Slave output |

- The DAC_CS signal is the active-Low slave select input to the DAC.
- The DAC_CLR signal is the active-Low, asynchronous, reset input to the DAC.

- SPI Communication Details.

* This figure shows a detailed example of SPI bus timing. Each bit is transmitted or received relative to the SPI_SCK clock signal. The bus is fully static and supports clocks rate up to the maximum of 50 MHz. However, check all timing parameters using the LTC2624 data sheet if operating at or close to the maximum ~~speed~~ speed.

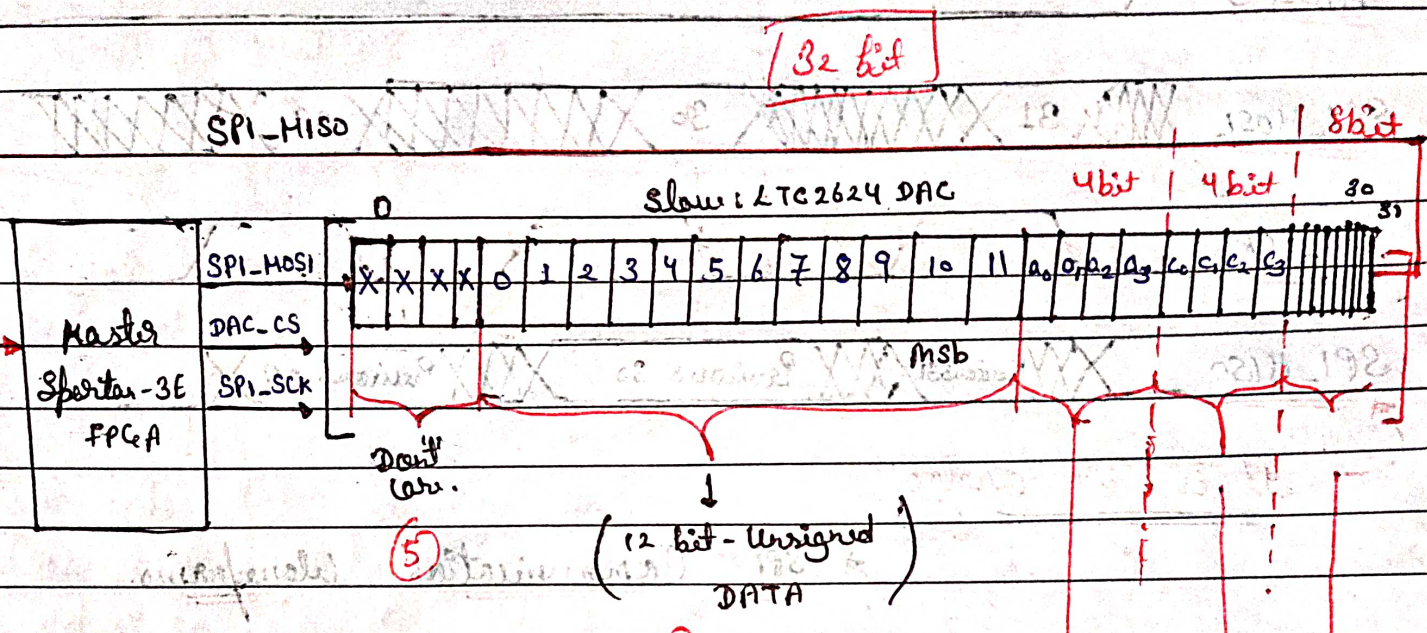



## ✱ SPI Communication Waveforms.

1. After driving the DAC_CS slave select signal low, the FPGA transmits data on the SPI_MOSI signal, MSB first. The LTC2624 captures input data (SPI_MOSI) on the rising edge of SPI_SCK; the data must be valid for at least 4 ns relative to the rising clock edge.
2. The LTC2624 DAC transmits its data on the SPI_MISO signal on the falling edge of SPI_SCK. The FPGA captures this data on the next rising ~~SPI_CLK~~ SPI_SCK edge. The FPGA must read the first SPI_MISO value on the first rising SPI_SCK edge after DAC_CS goes low. Otherwise, bit 31 is missed.
3. After transmitting all 32 data bits, the FPGA completes the SPI bus transaction by returning the DAC_CS slave select signal high. The high-going edge starts the actual digital-to-analog conversion process within the DAC.

→ All these bits going from MSB to LSB.

Date .....




- Total bits:-

8 + 4 + 4 + 12 + 4

= 32 bit

| $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ | Address |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | DAC A |
| 0 | 0 | 0 | 1 | DAC B |
| 0 | 0 | 1 | 0 | DAC C |
| 0 | 0 | 1 | 1 | DAC D |
| 1 | 1 | 1 | 1 | All |

- SPI Communication protocol to LTC2624 DAC.

→ How 32 bit is sent →

- The FPGA first sends eight dummy or "don't care" bits, followed by a 4-bit command. The most commonly used command with the board is COMMAND[3:0] = '0011' which immediately updates the selected DAC output with the specified data value. Following the command, the FPGA selects one or all the DAC outputs channels. via a 4-bit address field. Following the address field, the FPGA sends a 12-bit unsigned data value that the DAC converts to an analog value on

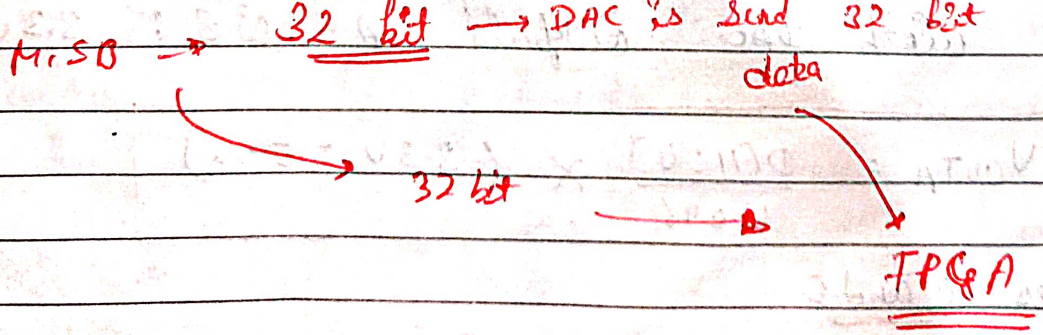
Date .....

the selected output(s). Finally, four additional dummy or don't care bits fad the 32-bit command word.

* Communication Protocol.

- Figure - shows the communications protocol required to interface with the LTC2624 DAC. The DAC supports both a 24-bit and 32-bit protocol. The 32-bit protocol is shown.

Important :- Inside the D/A converter, the SPI interface is formed by a 32-bit shift register. Each 32-bit command word consists of a command, an address, followed by data value. As a new command enters the DAC, the previous 32-bit command word is echoed back to the master. The response from the DAC can be ignored although it is a useful to confirm correct communication.



## Specifying the DAC Output voltage

Date .....

each DAC output level is the analog equivalent of a 12-bit unsigned digital value, D[11:0], written by the FPGA to the DAC via the SPI interface.

- The voltage on a specific output is generally described. The reference voltage, $V_{REFERENCE}$, is different between the four DAC outputs, channels A and B use a 3.3 V reference voltage, and channels C and D use a 2.5 V reference. The reference voltages themselves have a ± 5% tolerance, so there will be slight corresponding variances in the output voltage.

$$V_{OUT} = \frac{D[11:0]}{4.096} \times V_{REFERENCE}$$

- DAC outputs A and B

provides the output voltage equation for DAC outputs A & B. The reference voltage associated with DAC outputs A & B is 3.3 V ± 5%.

$$V_{OUTA} = \frac{D[11:0]}{4.096} \times (3.3\,V \pm 5\%)$$

- DAC outputs C and D

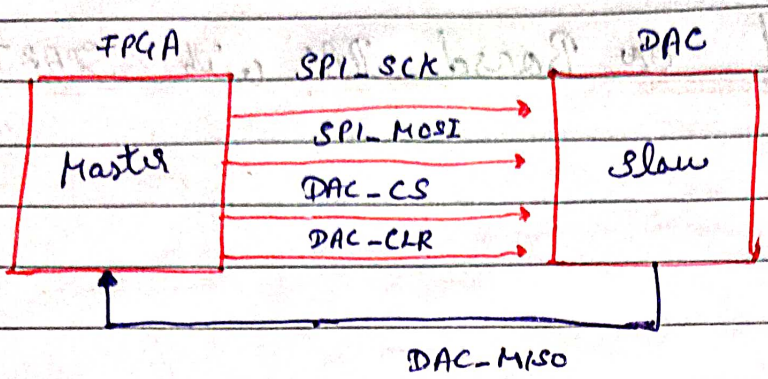
→ 2.5 V ± 5 %

$$V_{OUTC} = \frac{D[11:0]}{4.096} \times (2.5\,V \pm 5\%)$$

Spiral

Date .....

## ★ DAC - FPGA ( block Diagram)




★ 32 = 12 bit.

- DAC A ( channel A) selected.

$$\Rightarrow \frac{D[11:0]}{4096} \times 3.3 \text{ volt}$$

→ D[11:0] convert it in decimal no.

Ex:-> 1010 => 10

$$\Rightarrow \frac{10}{4096} \times 3.3 \Rightarrow 0.25$$

Here, 0.25 is the analog voltage of DAC A.

Steps

- Analog voltage for A, B, C, D → DACK.

→ if we select DACK A, then take a multi-meter then, you have to connect one probes of multimeter to this A pin and one probes to the ground.

→ then set the voltage part.

→ whatever voltage is shown, that is the 12-bit digital data that you sent on MOSI line.