

- SPI protocol is most famous and important interface in consumer electronics.

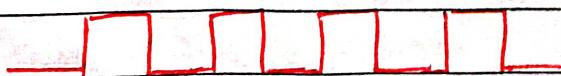
STUDY

SPI Protocol

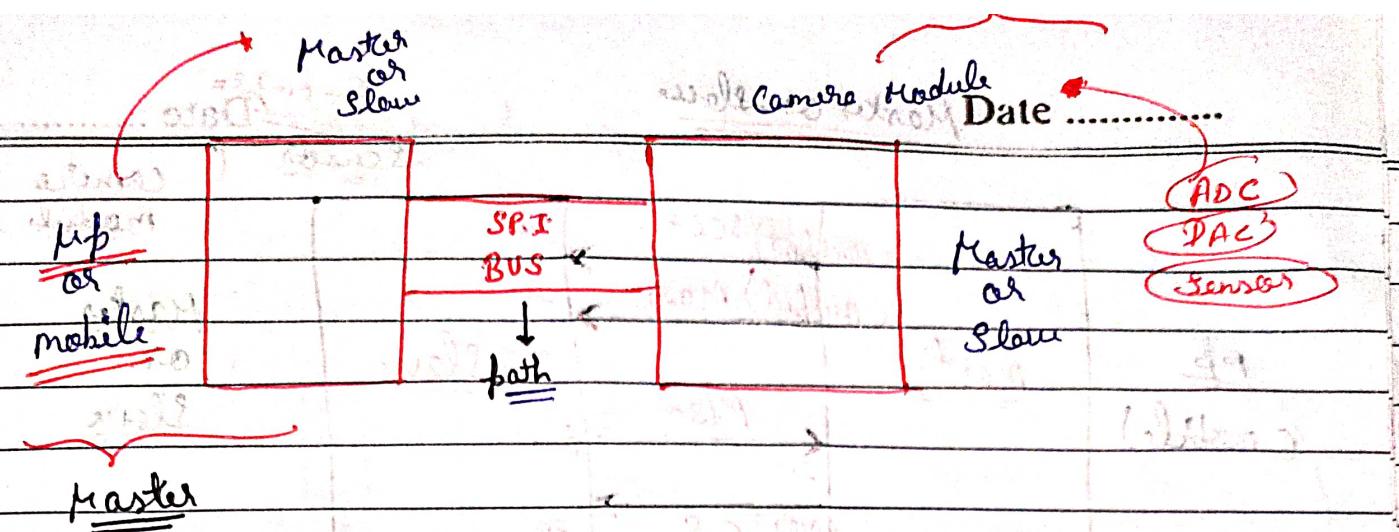
Date

SERIAL PERIPHERAL INTERFACE (SPI)

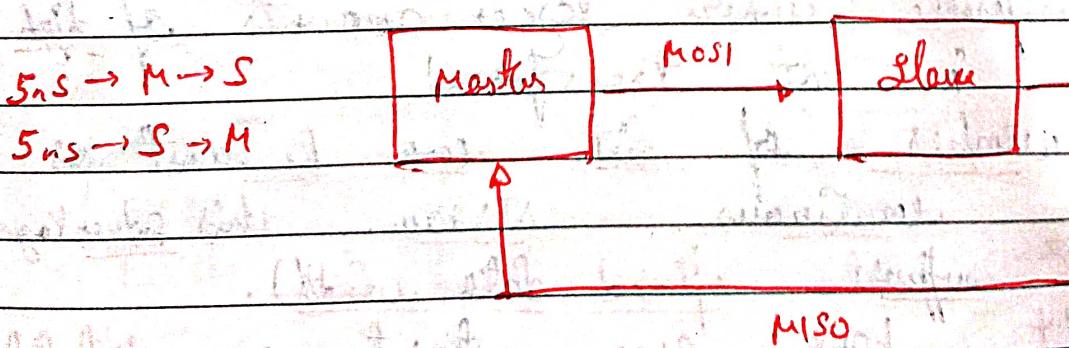
- Developed by Motorola. (Low cost, and simple interface, ease of use, use less hardware and system resources).
- SPI bus is used to send data b/w microcontrollers and peripherals like EEPROM, ADC, DAC, RTC, SENSORS, SD CARD, LCD, RFID CARD MODULE, WIRELESS TX/RX etc.
- It's a serial communication protocol.
- It's a synchronous data bus as master or slave is synchronized on the edges of clock.
 - Data Tx by master
Data Rx by slave
 - Data Tx by slave
Data Rx by master
- Max speed goes over 10 Mbps.



or triggered by clock edge
↑ ↓ ↑ ↓



- It's a simple bus having 4 wires for data communication.
- SCLK (serial clock used for all data communication)
- MOSI (master out slave in - output data line from master)
- MISO (master in slave out - input data line for master coming from slave)
- SS/CS (slave select / chip-select - used to select a slave).
- It's a simple master communication protocol where one device initiates the communication with slaves.
- It is full duplex (both master and slave can send date at same time through MOSI and MISO lines respectively).



- MOSI & MISO are independently lines so that master and slave may send data to each other.

Spiral

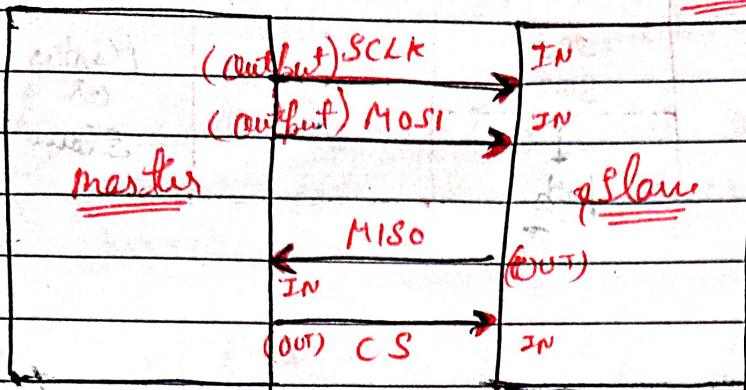
Master or Slave

Exempl

Date

Sensor

(camera module)

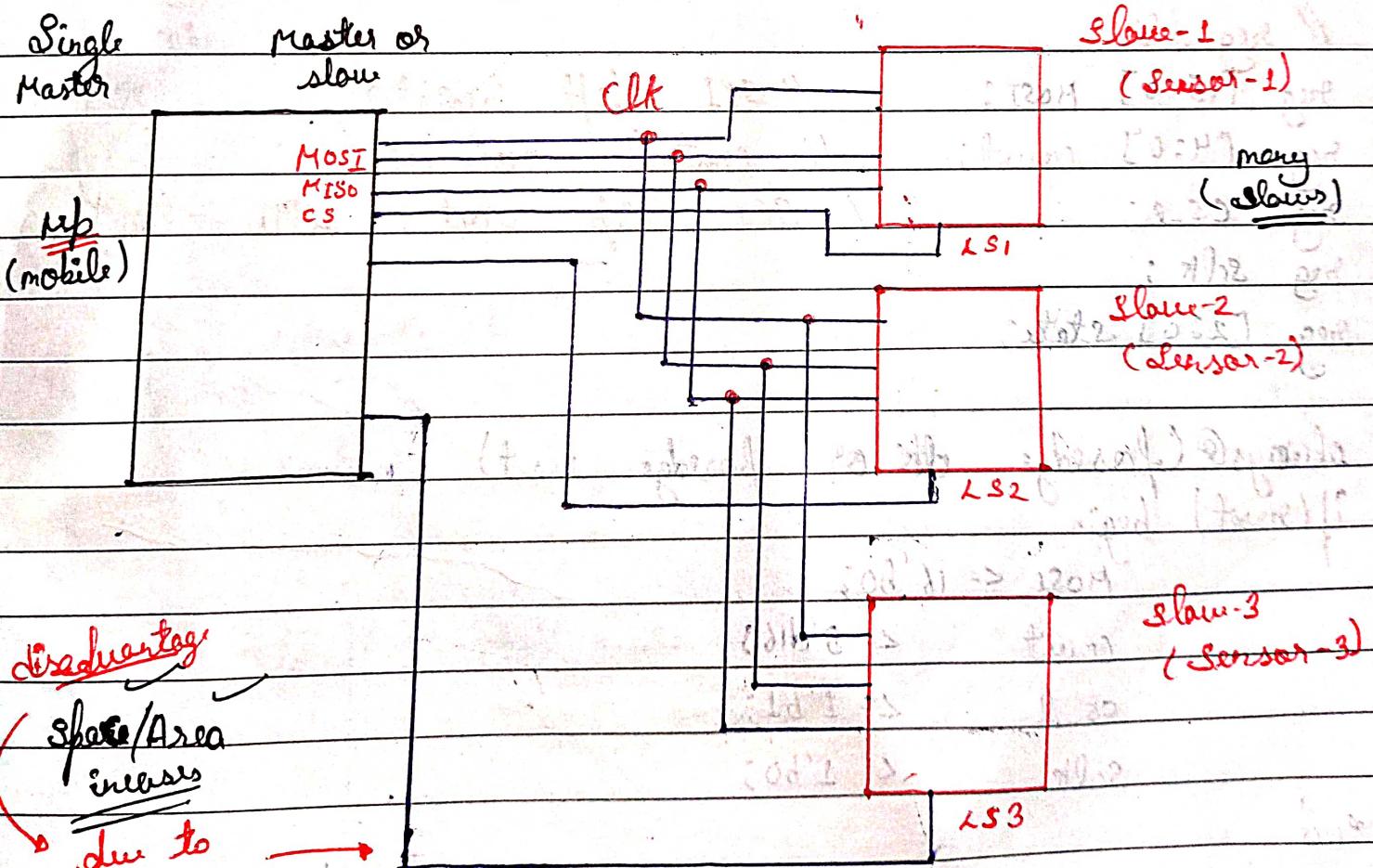
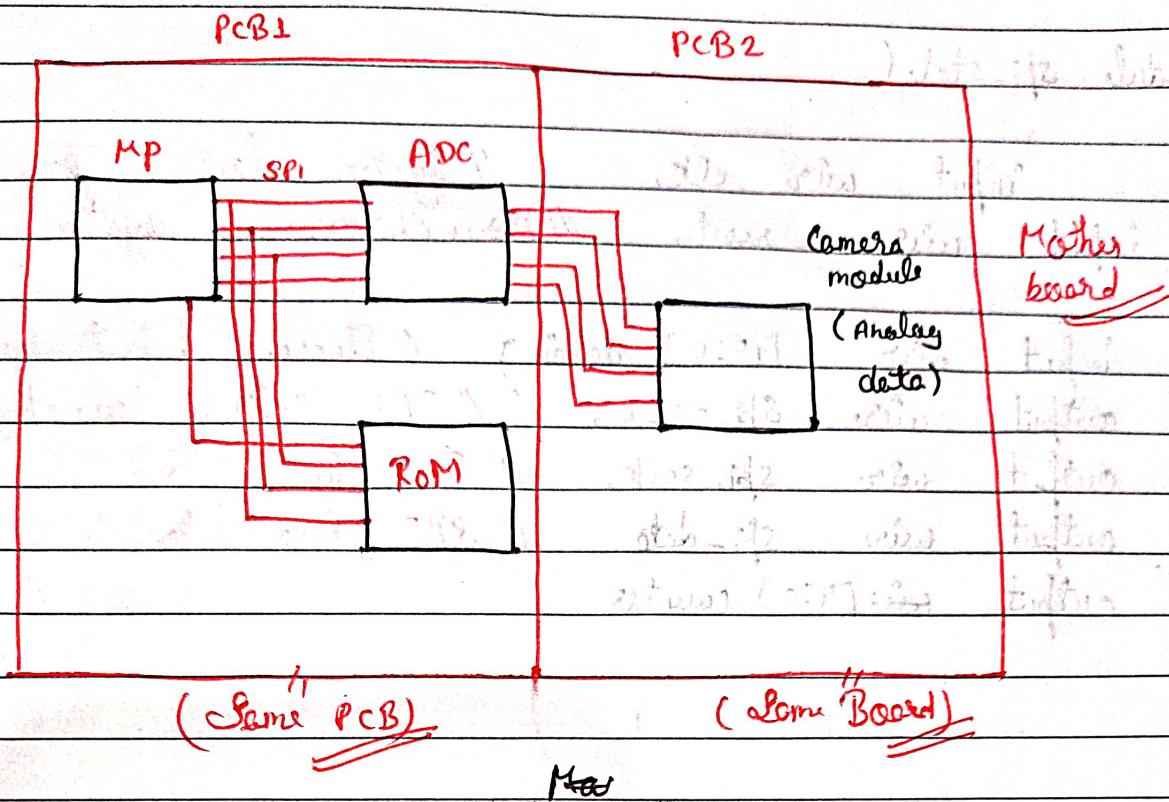


Slave can be any sensor.

1. It's normally used to short distance communication means communication within same circuit board or between the devices on the same PCB.
 2. If singular master means here one device is considered the master (microcontroller or processor) and all other peripheral devices (peripherals or other microcontroller) are considered as slaves. Slaves takes information from master.
 3. For every slave there is one SS lines so it occupies more space even more slaves are added. It is the disadvantage.
 4. Here only one master but it can have many slaves. (10Mbps)
 5. Its preferable where large amounts of high speed data is not transferred.
 6. Here any number of bit can be sent or received in a continuous stream. It's advantage. (some protocol support fixed data width).
 7. If doesn't have any start or stop bit, so, simple communication. (So no extra circuit required).
- (for error correction) \rightarrow (start stop bit)

Motherboard

Date



disadvantage

share/Area increases

→ due to →

extra CS line like (ss)

Shared

module spi_stat (

```

    input wire clk,           // System clock
    input wire reset,         // Asynchronous system reset
    input wire [15:0] datain, // Binary input vector
    output wire . spi_cs_l,   // SPI Active-low chip select
    output wire spi_sclk,     // SPI bus clock
    output wire spi_data,     // SPI bus data
    output wire [4:0] counter
);

```

// reg decl;

```

reg [15:0] MOSI;           // SPI shift register
reg [4:0] count;           // control counter
reg cs_l;                  // SPI chip select (active-low)
reg sclk;                 .
reg [2:0] state;

```

*always@ (posedge clk or posedge reset)**if (reset) begin*

MOSI <= 16'b0;

count <= 5'd16;

cs_l <= 1'b1;

sclk <= 1'b0;

*end**else begin**case (state)*

```

0: begin
    sclk     <= 1'b0;
    cs_l     <= 1'b1;
    stat     <= 1'0;
end

```

```

1: begin
    sclk     <= 1'b0;
    cs_l     <= 1'b0;
    MOSI    <= datain [count - 1];
    count   <= count - 1;
    State   <= 2;
end

```

```

2: begin
    sclk     <= 1'b1;
    if (count > 0)
        state <= 1;
    else begin
        count <= 16;
        state <= 0;
    end
end

```

default t: state <= 0;

endelse

end

```

assign spi_cs_l = cs_l;
assign spi_sclk = Sclk;
assign spi_data = MOSI; //MOSI
assign counter = count;
endmodule

```