FPGA Projects

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1. Nexys 4 FPGA Kit

- Nexys 4™ FPGA Board
- Artix 7 FPGA mounted on this chip.

Question:- Xilinx part number XC7A100T-1CSG324C.

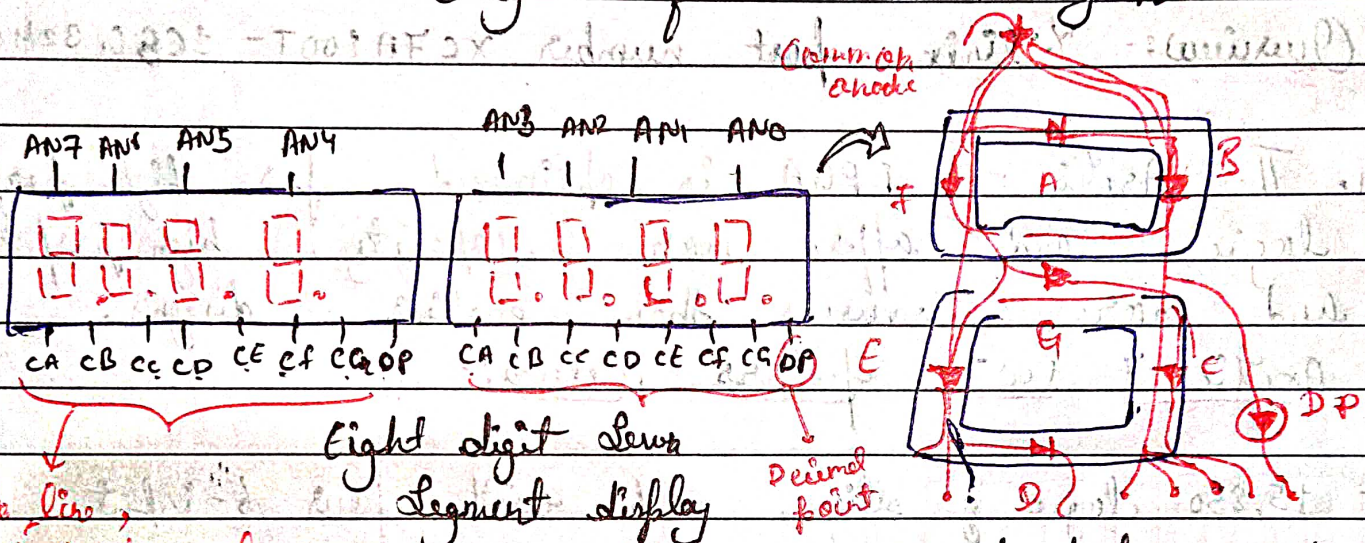
1. The Artix-7 FPGA is optimized for high performance logic, and offers more capacity, high performance, and more resources than earlier designs.

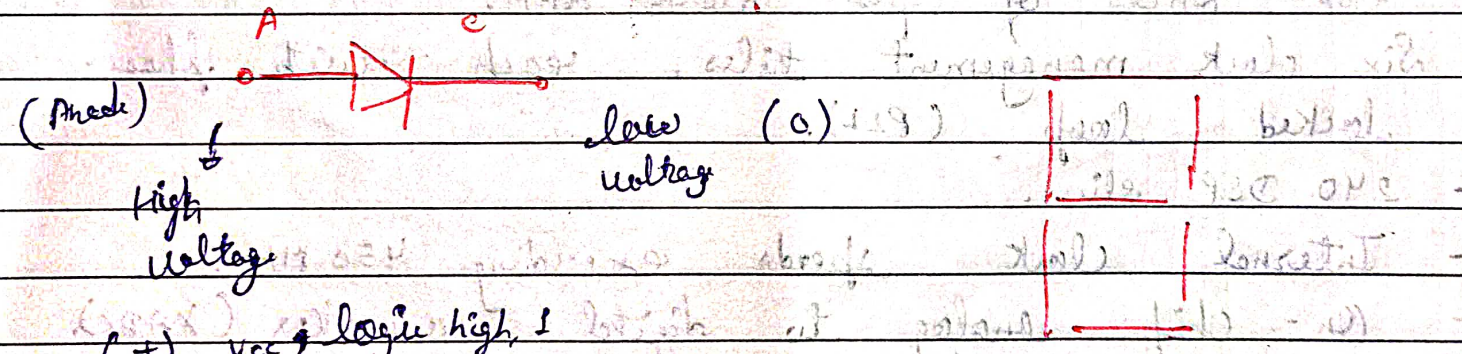
Artix-7 100T features include:-

- 15,850 logic g slices, each with four 6-input LUTs and 8 flip-flops.
- 4,860 kbits of fast block RAM.
- Six clock management tiles, each with phase-locked loop (PLL).
- 240 DSP slices.
- Internal clock speeds exceeding 450 MHz.
- On-chip analog to digital converter (XADC).

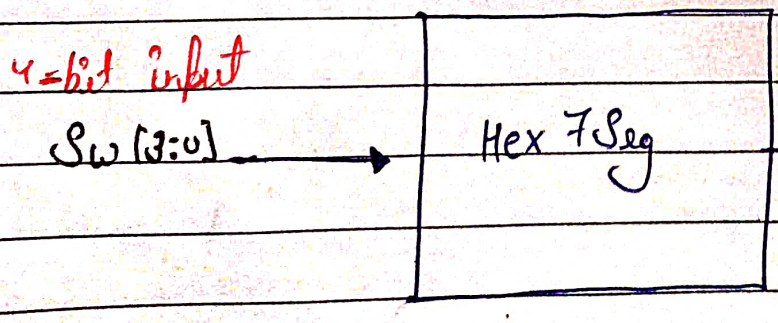
1. Overview of 7-segments and how they can be used on FPGA Board.
- verilog code for hex to 7 Segment conversion.

o Block diagram of - Hex to 7 Segment.





* Decoder → which connected to the FPGA



Spiral

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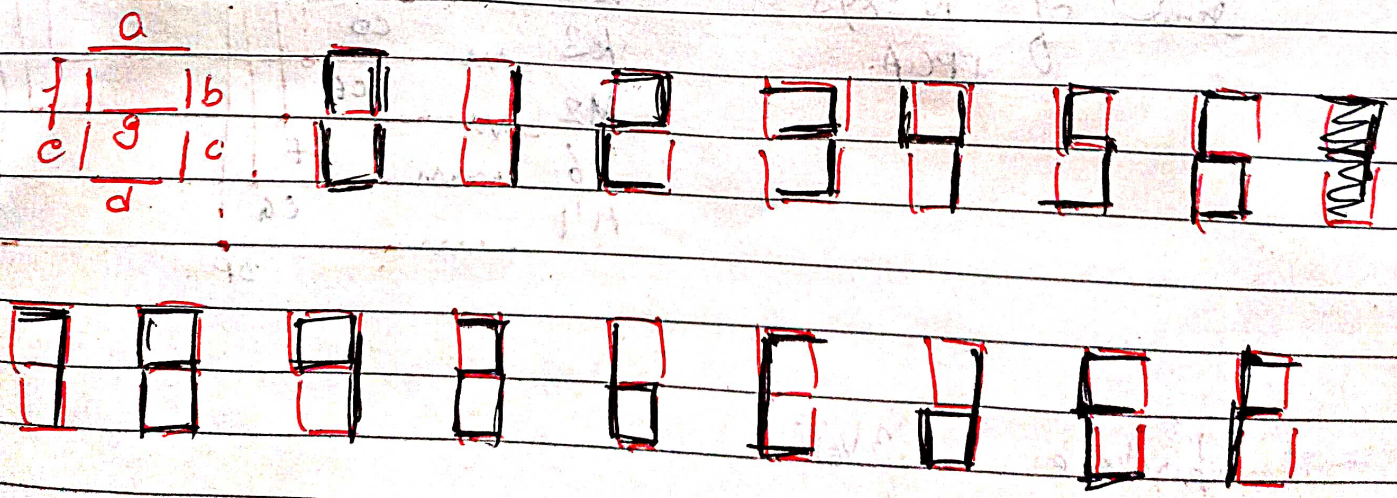
* How it is done?

Switches

Common Cathode

X	a	b	c	d	e	f	g
0000 ← 0	0	0	0	0	0	0	1
0001 ← 1	1	0	0	1	1	1	1
0010 ← 2	0	0	1	0	0	1	0
0011 ← 3	0	0	0	0	1	1	0
0100 ← 4	1	0	0	1	1	0	0
0101 ← 5	0	1	0	0	1	0	0
0110 ← 6	0	1	0	0	0	0	0
0111 ← 7	0	0	0	1	1	1	1
1000 ← 8	0	0	0	0	0	0	0
1001 ← 9	0	0	0	0	1	0	0
1010 ← A	0	0	0	1	0	0	0
1011 ← b	1	1	0	0	0	0	0
1100 ← C	0	1	1	0	0	0	1
1101 ← d	1	0	0	0	0	1	0
1110 ← E	0	1	1	0	0	0	0
1111 ← f	0	1	1	1	0	0	0



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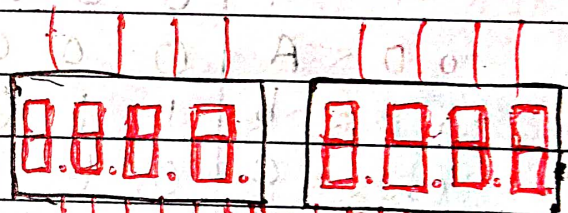
* 7 Seg on Nexys FPGA

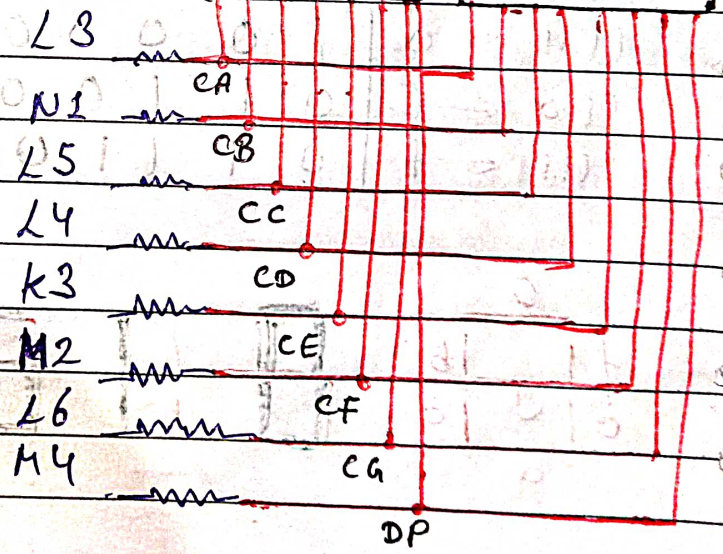
Switches { SW1 → U9, SW2 → U8, SW3 → R7, SW2 → R6 } inputs →

those input of Nexys FPGA → SW[3:0] → Hex7Seg → a_to_g[6:0] →

connected to the inputs of Hex7Seg



→ those output connect to the 7seg data pins of Nexys FPGA.



- It operates on 3.3 Volt.