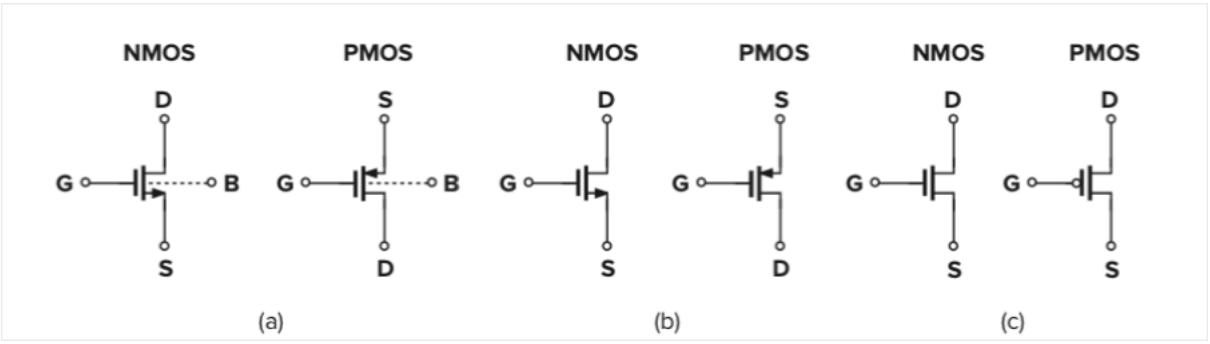
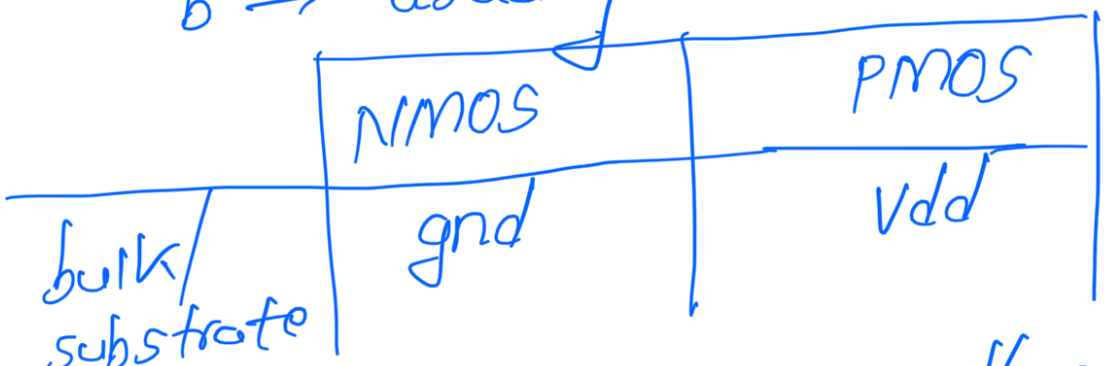
MOS Symbols :



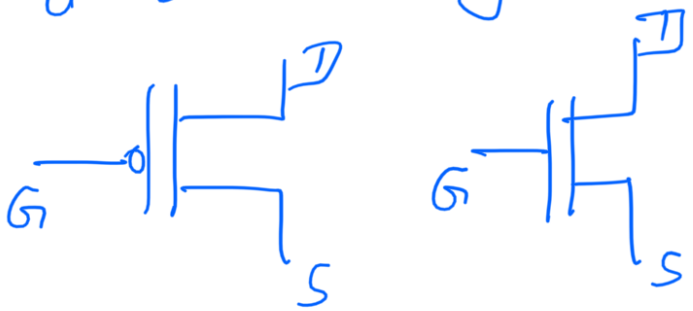
a → typical structure

b → usually we connect



So we are ignoring these terms representation.

c → rep² in digital circuits using a 'switch" symbols.



MOS I/V characteristics :-

generation & transport of charge as a function of terminal voltage.

1. Threshold Voltage

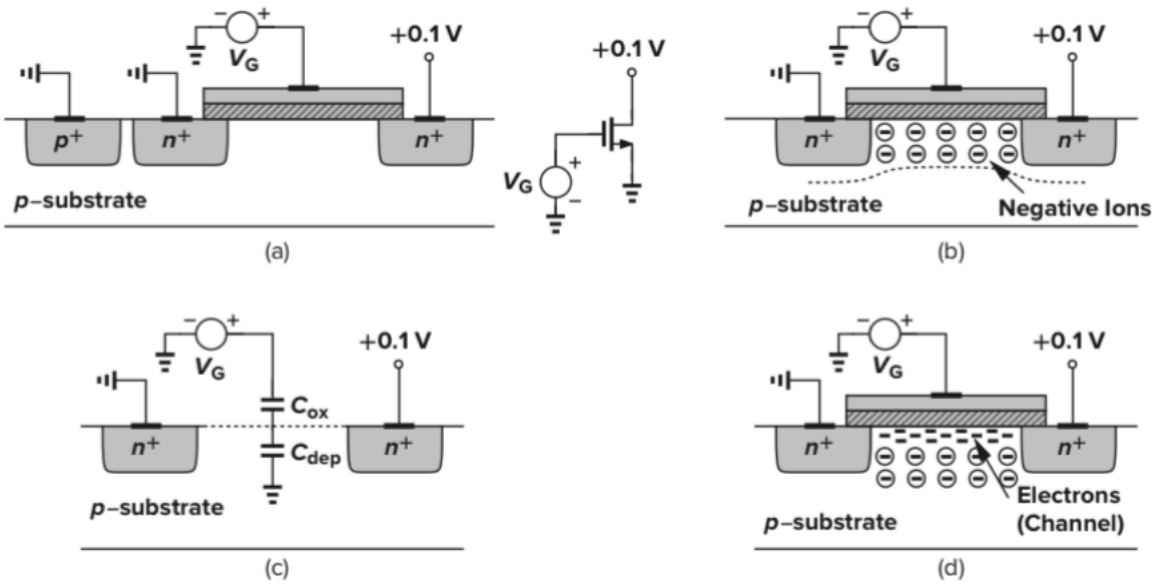
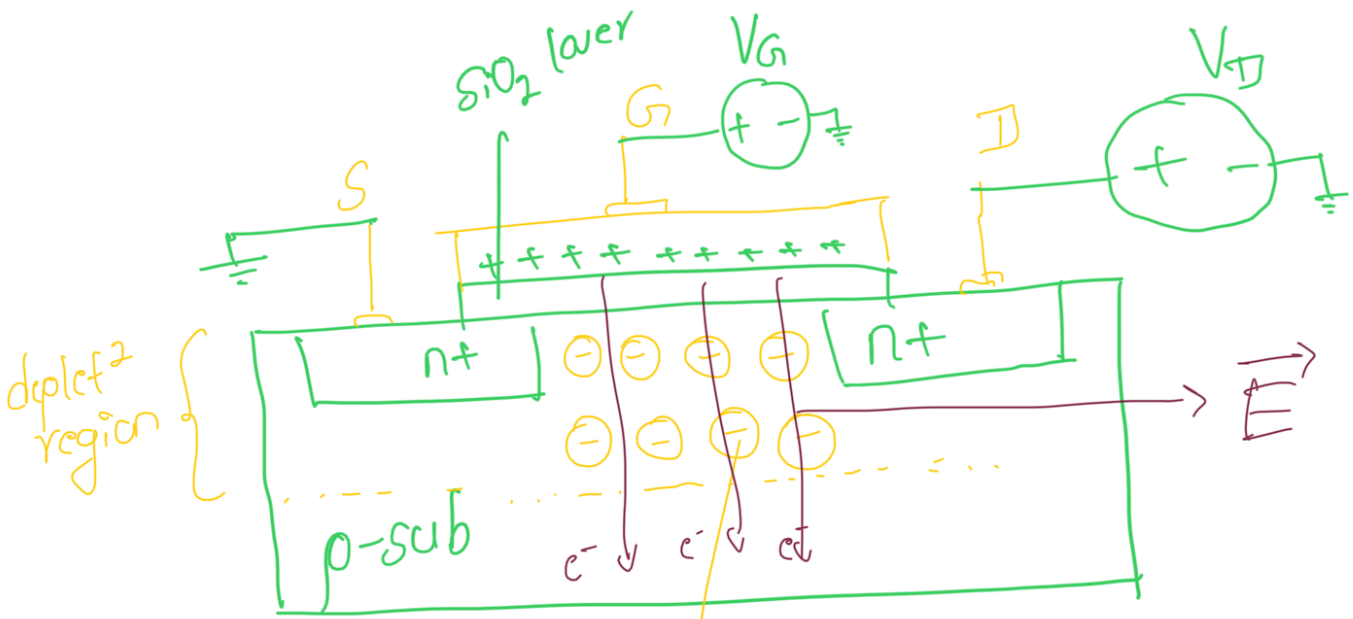


Figure 2.6 (a) A MOSFET driven by a gate voltage; (b) formation of depletion region; (c) onset of inversion; (d) formation of inversion layer.

When V_G increases from 0V,

- V_G becomes more $+^{ve}$
- holes in p-substrate repelled from gate area
  $\therefore +^{ve}$ repels $+^{ve}$

leaving $-^{ve}$ ions



negative ions (immobile)

So no current conduction.

It resembles like 2 capacitors in

series :

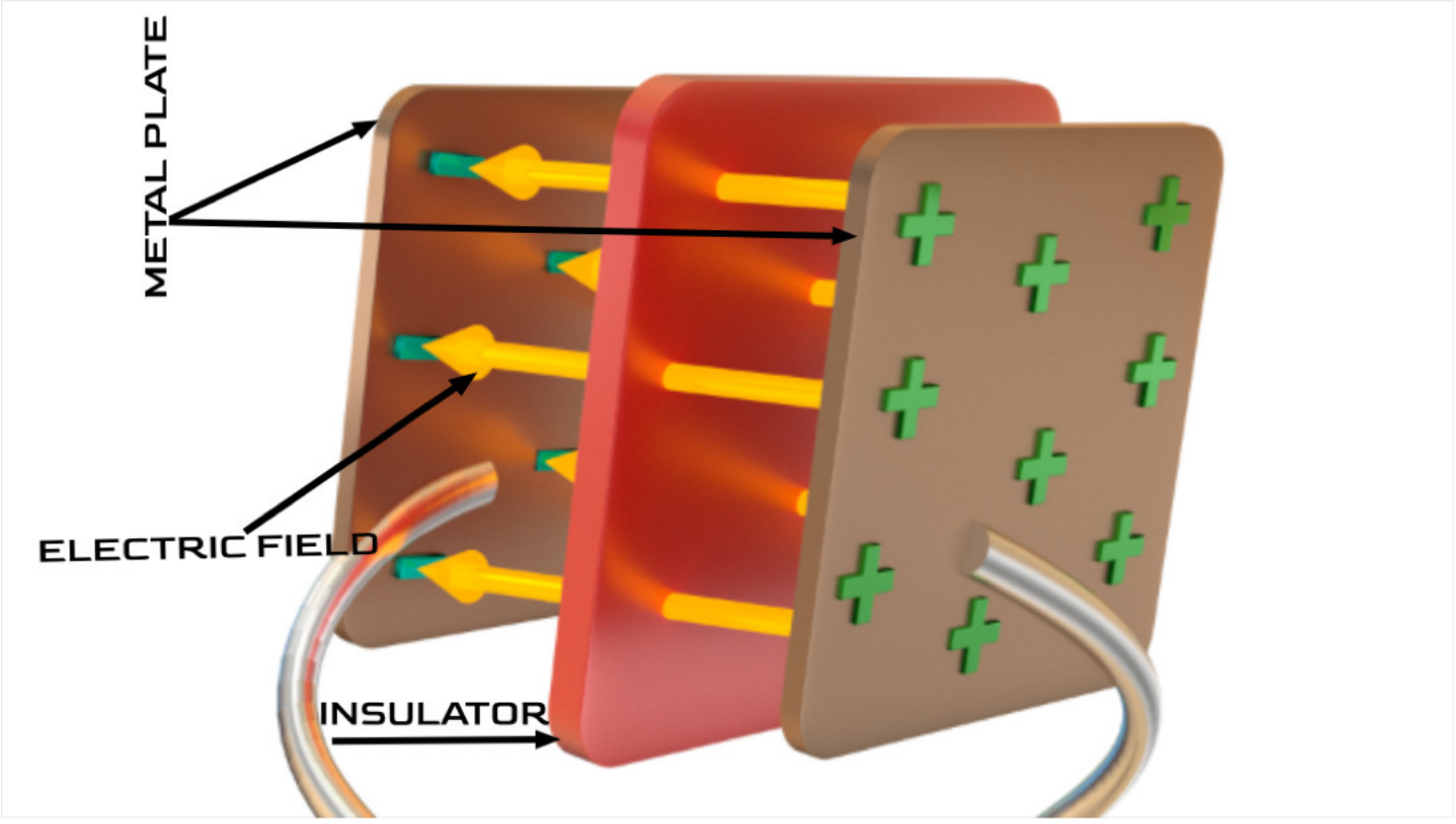
oxide cap — C_{ox}

depl^2 region cap — C_{dep}

- when $V_G \uparrow$, interface potential $\uparrow$

So, at certain interface potential.

the electric field blw



there are some free electrons even in the P-type region. The electric field produced by the capacitive action will attract the electrons

e⁻ flows from source to interface & eventually to drain.

"channel" of charge carriers formed under gate oxide b/w S & D.

hey!! our transistor is now turned ON.

interface is inverted

channel = inversion layer

Threshold Voltage :- The value of V_G for which channel inversion occurs. (V_{TH})

In Semiconductor Physics.

V_{TH} = gate voltage for which the interface is as much "n-type as the substrate is p-type"

Substrate

$$V_{TH} = \phi_{ms} + 2\phi_F + \frac{Q_{dep}}{C_{ox}}$$

ϕ_{ms} → difference b/w work functions of polysilicon gate & silicon substrate.

$$\phi_F = \left(\frac{kT}{q}\right) \ln\left(\frac{N_{sub}}{n_i}\right)$$

k → Boltzman's constant
1.38×10^{-23} J/k

q → electron charge
1.6×10^{-19} Coulombs

N_{sub} → doping density of substrate

n_i → density of e^- in undoped Si

Q_{dep} → charge in depletion region

source

C_{ox} → gate-oxide capacitance per unit area

$t_{ox} \approx 20\ A^\circ \Rightarrow C_{ox} \approx 17.25\ fF/\mu m^2$

But, in practice the native V_{TH} value may not be suited to circuit design.

V_{TH} is typically adjusted by implementation of dopants into channel area during device fabrication.

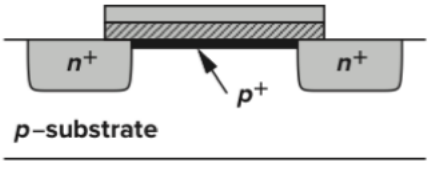


Figure 2.7 Implantation of $p+$ dopants to alter the threshold.

for PMOS, turn-ON phenomenon, all polarities of NMOS reversed

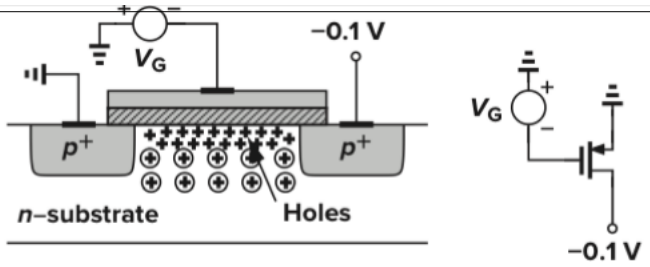


Figure 2.8 Formation of inversion layer in a PFET.