Why Anolog -> For small RF signal, it require ADC which consumes lot of power like the received signal is in range of few mili-voit & dup of few hundred u-seconds. So to make ADC (analog port) to consume very less power when digital signal is too small or so distorted analog equalizer is more preferable when doto rates are high. Lower Specd heigher good analog Annahan onatog dig falize digital demain Analog Design Challenges

-> Transistor Imperfections -> Declining Supply Voltage -> Power Consumption -> Crouit Complexity -> PVT variations L'fabrication process Loupply voltage Lambient temperature In multiple electronic devices on same substrate Integrated Why CMOS? Complementory MOS (with both p & n type tronsistive) + Device Scaling MASFET

Lower supply vottage

Lower supply vottage

Lovels of Abstraction:

device physics level

transistor level

orchitecture level

system level

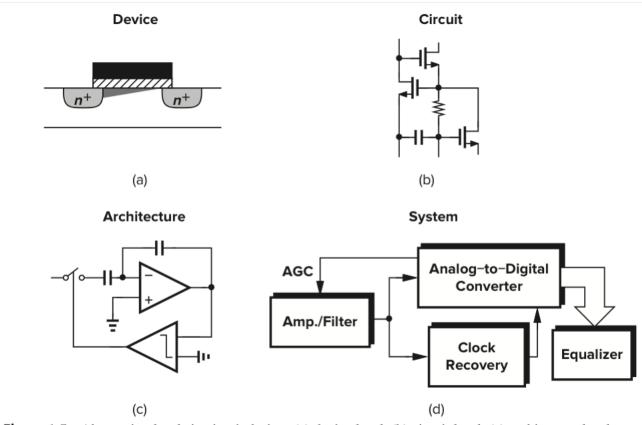


Figure 1.5 Abstraction levels in circuit design: (a) device level, (b) circuit level, (c) architecture level, (d) system level.