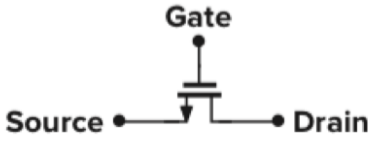
MOSFET

general consideration :

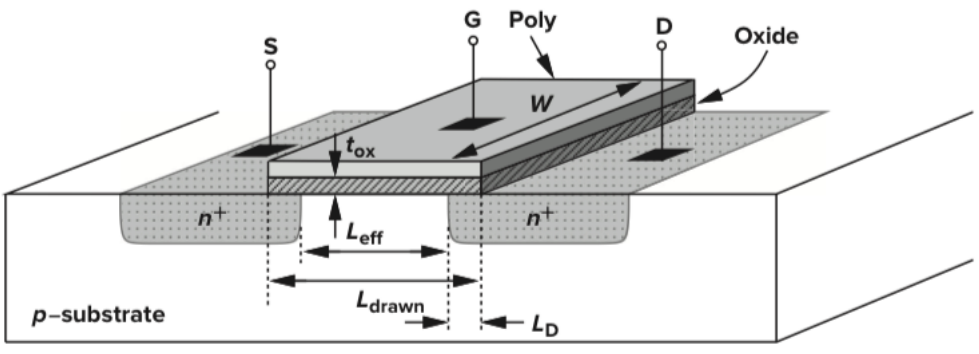
Let's consider MOSFET as switch.



→ transistor connects S & D together if gate voltage V_G is 'high'

→ isolates when V_G is low.

MOSFET structure :



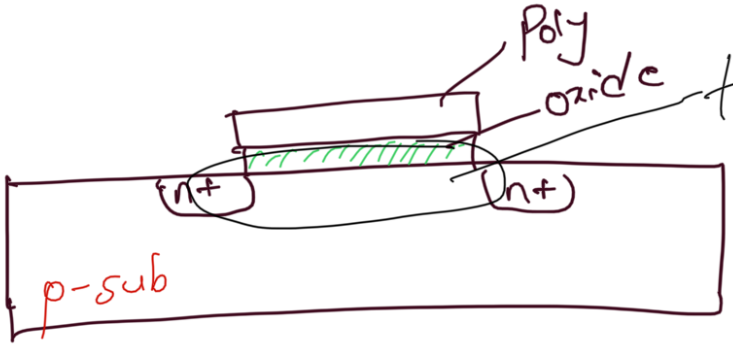
nMOS structure

Poly : heavily-doped conductive piece of Polysilicon. → gate

↳ What is Polysilicon?

It's Silicon in amorphous (non crystal) form

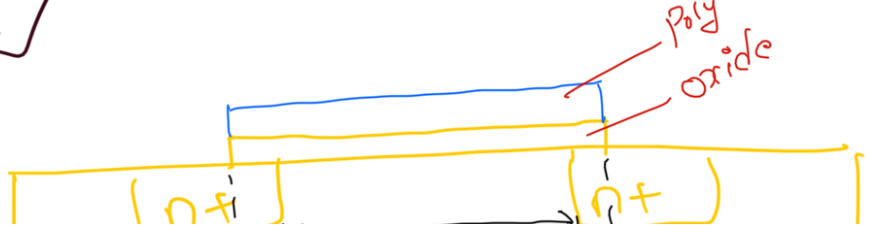
Oxide : SiO_2 → insulates gate from substrate

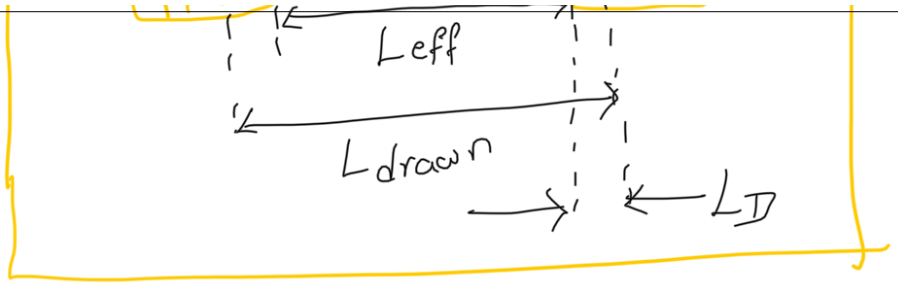


this is where useful action of device occurs.

Important dimentions :

a) Length :- Lateral dimension of gate along source-drain path





L_{eff} → L effective

L_{drawn} → Length that we draw in layout of transistor

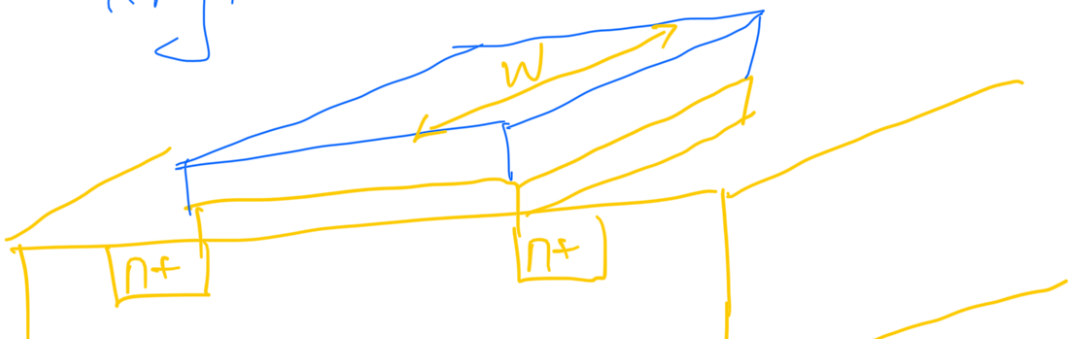
L_D → side diffusion

Side-diffusion of n+ here occur during fabrication.

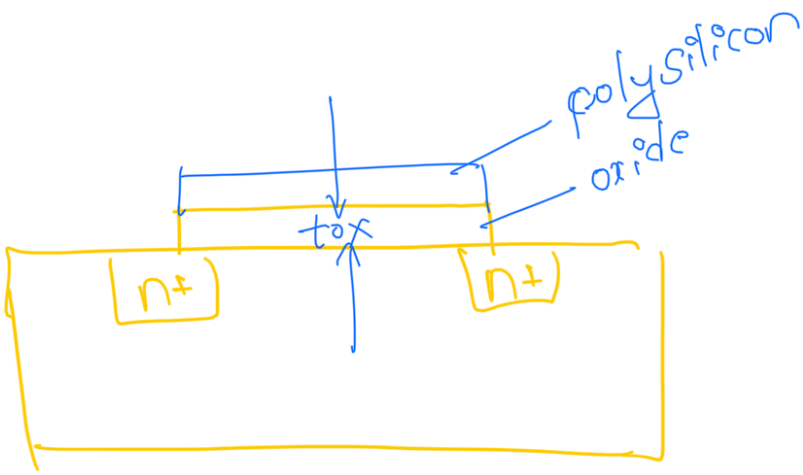
So, actual distance b/w S & D is

$$L_{eff} = L_{drawn} - 2L_D$$

*) Width :- perpendicular to transistor length



*) gate oxide thickness :- (t_{ox})



Leff & tox plays imp. role in performance of MOS circuit.

As generation ↑, principle thrust is to ↓ Leff & ↓ tox without degrading other parameter of device

---

∴ MOS structure is symmetric.

then why do we call

1 n region → source

another n region → drain

???

Source : terminal that provides charge carrier.

Drain : terminal that collects charge carrier.

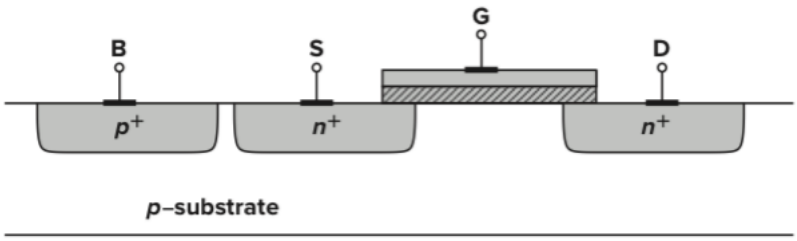
! S & D may exchange their roles depending on terminal voltage.

What is substrate ?

that's our base material on which we diffuse S & D regions.

potential is

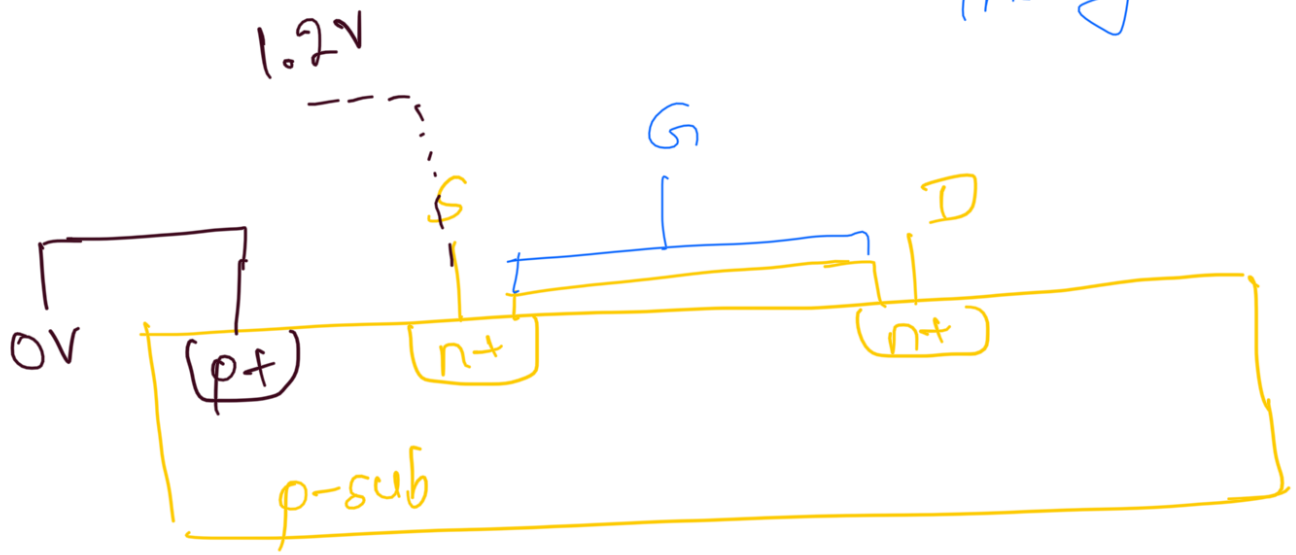
∴ Substrate [illegible] an important parameter which influences device characteristics



typical mos operation. S & D must be reverse biased.

∴ Substrate of NMOS

tied to most negative supply in the system.

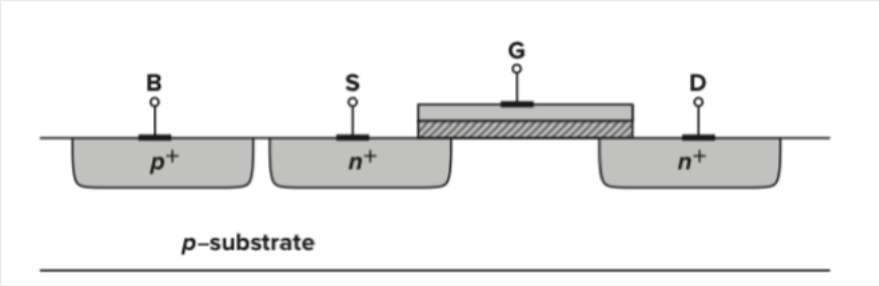


0V << 1.2V

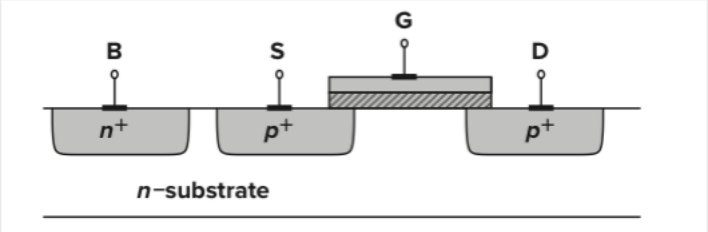
substrate source.

PMOS → negate all doping

types in MMOS



NMOS

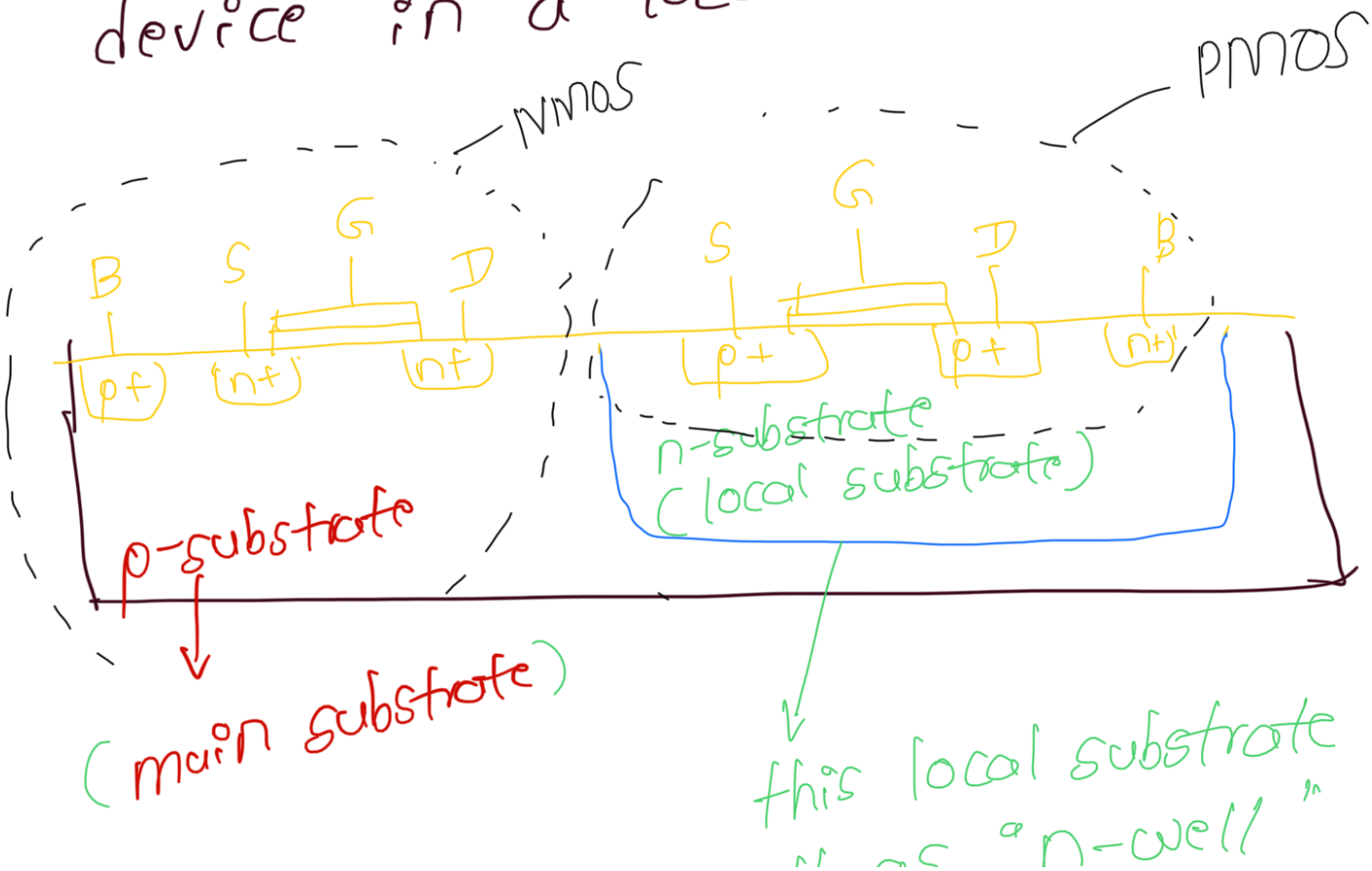


PMOS

here we are using 2 base wafers. n-substrate & p-substrate

→ but in practice, we build both NMOS & PMOS on same wafer [Complementary MOS (CMOS)]

So we can place one of the device in a "local substrate"



we call as

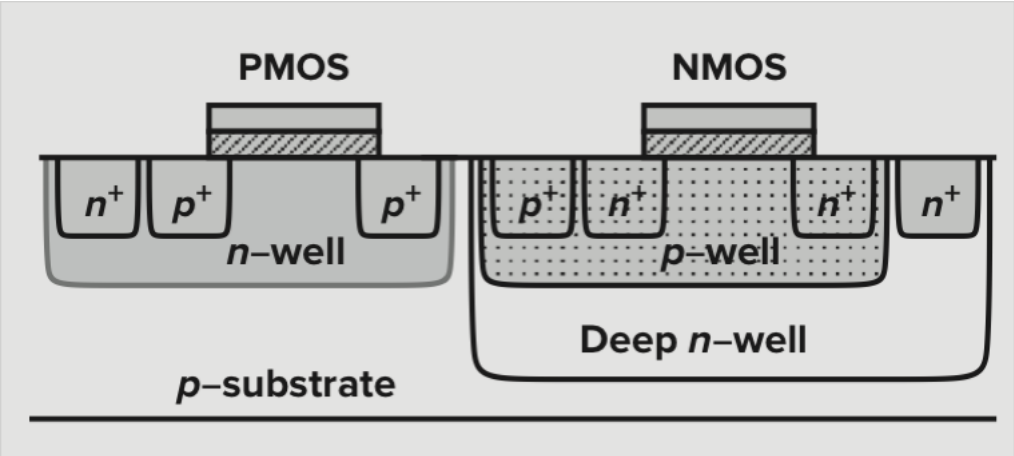
- all nmos share same substrate
- each pmos can have independant n-well

What I have to do if I want few NMOS's bulk have to be at different potential?

Since we told, all NMOS share a common substrate i.e bulk, how can we achieve NMOS inside CMOS with different substrate potential?

i.e We use Deep n-well

n-well (n-type substrate) which contains NMOS device & it's p+ bulk.



So, here

isolated bulk of NMOS using deep n-well technique