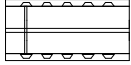


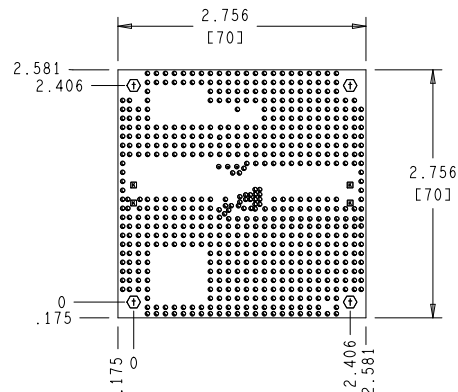
Cu  
Thick. Cu Foil  
Layer (mils) wt(oz)  
1 2.40 2 oz



Layers Drill Type Via Fill  
1-2 PTH --  
TOTAL 62 MILS +/-10% thickness board

DRILL CHART: TOP to BOTTOM  
ALL UNITS ARE IN MILS

FIGURE	SIZE	TOLERANCE	PLATED	QTY
•	12.0	+3.0/-10.0	PLATED	597
•	40.0	+3.0/-3.0	PLATED	3
⊗	63.0	+3.0/-3.0	PLATED	4
①	150.0	+3.0/-3.0	PLATED	4



FAB NOTE

#### NOTES:

- Specifications.
  - Fabricate IAW IPC600, latest revision.
  - Producibility study - It is the responsibility of the supplier to conduct a thorough review of the artwork and media for manufacturability in the supplier's process compliance to all applicable specifications. Customer must be advised in writing (in advance of manufacturing) of any changes, revisions, or corrections made or recommendations to ensure conformance to standards, and of any specifications that cannot be met.
  - This drawing is to be used in conjunction with the provided gerber and drill data when applicable.
  - All notes are "Unless Otherwise Specified."
- Material.
  - FR406.
  - Color to be opaque.
- Soldermask  
Solder mask both sides with (green color) liquid photoimageable soldermask, 003 max. thickness.  
Soldermask over bare copper.  
Soldermask is allowed in via holes.
- Drilling
  - All hole diameters are finished sizes.
  - All hole to be +/- .003 from true position unless otherwise specified.
  - All hole diameters to be +/- .003 unless otherwise specified.
  - An NC drill file has been supplied - see drill table.
- Finish
  - Plate thru with copper .0010 min to .002 max. thickness drill size dimension apply after plating.
  - Use gold immersion over nickel.
  - Finished boards shall not have nicks, scratches, voids, exposed copper, poor plating, all misdrilled holes.
- Silkscreen
  - Silkscreen using white non-conductive epoxy or equivalent (both sides).
  - No silkscreen allowed on exposed lands.
  - Silkscreen must be a minimum of 3mm away from fiducial marks.
  - Minimum clearance between silkscreen legend and vias, pads, or holes to be .005.
  - Silkscreen is allowed in via holes.
- Electrical Test
  - All boards shall be 100% electrically tested for opens/short at 10 volts. MIL-SPEC boards to be tested at 40 volts.
  - Apply test stamp in non-legend area on solder side of PCB.
  - Test is required on both sides of the board.
- Cleanliness
  - Boards shall be free of fiber glass dust or any other foreign material.
  - Finished boards must conform to 0.01 MG/IN max NaCl ionic contamination as measured by the omega meter 600SMD.
- Packaging  
There shall be a max of 25 units per package, individually wrapped, and shipped in cardboard cratons with sufficient surrounding material to prevent shipping damage.
- Bow and Twist  
Bow and twist to be .007 IN/IN or .090 max according to IPC-A-600D.
- Inspection
  - Automatic optical inspection of all layers required.
  - The impedance should be controlled by stackup layer.
- Inside corners should be rounded-off
- Changes to board geometries and apertures are not allowed unless they are approved by customer.
- Rounding is allowed on 90 degree corners with the size of standard routing bit.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

<b>ROHM</b> SEMICONDUCTOR	FAB DRAWING	COMPANY NAME: ROHM SEMICONDUCTOR USA	UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES  TOLERANCES DECIMAL ANGLES FRACTIONS HOLE DIA. HOLE DIA. HOLE DIA.
	DESIGNER: PTHDC	PROJECT NAME: BD9109FVMEVX-101	
	CHECKER: INITIAL	FAB NUMBER:	
	DATE: 2008/10/10	REV: 00	
JON		NUMBER	00 1 OF 2