Application Note

ROHM Switching Regulator Solutions

Evaluation Board: 4.5V to 18V, 6A Integrated MOSFET 1ch Synchronous Buck DC/DC Converter

BD9C601EFJEVK-101 (3.3V | 6A Output)

No.000000000

● Introduction

This application note will provide the steps necessary to operate and evaluate ROHM's synchronous buck DC/DC converter using the BD9C601EFJ evaluation boards. Component selection, board layout recommendations, operation procedures and application data is provided.

● Description

This evaluation board has been developed for ROHM's synchronous buck DC/DC converter customers evaluating BD9C601EFJ. While accepting a wide power supply of 4.5-18V, an output of 3.3V can be produced. The IC has internal 50mΩ high-side Nch MOSFET and 35mΩ low-side Nch MOSFET and a synchronization frequency is of 500 kHz. A fixed Soft Start circuit prevents in-rush current during startup along with UVLO (Under Voltage Lockout Protection) and TSD (Thermal Shutdown Protection) circuits. An EN pin allows for simple ON/OFF control of the IC to reduce standby current consumption. Include OCP (Over Current Protection) and SCP (Short Circuit Protection).

● Applications

LCD TVs
Set Top Boxes (STB)
DVD/Blu-ray players/recorders
Broadband Network and Communication Interface
Entertainment Devices

● Evaluation Board Operating Limits and Absolute Maximum Ratings (TA=25ºC)

Parameter		Symbol	Limit			Unit	Conditions
			MIN	TYP	MAX		
Supply Voltage							
	BD9C601EFJ	V_{CC}	4.5	-	18	V	
Output Voltage / Current							
	BD9C601EFJ	V_{OUT}	-	3.3	-	V	
		I_{OUT}	-	-	6	A	

● Evaluation Board

Below is evaluation board with the BD9C601EFJ.

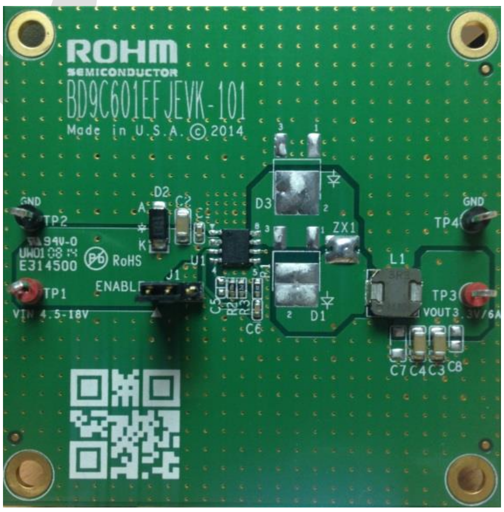
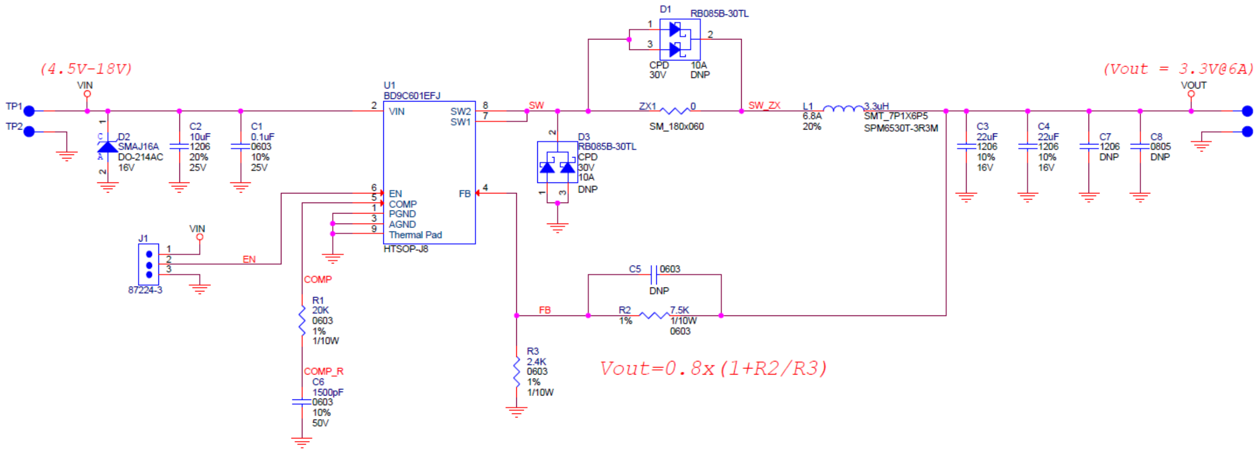


Fig 1: BD9C601EFJ Evaluation Board

- **Evaluation Board Schematic**

  Below is evaluation board schematic for BD9C601EFJ.



Note (D1,D3): *If a large inductive load is connected that might introduce back electromotive force at the start up and output, please insert protection diodes D1, D3 and remove solder short at ZX1.*

Fig 2: BD9C601EFJ Evaluation Board Schematic

- **Evaluation Board I/O**

  Below is reference application circuit that shows the inputs (V_{IN}, EN) and the output (V_{OUT}).

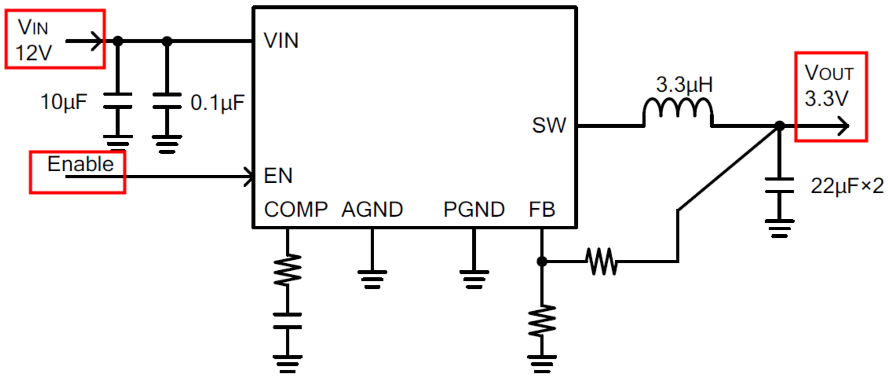


Fig 3: BD9C601EFJ Evaluation Board I/O

- **Evaluation Board Operation Procedures**

  Below is the procedure to operate the evaluation board.

1. Connect power supply's GND terminal to GND test point TP2 on the evaluation board.
2. Connect power supply's VCC terminal to VIN test point TP1 on the evaluation board. This will provide VIN to the IC U1. Please note that the V_{CC} should be in range of 4.5V to 18V.
3. Check if shunt jumper of J1 is at position ON (Pin2 connect to Pin1, EN pin of IC U1 is pulled high as default).
4. Now the output voltage V_{OUT} (+3.3V) can be measured at the test point TP3 on the evaluation board with a load attached. The load can be increased up to 6A MAX.

Notes:

Do not perform hot plugging on this board because the peak voltage transition could exceed the maximum voltage input rating 20V of BD9C601EFJ which may cause IC damage. Please refer figure 4

- **Reference Application Data for BD9C601EFJEVK-101**

  Following graphs show hot plugging test, quiescent current, efficiency, load response, output voltage ripple response of the BD9C601EFJ evaluation board.

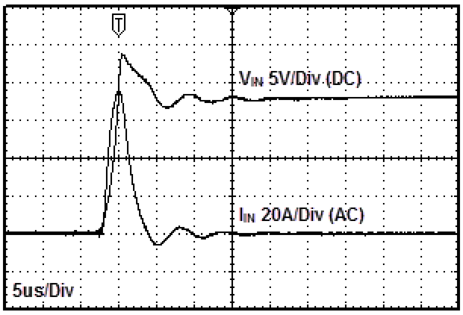


Fig 4: Hot Plug-in Test with TVS Diode SMAJ16A, V_{IN}=18V, V_{OUT}=3.3V, I_{OUT}=6A

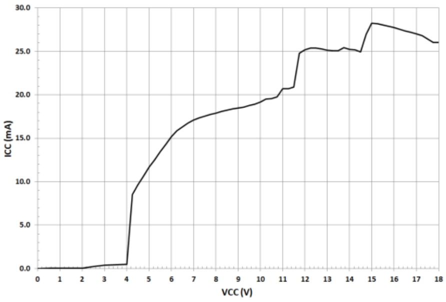


Fig 5: Circuit Current vs. Power supply Voltage Characteristics (Temp=25°C)

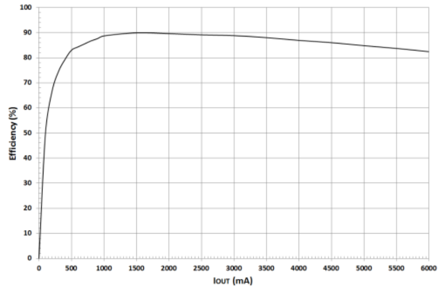


Fig 6: Electric Power Conversion Rate (V_{IN}=12V, V_{OUT}=3.3V)

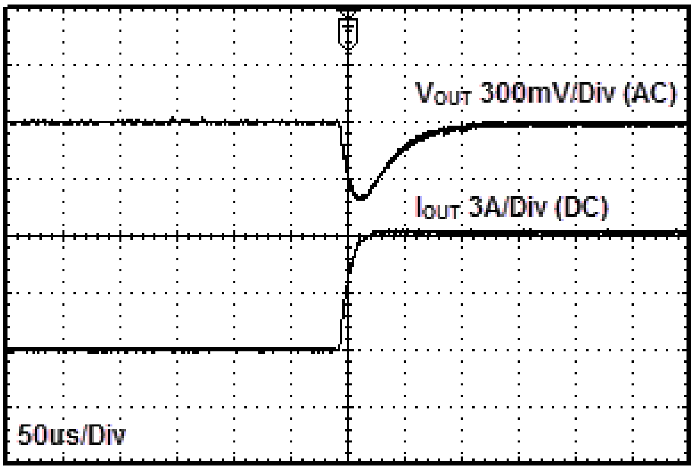


Fig 7: Load Response Characteristics
(V_{IN}=12V, V_{OUT}=3.3V, L=3.3uH, C_{OUT}=22uF[x2], I_{OUT}=0A→6A)

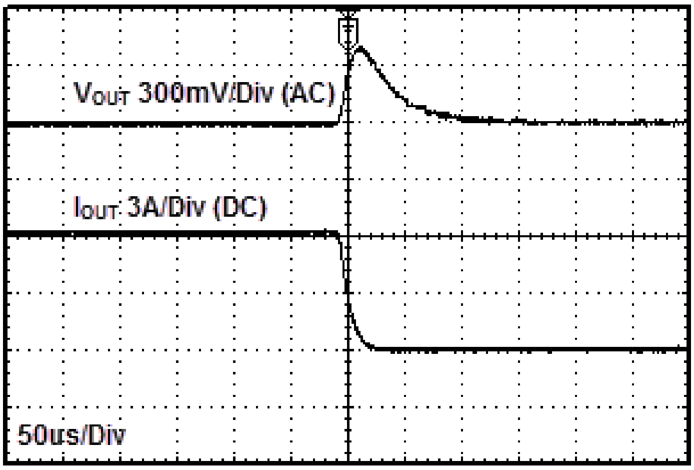


Fig 8: Load Response Characteristics
(V_{IN}=12V, V_{OUT}=3.3V, L=3.3uH, C_{OUT}=22uF[x2], I_{OUT}=6A→0A)

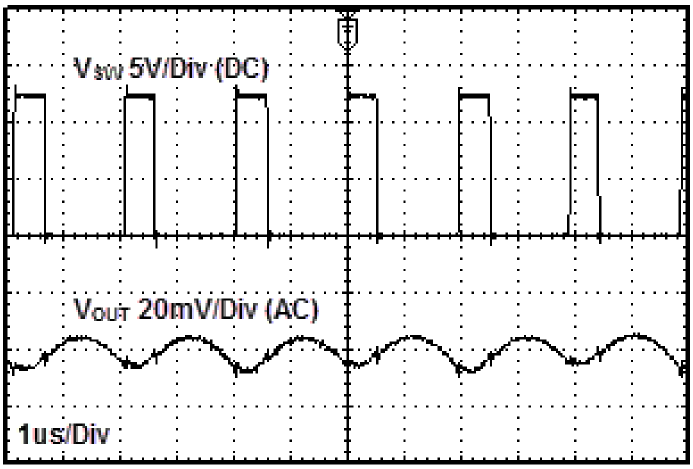


Fig 9: Output Voltage Ripple Response Characteristics
(V_{IN}=12V, V_{OUT}=3.3V, L=3.3uH, C_{OUT}=22uF[x2], I_{OUT}=0A)

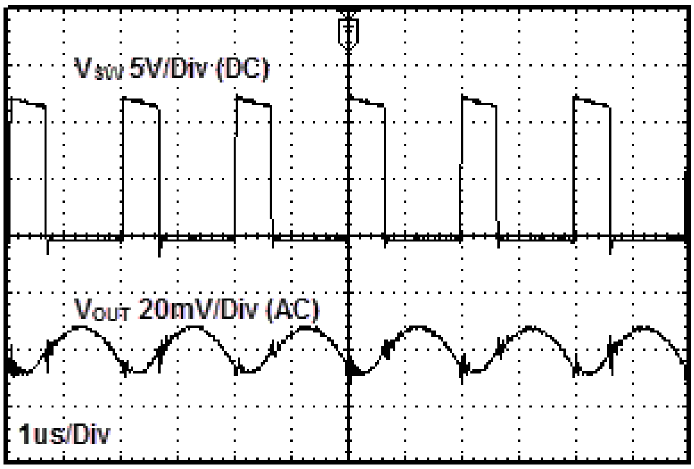


Fig 10: Output Voltage Ripple Response Characteristics
(V_{IN}=12V, V_{OUT}=3.3V, L=3.3uH, C_{OUT}=22uF[x2], I_{OUT}=6A)

- **Evaluation Board Layout Guidelines**

In the step-down DC/DC converter, a large pulse current flows into two loops. The first loop is the one into which the current flows when the top FET is turned ON. The flow starts from the input capacitor C_{IN}, runs through the FET, inductor L and output capacitor C_{OUT} and back to GND of C_{IN} via GND of C_{OUT}. The second loop is the one into which the current flows when the bottom FET is turned on. The flow starts from the bottom FET, runs through the inductor L and output capacitor C_{OUT} and back to GND of the bottom FET via GND of C_{OUT}. Route these two loops as thick and as short as possible to allow noise to be reduced for improved efficiency. It is recommended to connect the input and output capacitors directly to the GND plane. The PCB layout has a great influence on the DC/DC converter in terms of all of the heat generation, noise and efficiency characteristics.

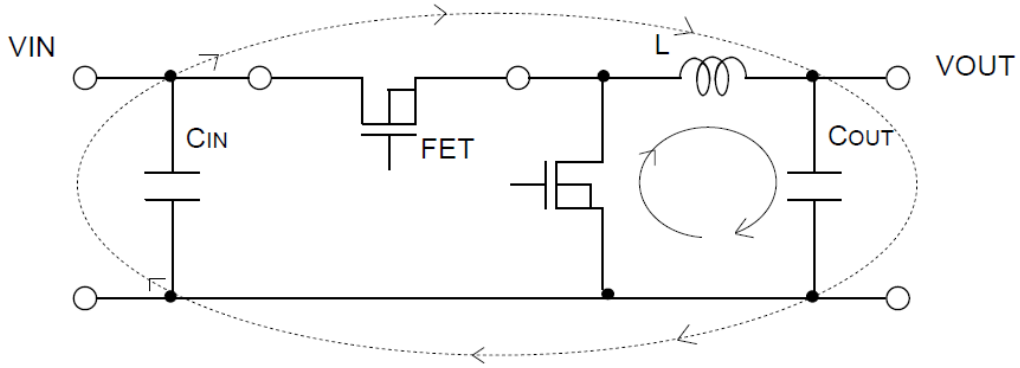


Fig 11: Current loop Buck regulator system

Accordingly, design the PCB layout considering the following points.

- Connect an input capacitor as close as possible to the IC VIN pin on the same plane as the IC.
- If there is any unused area on the PCB, provide a copper foil plane for the GND node to assist heat dissipation from the IC and the surrounding components.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Route the coil pattern as thick and as short as possible.
- Provide lines connected to FB and COMP far from the SW nodes.
- Place the output capacitor away from the input capacitor in order to avoid the effect of harmonic noise from the input.

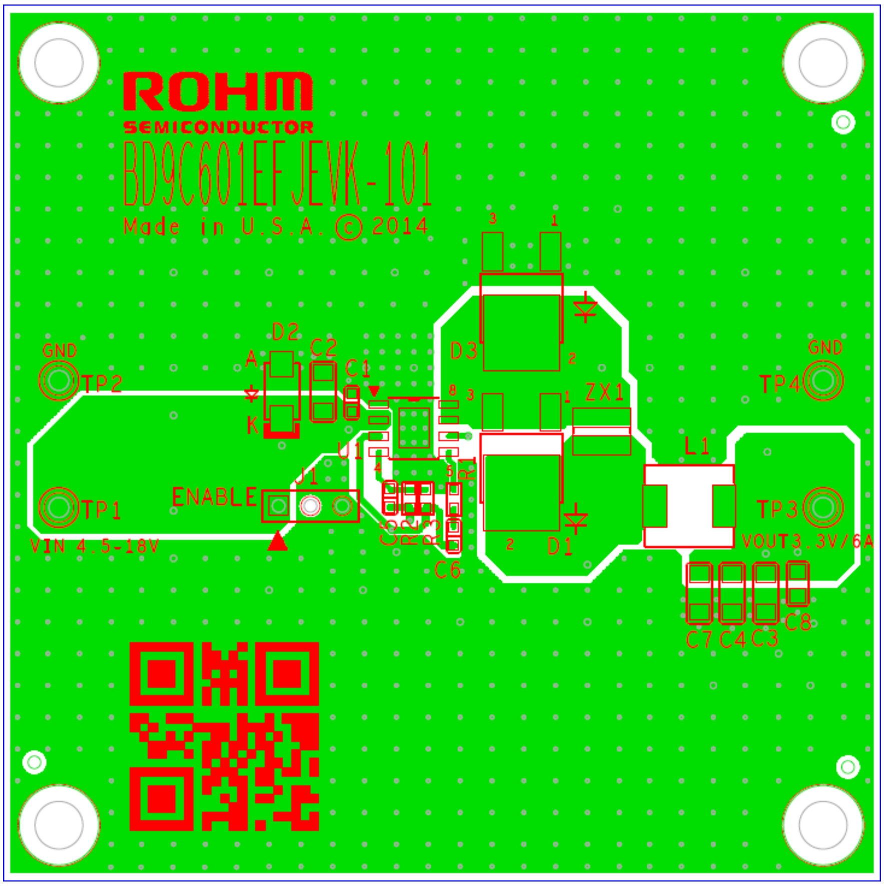


Fig 12: BD9C601EFJ Evaluation Board PCB Layout

- **Calculation of Application Circuit Components**

1. Output LC Filter Constant

The DC/DC converter requires an LC filter for smoothing the output voltage in order to supply a continuous current to the load. Selecting an inductor with a large inductance causes the ripple current ΔIL that flows into the inductor to be small. However, decreasing the ripple voltage generated in the output is not advantageous in terms of the load transient response characteristic. An inductor with a small inductance improves the transient response characteristic but causes the inductor ripple current to be large which increases the ripple voltage in the output voltage, showing a trade-off relationship. It is recommended to select an inductance such that the size of the ripple current component of the coil will be 20% to 40% of the average output current (average inductor current).

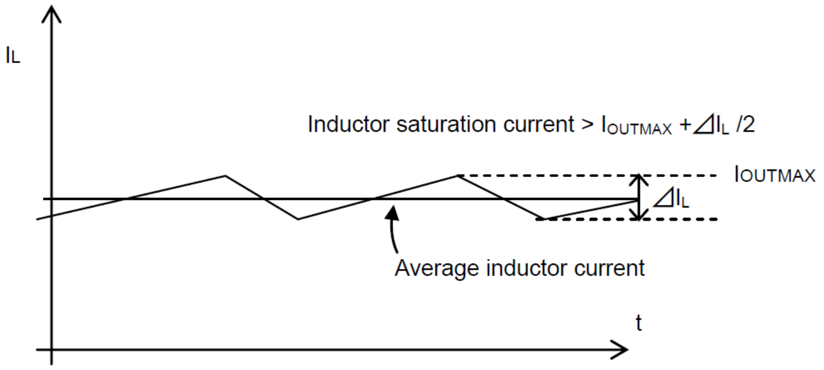


Fig 13: Waveform of current through inductor

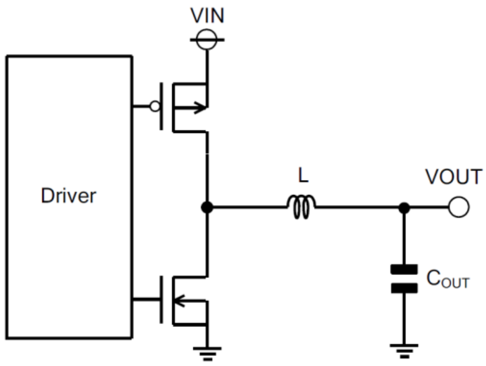


Fig 14: Output LC filter circuit

With V_{IN} = 12 V, V_{OUT} = 3.3 V and the switching frequency F_{OSC} = 500 kHz, the calculation is shown in the following equation.
Coil ripple current ΔI_L = 30% x Average output current (5A) = 1.5 [A]

$$L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times F_{OSC} \times \Delta I_L} = 3.19\mu H \approx 3.3\mu H$$

Where: F_{OSC} is a switching frequency

The saturation current of the inductor must be larger than the sum of the maximum output current and 1/2 of the inductor ripple current ΔI_L.
The output capacitor COUT affects the output ripple voltage characteristics. The output capacitor COUT must satisfy the required ripple voltage characteristics.
The output ripple voltage can be represented by the following equation.

$$\Delta V_{RPL} = \Delta I_L \times \left(R_{ESR} + \frac{1}{8 \times C_{OUT} \times F_{OSC}} \right) \ [V]$$

Where: R_{ESR} is the Equivalent Series Resistance (ESR) of the output capacitor.

Also this IC provides 1msec [Typ.] soft start function to reduce sudden current which flows in output capacitor when startup. But when capacity value of output capacitor COUT becomes bigger than the following method, correct soft start waveform may not appear in some cases (Ex. V_{OUT} over shoot at soft start).
Select output capacitor COUT fulfilling the following condition including scattering and margin.

$$C_{OUT} < \frac{I_{OCP} \times T_{SS}}{V_{OUT}} \ [F]$$

Where:
I_{OCP} is switch current restricted value (= 6.5A [min])
T_{SS} is soft start time (= 0.5ms [min])

Caution: Concerning C_{OUT} total the capacity value of every part connected to Output line.

2. Output Voltage Setting

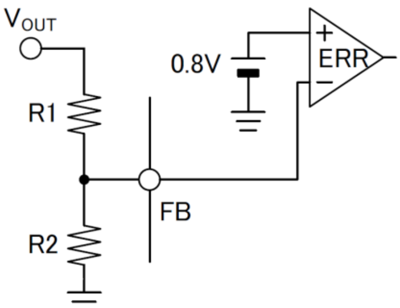


Fig15: Feedback Resistor Circuit

The output voltage value can be set by the feedback resistance ratio.

$$\mathbf{V_{OUT}} = \frac{\mathbf{R1 \times R2}}{\mathbf{R2}} \times \mathbf{0.8} \ [\mathbf{V}]$$

V_{OUT} has restriction with V_{IN} by the following equation
V_{OUTMin}: 0.075 × VIN ≥ 0.8V
V_{OUTMax}: 0.7 × VIN

3. Phase Compensation Component

A current mode control buck DC/DC converter is a two-pole, one-zero system. Two poles are formed by an error amplifier and load and the one zero point is added by phase compensation. The phase compensation resistor R_{CMP} determines the crossover frequency F_{CRS} where the total loop gain of the DC/DC converter is 0dB. A high value crossover frequency F_{CRS} provides a good load transient response characteristic but inferior stability. Conversely, a low value crossover frequency F_{CRS} greatly stabilizes the characteristics but the load transient response characteristic is impaired. Here, select the constant so that the crossover frequency F_{CRS} will be 1/10 of the switching frequency.

(1) Selection of Phase Compensation Resistor R_{CMP}

The Phase Compensation Resistance R_{CMP} can be determined by using the following equation.

$$\mathbf{R_{CMP}} = \frac{\mathbf{2\pi \times V_{OUT} \times F_{CRS} \times C_{OUT}}}{\mathbf{V_{FB} \times G_{MP} \times G_{MA}}}\ [\mathbf{\Omega}]$$

V_{OUT} is Output Voltage
F_{CRS} is Crossover Frequency
C_{OUT} is Output Capacitance
V_{FB} is Feedback Reference Voltage (0.8V Typ.)
G_{MP} is Current Sense Gain (6.8A/V Typ.)
G_{MA} is Error Amplifier Trans conductance (400µA/V Typ.)

(2) Selection of Phase Compensation Capacitance C_{CMP}

The phase compensation capacitance C_{CMP} can be determined by using the following equation.

$$C_{CMP} = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_{CMP}}\ [F]$$

(3) Loop Stability

To ensure the stability of the DC/DC converter, make sure that a sufficient phase margin is provided. A phase margin of at least 45º in the worst conditions is recommended.

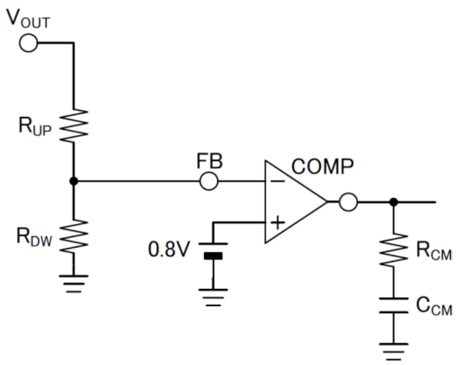


Fig 16: Phase Compensation Circuit

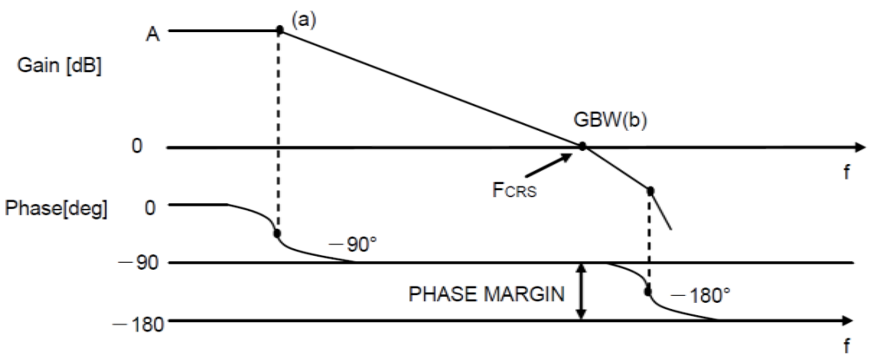


Fig 17: Bode Plot

- **Evaluation Board BOM**

Below is a table with the build of materials. Part numbers and supplier references are provided.

Item	Qty.	Ref	Description	Manufacturer	Part Number
1	1	C1	CAP CER 0.1UF 25V 10% X7R 0603	Murata	GRM188R71E104KA01D
2	1	C2	CAP CER 10UF 25V 20% X5R 1206	Murata	GRM31CR61E106MA12L
3	2	C3,C4	CAP CER 22UF 16V 10% X5R 1206	Murata	GRM31CR61C226KE15K
4	1	C6	CAP CER 1500PF 50V 10% X7R 0603	Murata	GRM188R71H152KA01D
5	1	D2	TVS DIODE 16VWM 26VC SMA	Littelfuse Inc	SMAJ16A
6	1	J1	CONN HEADER VERT .100 3POS 15AU	TE Connectivity Div	87224-3
7	1	L1	INDUCTOR 3.3UH 6.8A 20% SMD	TDK Corporation	SPM6530T-3R3M
8	1	R1	RES 20K OHM 1/10W 1% 0603 SMD	Rohm	TRR03EZPF2002
9	1	R2	RES 7.5K OHM 1/10W 1% 0603 SMD	Rohm	MCR03ERTF7501
10	1	R3	RES 2.4K OHM 1/10W 1% 0603 SMD	Rohm	MCR03ERTF2401
11	2	TP1,TP3	TEST POINT PC MULTI PURPOSE RED	Keystone Electronics	5010
12	2	TP2,TP4	TEST POINT PC MULTI PURPOSE BLK	Keystone Electronics	5011
13	1	U1	4.5V to 18V Input, 6.0A Integrated MOSFET 1ch Synchronous Buck DC/DC Converter	ROHM	BD9C601EFJ
14	1	ZX1	1806 footprint solder-short during assembly		
15	1		Shunt jumper for header J1 (item #6), CONN SHUNT 2POS GOLD W/HANDLE	TE Connectivity	881545-1

Thank you for your accessing to ROHM product information.
More detail product information and catalogs are available, please contact us.

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