ROHM Switching Regulator Solutions

# Evaluation Board: Synchronous Buck Converter Integrated FET

## BD9E151NUX-E2EVK-101 (5.0V | 1.2A Output)

No.000000000

- **Introduction**

  This application note will provide the steps necessary to operate and evaluate ROHM's synchronous buck DC/DC converter using the BD9E151NUX evaluation boards. Component selection, board layout recommendations, operation procedures and application data is provided.

- **Description**

  This evaluation board has been developed for ROHM's synchronous buck DC/DC converter customers evaluating BD9E151NUX. While accepting a power supply of 6.0-28.0V, an output of 1.0V to 23.0V can be produced. The IC has internal 80mOhm high-side MOSFET and a operation frequency fixed to 600 kHz. A fixed Soft Start circuit prevents in-rush current during startup along with UVLO (low voltage error prevention circuit) and TSD (thermal shutdown detection) protection circuits. An EN pin allows for simple ON/OFF control of the IC to reduce standby current consumption.

- **Applications**

  Surveillance Camera Applications
  OA Applications
  12V, 24V Distributed Power Systems

- **Evaluation Board Operating Limits and Absolute Maximum Ratings**

| Parameter | | Symbol | Limit | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | |
| **Supply Voltage** | | | | | | | |
| | BD9E151NUX | $V_{CC}$ | 6.0 | - | 28.0 | V | |
| **Output Voltage / Current** | | | | | | | |
| | BD9E151NUX | $V_{OUT}$ | 1.0(*2) | - | VINx0.7 or VIN-5 | V | * Set by R1 and R2 |
| | | $I_{OUT}$ | - | - | 1.2 | A | |

(*2)Restricted by minimum on pulse typ. 100nsec

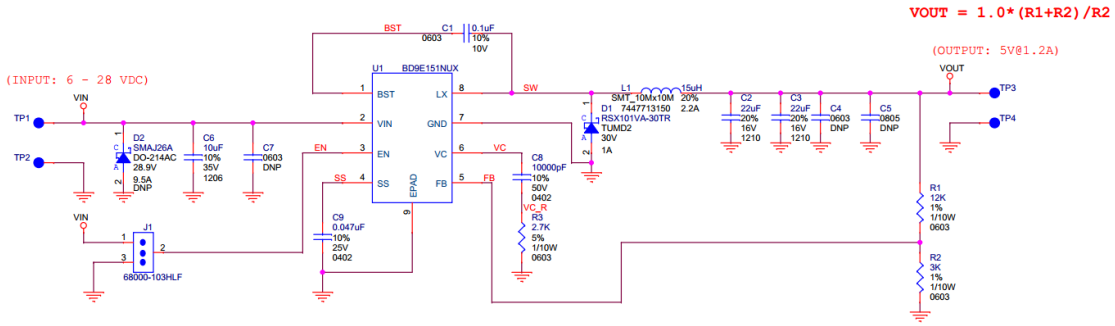
- **Evaluation Board**

  Below is evaluation board with the BD9E151NUX.


**Fig 1: BD9E151NUX Evaluation Board**

- **Evaluation Board Schematic**

  Below is evaluation board schematic for BD9E151NUX.




| BD9E151NUX-E2EVK-101 Jumper Positions | | |
|---|---|---|
| Reference Designator | Position | Description |
| J1 | 2 - 1 | Enable U1 |
| | 2 - 3 | Disable U1 |

Note:
1. 1V =< VOUT =< 0.7*VIN Or VIN-5

**Fig 2: BD9E151NUX Evaluation Board Schematic**

- **Evaluation Board I/O**

  Below is reference application circuit that shows the inputs ($V_{IN}$, EN) and the output ($V_{OUT}$).

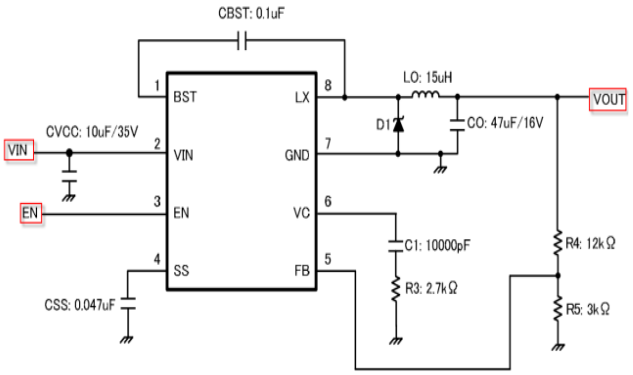



**Fig 3: BD9E151NUX Evaluation Board I/O**

- **Evaluation Board Operation Procedures**

  Below is the procedure to operate the evaluation board.

  1. Connect power supply's GND terminal to GND test point TP2 on the evaluation board.
  2. Connect power supply's $V_{CC}$ terminal to $V_{IN}$ test point TP1 on the evaluation board. This will provide $V_{IN}$ to the IC U1. Please note that the $V_{CC}$ should be in range of 6V to 28V.
  3. Check if shunt jumper of J1 is at position ON (Pin2 connect to Pin1, EN pin of IC U1 is pulled high).
  4. Connect electronic load to TP3 and TP4. Do not turn on load.
  5. Turn on power supply. The output voltage $V_{OUT}$ (+5V) can be measured at the test point TP3. Now turn on the load. The load can be increased up to 1.2A MAX.

  ***Notes***:

  *The board does not support hot plugging protection. Please do not hot plug power supply.*

- **Reference Application Data for BD9E151NUX-E2EVK-101**

  Following graphs show quiescent current, efficiency, load response, output voltage ripple response of the BD9E151NUX evaluation board.

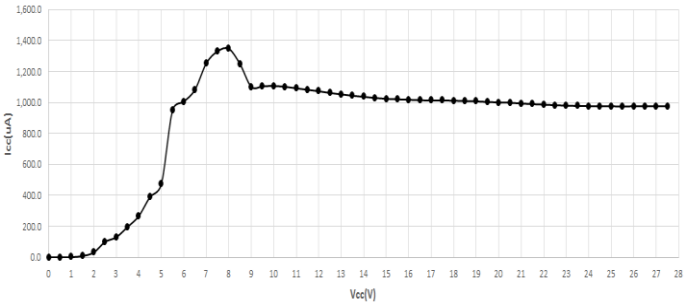



**Fig 4: Circuit Current vs. Power supply Voltage Characteristics ($V_{IN}$ = 0-28V, Temp=25ºC)**

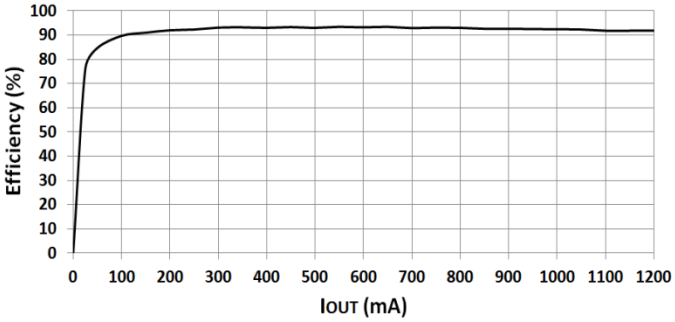



**Fig 5: Electric Power Conversion Rate ($V_{in}$=12V, $V_{OUT}$=5V)**

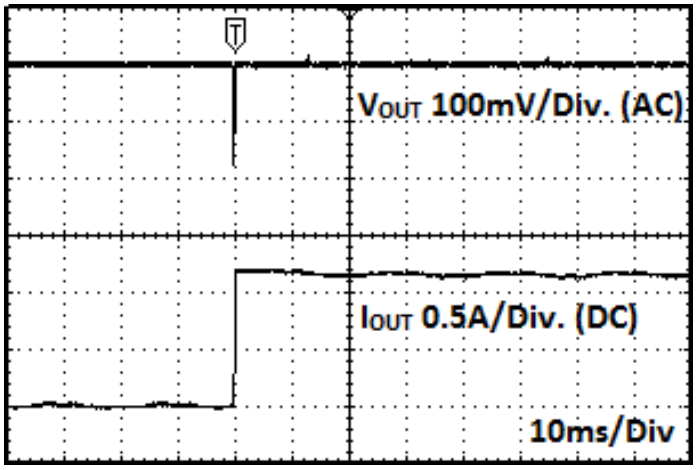



**Fig 6: Load Response Characteristics ($V_{IN}$=12V, $V_{OUT}$=5V, $I_{OUT}$=0A → 1.2A)**

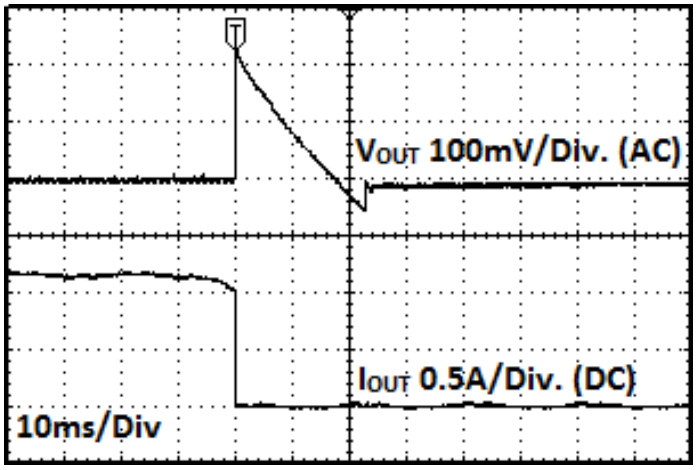



**Fig 7: Load Response Characteristics ($V_{IN}$ =12V, $V_{OUT}$ =5V, $I_{OUT}$ =1.2A → 0A)**

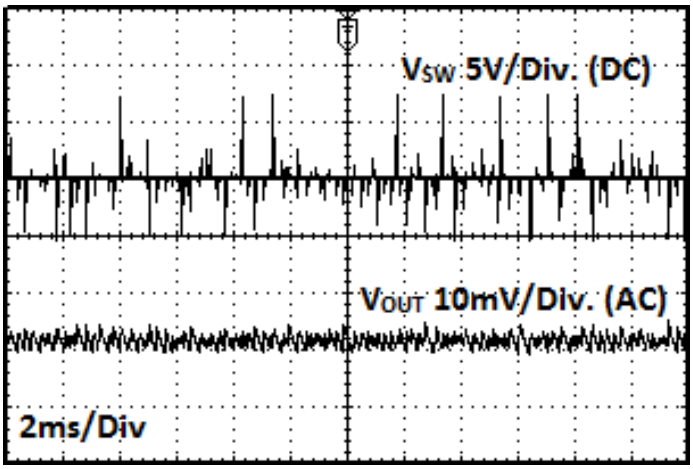



**Fig 8: Output Voltage Ripple Response Characteristics ($V_{IN}$=12V, $V_{OUT}$=5V, $I_{OUT}$=0A)**

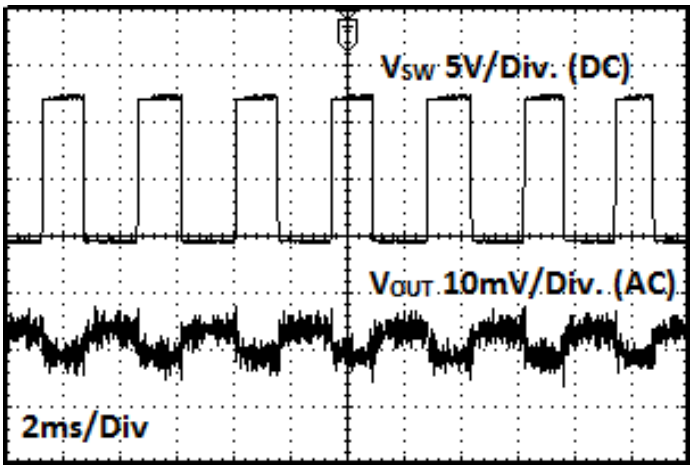



**Fig 9: Output Voltage Ripple Response Characteristics ($V_{IN}$=12V, $V_{OUT}$=5V, $I_{OUT}$=1.2A)**

- **Evaluation Board Layout Guidelines**

  Below are the guidelines that have been followed and recommended for BD9E151NUX designs.

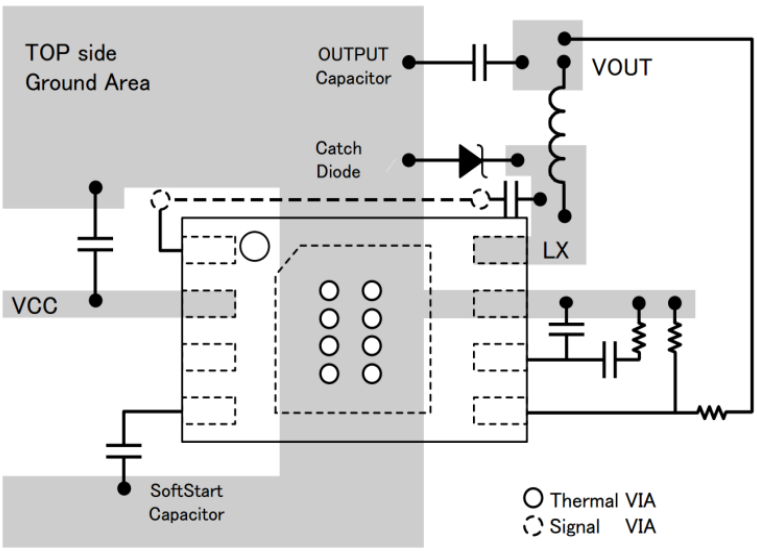



**Fig 10: BD9E151NUX PCB Layout**

Layout is a critical portion of good power supply design. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the $V_{IN}$ pin should be bypassed to ground with a low ESR ceramic bypass capacitor with B dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the $V_{IN}$ pin, and the anode of the catch diode. See Fig 10 for a PCB layout example.

In the BD9E151NUX, since the LX connection is the switching node, the catch diode and output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. And GND area should not be connected directly power GND, connected avoiding the high current switch paths. The additional external components can be placed approximately as shown.

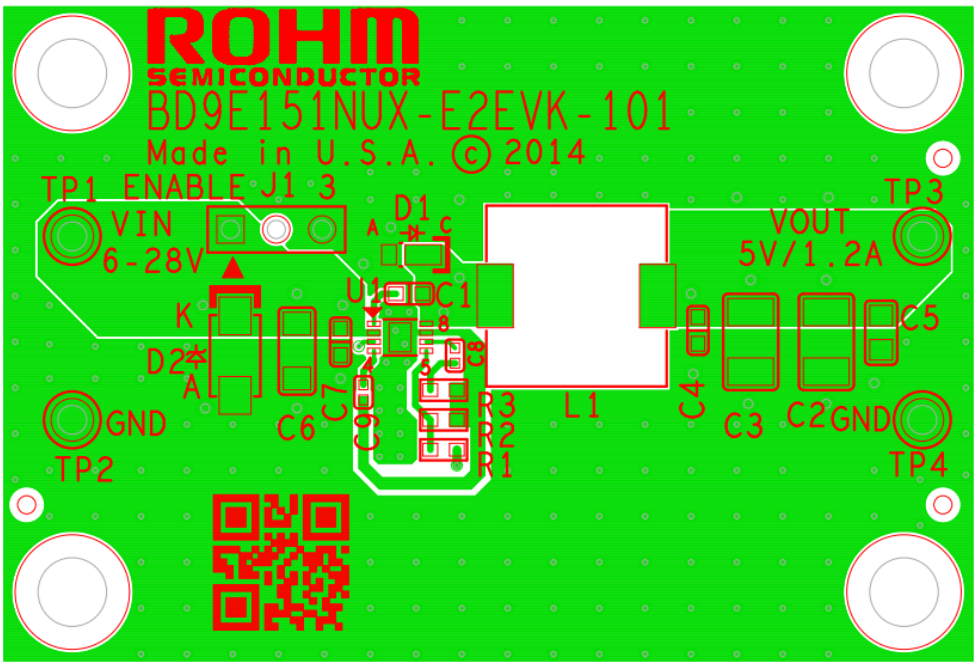



**Fig 11: BD9E151NUX-E2EVK-101 Board PCB layout**

- **Calculation of Application Circuit Components**

**(1) Inductors**

Something of the shield type that fulfills the current rating (Current value Ipecac below), with low DCR is recommended. Value of Inductance influences
Inductor Ripple Current and becomes the cause of Output Ripple.
In the same way as the formula below, this Ripple Current can be made small for as big as the L value of Coil or as high as the Switching Frequency.

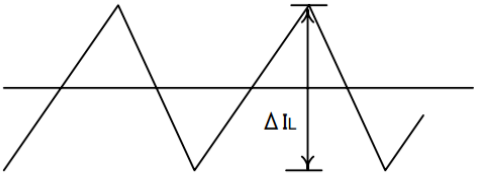



**Fig 12: Inductor Current**

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad \ldots (1)$$

$$\Delta I_L = \frac{V_{IN} - V_{out}}{L} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f} \quad \ldots (2)$$

($\Delta I_L$: Output Ripple Current, $V_{IN}$: Input Voltage, $V_{OUT}$: Output Voltage, f: Switching Frequency)
For design value of Inductor Ripple Current, please carry out design tentatively with about 20%～50% of Maximum Input Current

**(2) Output Capacitor**

In order for capacitor to be used in output to reduce output ripple, Low ceramic capacitor of ESR is recommended. Also, for capacitor rating, on top of putting into consideration DC Bias characteristics, please use something whose maximum rating has sufficient margin with respect to the Output Voltage. Output ripple voltage is looked for using the following formula. The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the crossover frequency of the design and LC corner frequency of the output filter. In general, it is desirable to keep the crossover frequency at less than 1/5 of the switching frequency. With high switching frequencies such as the 600kHz frequency of this design, internal circuit limitations of the BD9E151NUX limit the practical maximum crossover frequency to about 30kHz. In general, the crossover frequency should be higher than the corner frequency determined by the load impedance and the output capacitor. This limits the minimum capacitor value for the output filter to:

$$C_{OUT\_min} = \frac{1}{2\pi \times R_l \times f_{c\_max}} \quad \ldots (3)$$

Where: $R_l$ is the output load resistance and $f_{c\_max}$ is the maximum crossover frequency. The output ripple voltage can be estimated by:

$$V_{PP} = \Delta I_L \times \frac{1}{2\pi \times f \times C_{OUT}} + \Delta I_L \times R_{ESR} \ldots (4)$$

Please design in a way that it is held within Capacity Ripple Voltage.
In the BD9E151NUX, it is recommended a ceramic capacitor more than 10μF.

**(3) Output Voltage Setting**

ERROR AMP internal Standard Voltage is 1.0V. Output Voltage is determined as seen in (5) formula

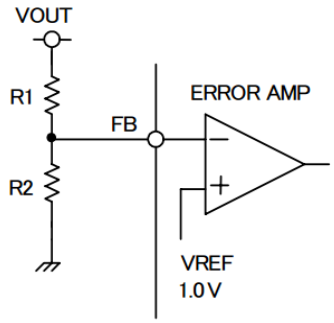



**Fig 13: Output Voltage Setting**

$$V_{OUT} = \frac{R1 + R2}{R2} \quad \ldots (5)$$

**(4) Bootstrap Capacitor**

Please connect from 0.047μF to 0.47μF (Laminate Ceramic Capacitor) between BST Pin and LX Pin.

**(5) Soft Start Function**

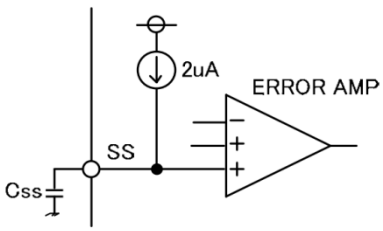



**Fig 14: Soft Start Time Setting**

It is highly recommended to program the soft start time externally to prevent high inrush current because no soft start time is implemented internally. A capacitor (Css) connected between the SS pin and ground implements a soft start time.The BD9E151NUX has an internal pull-up current source of 2uA that charges the external soft start capacitor. The equation for the soft start time (10% to 90%) is shown in below Equation.
The $I_{ss}$ current is 2uA.

$$\mathbf{T_{SS}} = \frac{\mathbf{C_{ss}} \times 0.1}{\mathbf{I_{ss}}} \ldots (6)$$

**(6) Catch Diode**

The BD9E151NUX is designed to operate using an external catch diode between LX and GND. The selected diode must meet the absolute maximum ratings for the application: Reverse voltage must be higher than the maximum voltage at the LX pin, which is $V_{INMAX}$ + 0.5 V. Peak current must be greater than $I_{OUTMAX}+\Delta I_L$ plus on half the peak to peak inductor current. Forward voltage drop should be small for higher efficiencies. It is important to note that the catch diode conduction time is typically longer than the high-side FET on time, so attention paid to diode parameters can make a marked improvement in overall efficiency. Additionally, check that the device chosen is capable of dissipating the power losses.

**(7) Input Capacitor**

The BD9E151NUX requires an input capacitor and depending on the application. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but low-ESR electrolytic capacitors may also suffice. The typical recommended value for the decoupling capacitor is 10uF. Please place this capacitor as possible as close to the $V_{IN}$ pin. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta_{\mathbf{VCC}} = \frac{\mathbf{I_{OUT}}}{\mathbf{f} \times \mathbf{C_{VCC}}} \times \frac{\mathbf{V_{OUT}}}{\mathbf{V_{CC}}} \times \left[\mathbf{1} - \frac{\mathbf{V_{OUT}}}{\mathbf{V_{CC}}}\right] \ldots (7)$$

Since the input capacitor ($C_{VIN}$) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$\mathbf{I_{CVCC}} = \mathbf{I_{OUT}} \times \sqrt{\frac{\mathbf{V_{OUT}}}{\mathbf{V_{CC}}} \times \left(\mathbf{1} - \frac{\mathbf{V_{OUT}}}{\mathbf{V_{CC}}}\right)} \ldots (8)$$

The worst case condition occurs at $V_{IN}$= 2$V_{OUT}$, where

$$\mathbf{I_{CVCC\_max}} = \frac{\mathbf{I_{OUT}}}{\mathbf{2}} \ldots (9)$$

**(8) About Adjustment of DC/DC Comparator Frequency Characteristics**

Role of Phase compensation element C1, C2, R3 (See Fig 3 Example of Reference Application Circuit)
Stability and Responsiveness of Loop are controlled through VC Pin which is the output of Error Amp.
The combination of zero and pole that determines Stability and Responsiveness is adjusted by the combination of resistor and capacitor that are connected in series to the VC Pin.
DC Gain of Voltage Return Loop can be calculated for using the following formula.

$$\mathbf{A_{dc}} = \mathbf{R_l} \times \mathbf{G_{CS}} \times \mathbf{A_{EA}} \times \frac{\mathbf{V_{FB}}}{\mathbf{Vout}} \ldots (10)$$

Here, $V_{FB}$ is Feedback Voltage (1.0V).$A_{EA}$ is Voltage Gain of Error amplifier (typ : 60 dB),
Gcs is the Trans-conductance of Current Detect (typ : 10A/V),and $R_l$ is the Output Load Resistance value.

There are 2 important poles in the Control Loop of this DC/DC.
The first occurs with through the output resistance of Phase compensation Capacitor (C1)and Error amplifier.
The other one occurs with through the Output Capacitor and Load Resistor.
These poles appear in the frequency written below.

$$\mathbf{f_{p1}} = \frac{\mathbf{G_{EA}}}{\mathbf{2\pi \times C1 \times A_{EA}}} \ \ldots(11)$$

$$\mathbf{f_{p2}} = \frac{\mathbf{1}}{\mathbf{2\pi \times C_{OUT} \times R_l}} \ \ldots(12)$$

Here, $G_{EA}$ is the trans-conductance of Error amplifier (typ : 250uA/V).

Here, in this Control Loop, one zero becomes important.
With the zero which occurs because of Phase compensation Capacitor C1 and Phase compensation Resistor R3, the Frequency below appears.

$$\mathbf{f_{z1}} = \frac{\mathbf{1}}{\mathbf{2\pi \times C1 \times R3}} \ \ldots(13)$$

Also, if Output Capacitor is big, and that ESR ($R_{ESR}$) is big, in this Control Loop, there are cases when it has an important, separate zero (ESR zero).
This ESR zero occurs due to ESR of Output Capacitor and Capacitance, and exists in the Frequency below.

$$\mathbf{fz_{ESR}} = \frac{1}{\mathbf{2\pi \times C_{OUT} \times R_{ESR}}} \ \ldots(14) \qquad \text{(ESR zero)}$$

In this case, the 3Rd pole determined with the 2nd Phase compensation Capacitor (C2) and Phase Correction Resistor (R3) is used in order to correct the ESR zero results in Loop Gain.
This pole exists in the frequency shown below.

$$\mathbf{f_{p3}} = \frac{\mathbf{1}}{\mathbf{2\pi \times C2 \times R3}} \ \ldots(15) \qquad \text{(pole that corrects ESR zero)}$$

The target of Phase compensation design is to create a communication function in order to acquire necessary band and Phase margin.

Cross-over Frequency (band) at which Loop gain of Return Loop becomes “0” is important.
When Cross-over Frequency becomes low, Power supply Fluctuation Response, Load Response, etc worsens.
On the other hand, when Cross-over Frequency is too high, instability of the Loop can occur.
Tentatively, Cross-over Frequency is targeted to be made 1/20 or below of Switching Frequency. Selection method of Phase Compensation constant is shown below.

1. Phase Compensation Resistor ($R_3$) is selected in order to set to the desired Cross-over Frequency.

Calculation of RC is done using the formula below.

$$\mathbf{R3} = \frac{\mathbf{2\pi \times C_{OUT} \times f_c}}{\mathbf{G_{EA} \times G_{CS}}} \times \frac{\mathbf{V_{OUT}}}{\boldsymbol{V_{FB}}} \ \ldots(16)$$

Here, $f_c$ is the desired Cross-over Frequency. It is made about 1/20 and below of the Normal Switching Frequency ($f_s$).

2. Phase compensation Capacitor (C1) is selected in order to achieve the desired phase margin.

In an application that has a representative Inductance value (about several 10uH～22uH), by matching zero of compensation to 1/4 and below of the Cross-over Frequency, sufficient Phase margin can be acquired. C1 can be calculated using the following formula.

$$\mathbf{C1} > \frac{\mathbf{4}}{\mathbf{2\pi \times R3 \times f_c}} \ \ldots(17)$$

$R_C$ is Phase compensation Resistor.

3. Examination whether the second Phase compensation Capacitor C2 is necessary or not is done.

If the ESR zero of Output Capacitor exists in a place that is smaller than half of the Switching Frequency, a second Phase compensation Capacitor is necessary. In other words, it is the case wherein the formula below happens.

$$\frac{\mathbf{1}}{\mathbf{2\pi \times C_{OUT} \times R_{ERS}}} < \frac{\mathbf{f_s}}{\mathbf{2}} \ \ldots(18)$$

In this case, add the second Phase compensation Capacitor C2, and match the frequency of the third pole to the Frequency $f_{p3}$ of ESR zero.

C2 is looked for using the following formula.

$$\mathbf{C2} = \frac{\mathbf{C_{OUT} \times R_{ERS}}}{\mathbf{R3}} \quad \ldots (19)$$

**Output Voltage Restriction**

BD9E151NUX have a function of BSTUVLO to prevent malfunction at low voltage between BST and LX. Therefore OUTPUT voltage is restricted by BSTUVLO and Max Duty Cycle (min 85%).

① Restriction by BST-UVLO

When the voltage between BST and Lx is lower than 2.5V, High-Side FET will be made turned off and the charge will provide from $V_{IN}$ to BST directly to reset BSTUVLO (path①). The below formula is needed to be satisfied to reset BSTUVLO.

$$\mathbf{V_{IN}} \geq \mathbf{V_{IN}} + \mathbf{V_F} + \mathbf{BSTUVLO\ reset} \quad \ldots (20)$$

Here, BSTUVLO reset: BSTUVLO reset voltage, $V_F$: the diode forward bias voltage between $V_{IN}$ and BST
Considering the fluctuation of BSTUVLO reset voltage and $V_F$, maximum voltage is more than 5V.
Therefore maximum output voltage is defined as $V_{IN}$ - 5V.

②Restriction by Max Duty Cycle

Maximum output voltage is restricted by Max Duty Cycle (min 85%).
In this time it is needed to consider the effect of NchFET Ron
, OUTPUT current and forward voltage of SBD. OUTPUT voltage
can be calculated using the following formula.

$$\mathbf{V_{OUT\_max}} = (\mathbf{V_{IN}} - \mathbf{R_{ON}} \times \mathbf{I_{OUT}}) \times \mathbf{0.85} - \mathbf{V_F} \times \mathbf{0.15} \quad \ldots (21)$$

Considering the effect of catch diode type and the loss by inductor,
$V_{omax} = (V_{IN}\text{-}R_{on} \times I_{omax}) \times 0.85$ (casually formula)
Considering the negative voltage in the case of pulling diode current,
maximum voltage is more than $V_{IN} \times 0.7$.
Therefore maximum output voltage is defined as $V_{IN} \times 0.7$.

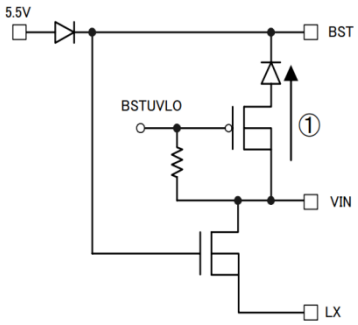



**Fig 15: BST charge pass**

Considering above restriction, adopt the lower output voltage as maximum voltage

- **Evaluation Board BOM**
  Below is a table with the build of materials. Part numbers and supplier references are provided.

| Item | Qty. | Ref | Description | Manufacturer | Part Number |
|---|---|---|---|---|---|
| 1 | 1 | C1 | CAP CER 0.1UF 16V 10% X7R 0603 | Murata | GRM188R71C104KA01D |
| 2 | 2 | C2,C3 | CAP CER 22UF 16V 20% X7R 1210 | Murata | GRM32ER71C226MEA8 |
| 3 | 1 | C6 | CAP CER 10UF 35V 10% X5R 1206 | Murata | GRM31CR6YA106KA12L |
| 4 | 1 | C8 | CAP CER 10000PF 50V 10% X7R 0402 | Murata | GRM155R71H103KA88D |
| 5 | 1 | C9 | CAP CER 0.047UF 25V 10% X7R 0402 | Murata | GRM155R71E473KA88D |
| 6 | 1 | D1 | DIODE SCHOTTKY 30V 1A 2TUMD | ROHM | RSX101VA-30TR |
| 7 | 1 | J1 | CONN HEADER VERT .100 3POS 15AU | FCI | 68000-103HLF |
| 8 | 1 | L1 | INDUCTOR POWER 15UH 2.2A SMD | Wurth Electronics | 7447713150 |
| 9 | 1 | R1 | RES 12K OHM 1/10W 1% 0603 SMD | ROHM | MCR03ERTF1202 |
| 10 | 1 | R2 | RES 3K OHM 1/10W 1% 0603 SMD | ROHM | MCR03ERTF3001 |
| 11 | 1 | R3 | RES 2.7K OHM 1/10W 1% 0603 SMD | ROHM | MCR03ERTF2701 |
| 12 | 2 | TP1,TP3 | TEST POINT PC MULTI PURPOSE RED | Keystone Electronics | 5010 |
| 13 | 2 | TP2,TP4 | TEST POINT PC MULTI PURPOSE BLK | Keystone Electronics | 5011 |
| 14 | 1 | U1 | IC REG BUCK ADJ 1.2A 8VSON | ROHM | BD9E151NUX-TR |
| 15 | 1 | | Shunt jumper for header J1 (item #8), CONN SHUNT 2POS GOLD W/HANDLE | TE Connectivity | 881545-1 |

## Notes



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Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

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ROHM SEMICONDUCTOR

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