ROHM Switching Regulator Solutions

Evaluation Board: High Voltage 3A Buck Converter With Integrated FET

BD9G341AEFJ-EVK-101 (5V | 3A Output) AED58-D1-0007

- **Introduction**

  This application note will provide the steps necessary to operate and evaluate ROHM's non-synchronous buck DC/DC converter using the BD9G341AEFJ evaluation boards. Component selection, board layout recommendations, operation procedures and application data is provided.

- **Description**

  This evaluation board has been developed for ROHM's non-synchronous buck DC/DC converter customers evaluating BD9G341AEFJ. While the BD9G341AEFJ accepts a power supply input range of 12V to 76V, and generates output voltages from 1V to Vcc, this evaluation board is setup for the same input voltage range and a fixed output of 5V can be produced. The IC has internal 150mΩ N-channel MOSFET and the operating frequency is programmable from 50kHz to 750kHz. A fixed Soft Start circuit prevents inrush current during startup along with UVLO (low voltage error prevention circuit) and TSD (thermal shutdown detection), OCP (over current protection), OVP (over voltage protection) protection circuits. The under voltage lockout and hysteresis can be set by external resistor using EN pin. An EN pin allows for simple ON/OFF control of the IC to reduce standby current consumption.

- **Applications**

  Industrial distributed power applications.
  Automotive application.
  Battery powered equipment.

- **Evaluation Board Operating Limits and Absolute Maximum Ratings**

Parameter		Symbol	Limit			Unit	Conditions
			MIN	TYP	MAX		
Supply Voltage							
	BD9G341AEFJ	V_{CC}	12	-	76	V	
Output Voltage / Current							
	BD9G341AEFJ	V_{OUT}	-	5	-	V	R5
		I_{OUT}	-	-	3	A	

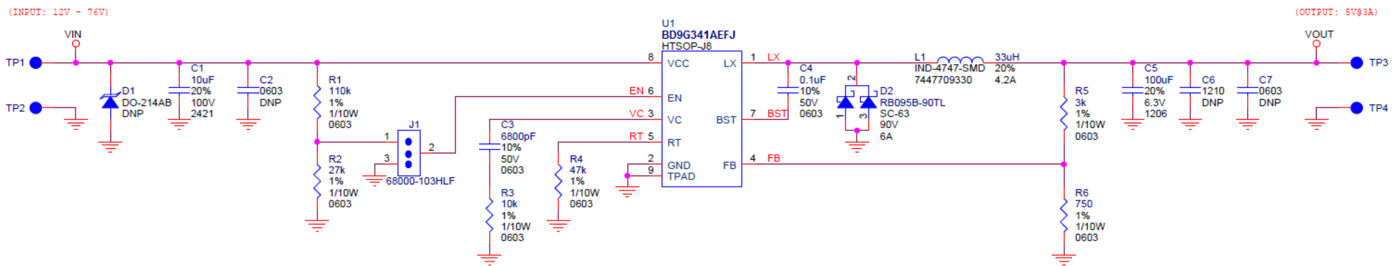
- **Evaluation Board**

  Below is evaluation board with the BD9G341AEFJ.

Fig 1: BD9G341AEFJ Evaluation Board

● Evaluation Board Schematic

Below is evaluation board schematic for BD9G341AEFJ.



BD9G341AEFJ EVM Jumper Positions

VOUT = (R5+R6)/R6

Reference Designator	Position	Description
J1	Open	Configure U1 fully operational
	2 - 1	
	2 - 3	Configure U1 in low power state

Fig 2: BD9G341AEFJ Evaluation Board Schematic

● Evaluation Board I/O

Below is reference application circuit that shows the inputs (V_{IN} and EN) and the output (V_{OUT}).

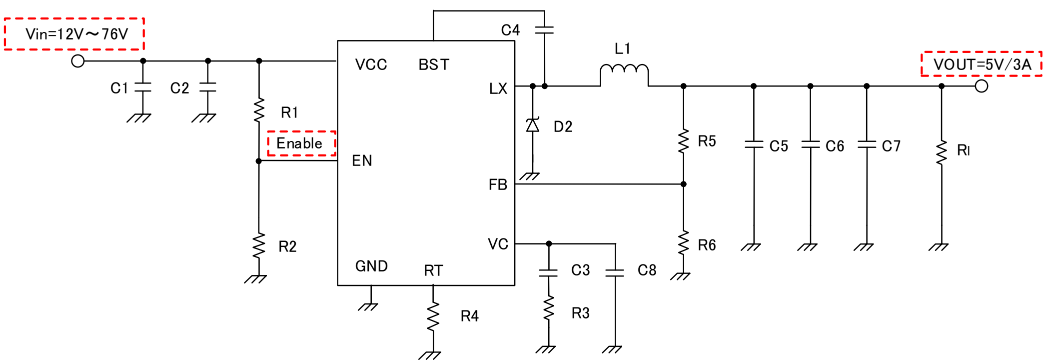


Fig 3: BD9G341AEFJ Evaluation Board I/O

● Evaluation Board Operation Procedures

Below is the procedure to operate the evaluation board.

1. Connect power supply's GND terminal to GND test point TP2 on the evaluation board.
2. Connect power supply's V_{CC} terminal to V_{IN} test point TP1 on the evaluation board. This will provide V_{IN} to the IC U1. Please note that the V_{CC} should be in range of 12V to 76V.
3. Check if shunt jumper of J1 is at position ON (Pin2 connect to Pin1, EN pin of IC U1 is pulled high).
4. Connect electronic load to TP3 and TP4. Do not turn on load (electronic load is off power).
5. Turn on power supply. The output voltage V_{OUT}(+5V) can be measured at the test point TP3. Now turn on the load. The load can be increased up to 3A MAX.

Notes:
The board does not support hot plugging protection. Do not perform hot plugging on this board.

- **Reference Application Data for BD9G341AEFJ-EVK-101**
  Following graphs show quiescent current, efficiency, load response, output voltage ripple response of the BD9G341AEFJ evaluation board.

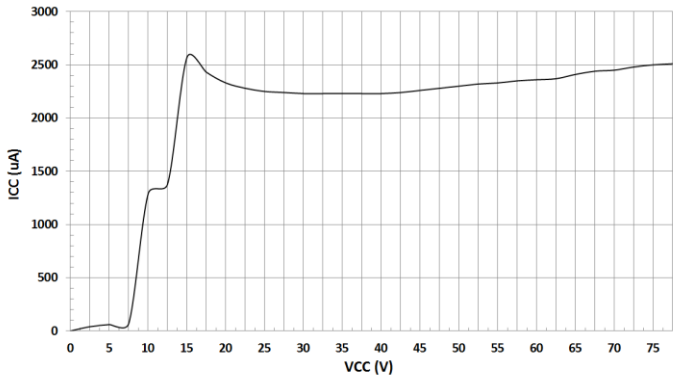


Fig 4: Circuit Current vs. Power supply Voltage Characteristics (Temp=25^{o}C)

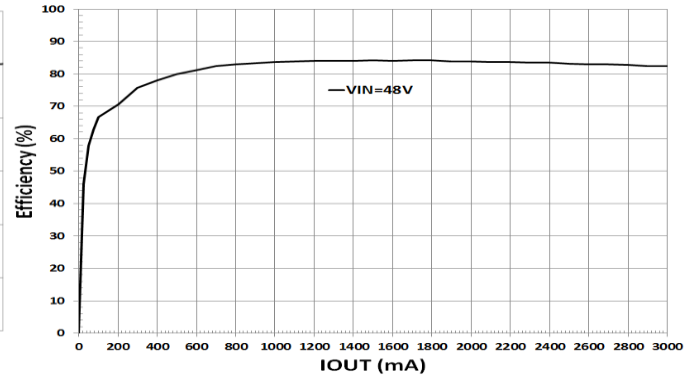


Fig 5: Electric Power Conversion Rate (V_{IN}=48V, V_{OUT}=5V)

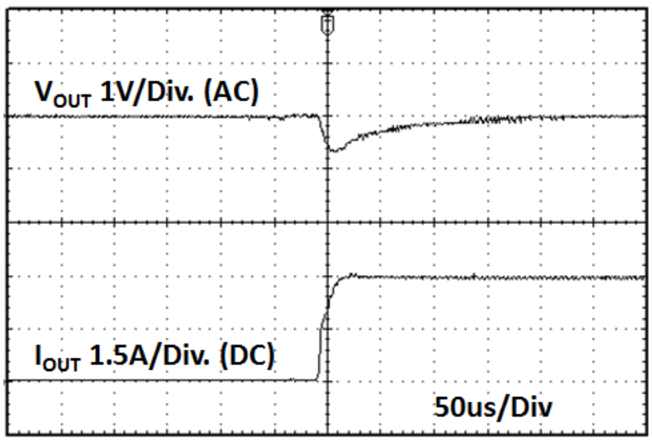


Fig 6: Load Response Characteristics (V_{IN}=48V, V_{OUT}=5V, I_{OUT}=0→3A)

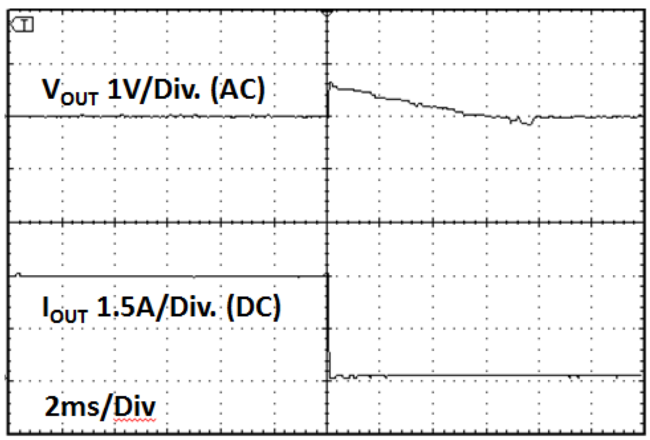


Fig 7: Load Response Characteristics (V_{IN}=48V, V_{OUT}=5V, I_{OUT}=3A→0A)

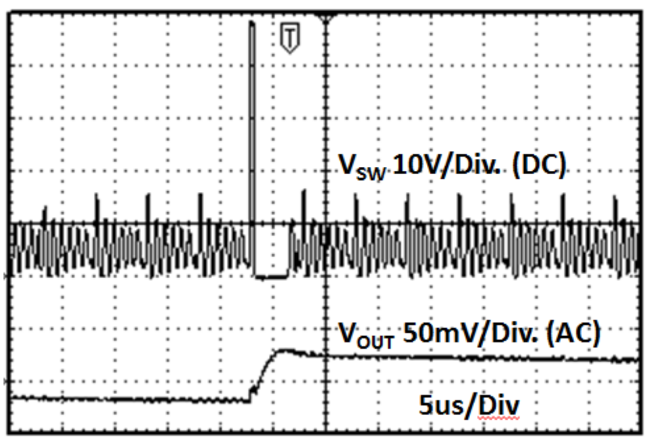


Fig 8: Output Voltage Ripple Response Characteristics (V_{IN}=48V, V_{OUT}=5V, I_{OUT}=0A)

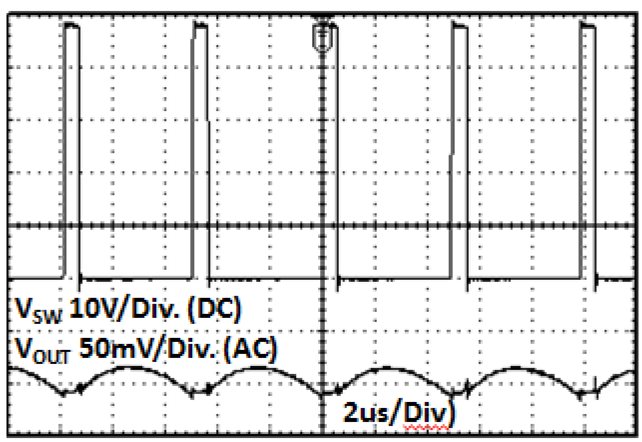
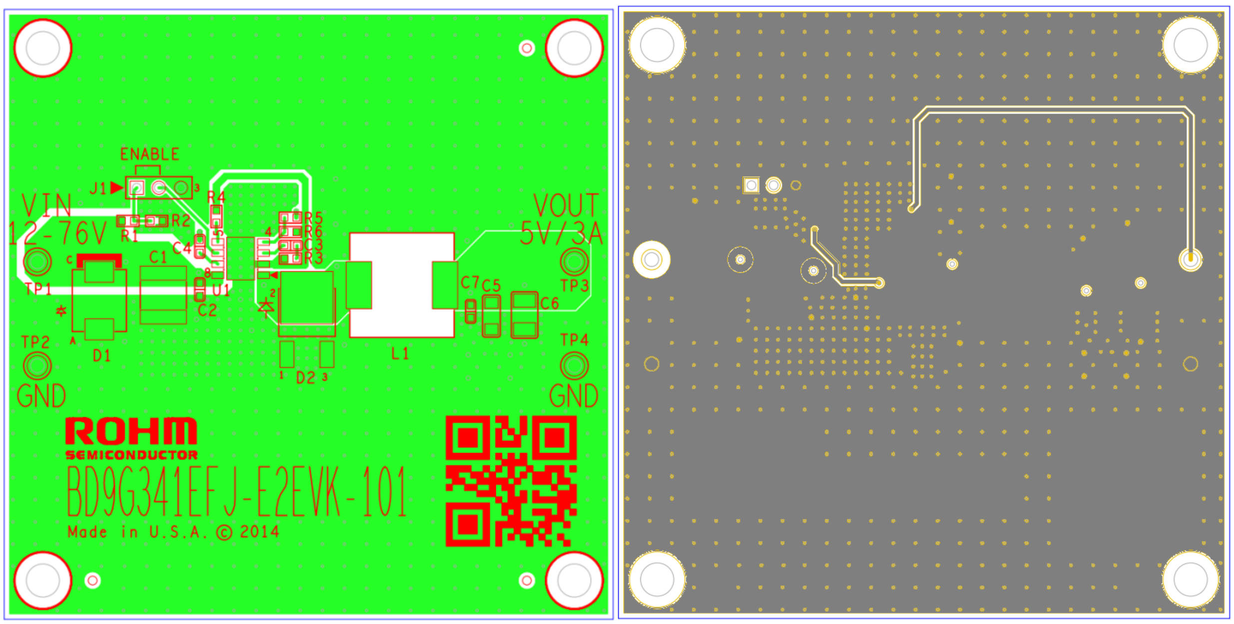


Fig 9: Output Voltage Ripple Response Characteristics (V_{IN}=48V, V_{OUT}=5V, I_{OUT}=3A)

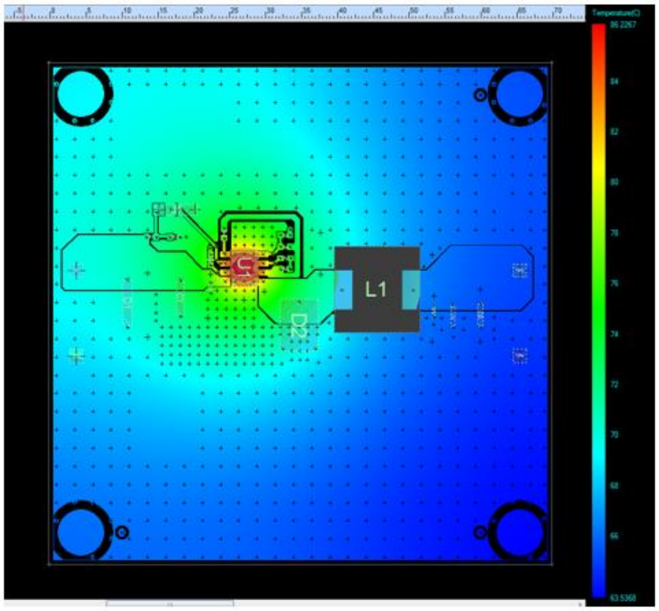
- **Evaluation Board Layout Guidelines**

Layout is a critical portion of good power supply design. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VCC pin should be bypassed to ground with a low ESR ceramic bypass capacitor with B dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VCC pin, and the anode of the catch diode. The GND pin should be tied directly to the thermal pad under the IC and the thermal pad. In order to reduce the influence of the impedance and L of the parasitic, the high current line is thick and short.
Input decoupling capacitor should be located as close to the VCC pins.
In order to minimize the parasitic capacitor and impedance of pattern, catch diode and inductance should be located as close to the Lx pin.
The thermal pad should be connected to any internal PCB ground planes using multiple VIAs directly under the IC.
GND feedback resistor, phase compensation element and RT resistor don't give the common impedance resistor against high current line…



Top Layer Bottom Layer

Fig 10: BD9G341AEFJ-E2EVK-101 and BD9G341AEFJ-EVK-101 Board PCB layout



U1: BD9G341AEFJ
- **Max. power dissipation: 3.825W @VIN=76V**
- **Component temperature = 86.2 ^{0}C**

L1: 7447709330
- **Max. power dissipation: 0.405W**
- **Component temperature = 70.4 ^{0}C**

Fig 11: BD9G341AEFJ-E2EVK-101 Thermal Characteristics at Temp=25^{o}C, No air flow, V_{IN}=76V, V_{OUT}=5V, I_{OUT}=3A. Thermal characteristics also apply to BD9G341AEFJ-EVK-101.

Thermal note: If the board is operated above room temperature (T>25^{o}C), an active cooling source (fan) or heat sink (soldered to bottom of PCB) need to be added.

Additional layout notes:

- The thermal Pad on the back side of IC has the great thermal conduction to the chip. So using the GND plane as broad and wide as possible can help thermal dissipation. And a lot of thermal via for helping the spread of heat to the different layer is also effective.
- The input capacitors should be connected to GND as close as possible to the VIN terminal.
- The inductor and the output capacitors should be placed close to SW pin as much as possible.
- For applications operating at or near maximum voltage conditions (76V max), additional precautions regarding heat dissipation need to be considered during board layout. The provided evaluation board is a 4-layer board meant for evaluation purposes only. At maximum conditions, the IC's internal thermal shutdown detection circuit will be potentially initiated and the output disabled until the junction temperature falls. For final designs operating near these conditions, we recommend using one of the below PCB options for better heat dissipation of the IC.

1) Use of a 4-layer PCB with internal GND planes connected to the IC GND pins.
2) Use of a 2-layer PCB with a heat sink attached to the IC package.
3) Use of a 2-layer PCB with a copper plane (>1oz) attached to the IC.

- **Calculation of Application Circuit Components**

1. Inductors

Something of the shield type that fulfills the current rating (Current value I_{peak} below), with low DCR is recommended.
Value of Inductance influences Inductor Ripple Current and becomes the cause of Output Ripple.
In the same way as the formula below, this Ripple Current can be made small for as big as the L value of Coil or as high as the Switching Frequency.

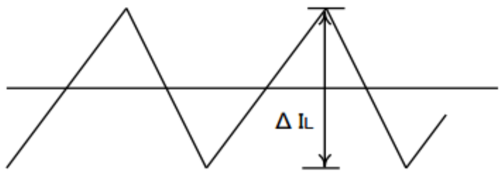


Fig 12: Inductor Current

$$\mathbf{I_{PEAK}} = \mathbf{I_{OUT}} + \frac{\Delta \mathbf{I_L}}{2} \ \ldots (1)$$

$$\Delta \mathbf{I_L} = \frac{\mathbf{V_{CC}} - \mathbf{V_{OUT}}}{\mathbf{L}} \times \frac{\mathbf{V_{OUT}}}{\mathbf{V_{CC}}} \times \frac{1}{\mathbf{f}} \ \ldots (2)$$

(ΔI_L: Output Ripple Current, V_{CC}: Input Voltage, V_{OUT}: Output Voltage, f: Switching Frequency)

For design value of Inductor Ripple Current, please carry out design tentatively with about 20%～50% of Maximum Input Current.
In the BD9G341AEFJ, it is recommended the below series of 4.7µH～33µH inductance value.
Recommended Inductor：SUMIDA CDRH127H Series

2. Output Capacitor

In order for capacitor to be used in output to reduce output ripple, Low ceramic capacitor of ESR is recommended.
Also, for capacitor rating, on top of putting into consideration DC Bias characteristics, please use something whose maximum rating has sufficient margin with respect to the Output Voltage.
Output ripple voltage is looked for using the following formula.

$$\mathbf{V_{PP}} = \Delta \mathbf{I_L} \times \frac{1}{2\pi \times \mathbf{f} \times \mathbf{C_{OUT}}} + \Delta \mathbf{I_L} \times \mathbf{R_{ESR}} \ldots (3)$$

Please design in a way that it is held within Capacity Ripple Voltage.
In the BD9G341AEFJ, it is recommended a ceramic capacitor over 10µF.

3. Output voltage setting

The internal reference voltage of ERROR AMP is 1.0V.

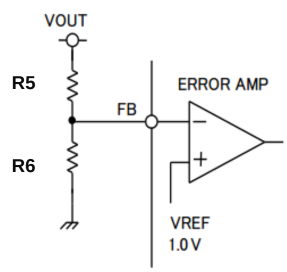


Fig 13: Output voltage setting

Output voltage is determined like (4) types

$$V_{OUT} = \frac{R5 + R6}{R6} \quad \ldots(4)$$

The available minimum output voltage is restricted by minimum duty shown as the following.
MinDuty = f ×MinOnTime (MinDuty : minimum duty, f : frequency, MinOnTime : minimum on time)
When the calculated voltage, VCC×MinDuty, is higher than 1V, the minimum output voltage is determined by VCC × MinDuty.

The available maximum output voltage is restricted by maximum duty shown as the following.
MaxDuty =1 - f × Toff_f (MaxDuty : maximum duty, Toff _f : Forced off time)
The available maximum output is shown as the following.
Maximum output voltage = VCC × MaxDuty – Iout ×Ron (Iout : load current, Ron : NMOS ON resistance)

4. Bootstrap Capacitor
Please connect from 0.1uF (Laminate Ceramic Capacitor) between BST Pin and Lx Pins.

5. Catch Diode
BD9G341AEFJ should be taken to connect external catch diode between Lx Pin and GND Pin. The diode require adherence to absolute maximum Ratings of application. Opposite direction voltage should be higher than maximum voltage of Lx Pin (V_{CCMAX} + 0.5V). The peak current is required to be higher than $I_{OUTMAX} + \Delta I_L$.

6. Input Capacitor
BD9G341AEFJ needs an input decoupling capacitor. It is recommended a low ceramic capacitor ESR over 4.7μF . Additionally, it should be located as close as possible.
Capacitor should be selected by maximum input voltage with input ripple voltage.
Input ripple voltage is calculated by using the following formula.

$$\Delta V_{CC} = \frac{I_{OUT}}{f \times C_{VCC}} \times \frac{V_{OUT}}{V_{CC}} \times \left[1 - \frac{V_{OUT}}{V_{CC}}\right] \quad \ldots(5)$$

C_{VCC}: Input capacitor
RMS ripple current is calculated by using the following formula.

$$I_{CVCC} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{CC}} \times \left(1 - \frac{V_{OUT}}{V_{CC}}\right)} \quad \ldots(6)$$

If $V_{CC}=2V_{OUT}$, RMS ripple current is maximum. That is determined by (9) .

$$I_{CVCC\_max} = \frac{I_{OUT}}{2} \quad \ldots(7)$$

7. About Adjustment of DC/DC Comparator Frequency Characteristics
Role of Phase compensation element C3, C8, R3.

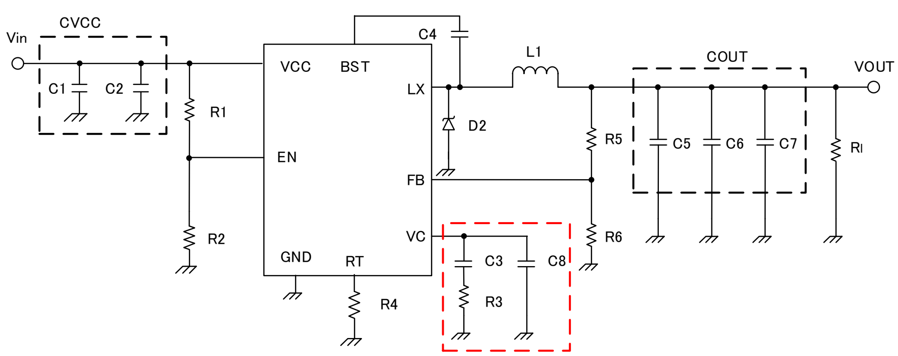


Fig 14: Feedback voltage resistance setting method

Stability and Responsiveness of Loop are controlled through VC Pin which is the output of Error Amp.
The combination of zero and pole that determines Stability and Responsiveness is adjusted by the combination of resistor and capacitor that are connected in series to the VC Pin.
DC Gain of Voltage Return Loop can be calculated for using the following formula.

$$\mathbf{A_{dc}} = \mathbf{R_l} \times \mathbf{G_{CS}} \times \mathbf{A_{VEA}} \times \frac{\mathbf{V_{FB}}}{\mathbf{Vout}} \quad \ldots(\mathbf{8})$$

Here, V_{FB} is Feedback Voltage (1.0V).A_{EA} is Voltage Gain of Error amplifier (typ: 55.6dB), Gcs is the Trans-conductance of Current Detect (typ: 10A/V), and R_l is the Output Load Resistance value.

There are 2 important poles in the Control Loop of this DC/DC.
The first occurs with/ through the output resistance of Phase compensation Capacitor (C3) and Error amplifier.
The other one occurs with/through the Output Capacitor and Load Resistor.
These poles appear in the frequency written below.

$$\mathbf{f_{p1}} = \frac{\mathbf{G_{EA}}}{\mathbf{2\pi \times C3 \times A_{VEA}}} \quad \ldots(\mathbf{9})$$

$$\mathbf{f_{p2}} = \frac{\mathbf{1}}{\mathbf{2\pi \times C_{OUT} \times R_l}} \quad \ldots(\mathbf{10})$$

Here, GEA is the trans-conductance of Error amplifier (typ: 300 µA/V).
Here, in this Control Loop, one zero becomes important. With the zero which occurs because of Phase compensation Capacitor C3 and Phase compensation Resistor R3, the Frequency below appears.

$$\mathbf{f_{z1}} = \frac{\mathbf{1}}{\mathbf{2\pi \times C3 \times R3}} \quad \ldots(\mathbf{11})$$

Also, if Output Capacitor is big, and that ESR (RESR) is big, in this Control Loop, there are cases when it has an important, separate zero (ESR zero).
This ESR zero occurs due to ESR of Output Capacitor and Capacitance, and exists in the Frequency below.

$$\mathbf{fz_{ESR}} = \frac{\mathbf{1}}{\mathbf{2\pi \times C_{OUT} \times R_{ESR}}} \quad \ldots(\mathbf{12}) \qquad \text{(ESR zero)}$$

In this case, the 3rd pole determined with the 2nd Phase compensation Capacitor (C8) and Phase Correction Resistor (R3) is used in order to correct the ESR zero results in Loop Gain.
This pole exists in the frequency shown below.

$$\mathbf{f_{p3}} = \frac{\mathbf{1}}{\mathbf{2\pi \times C8 \times R3}} \quad \ldots(\mathbf{13}) \qquad \text{(pole that corrects ESR zero)}$$

The target of Phase compensation design is to create a communication function in order to acquire necessary band and Phase margin.
Cross-over Frequency (band) at which Loop gain of Return Loop becomes “0” is important.
When Cross-over Frequency becomes low, Power supply Fluctuation Response, Load Response, etc worsens.
On the other hand, when Cross-over Frequency is too high, instability of the Loop can occur.
Tentatively, Cross-over Frequency is targeted to be made 1/20 or below of Switching Frequency.

Selection method of Phase Compensation constant is shown below.

1. Phase Compensation Resistor (R3) is selected in order to set to the desired Cross-over Frequency.
   Calculation of RC is done using the formula below.

   $$\mathbf{R3} = \frac{\mathbf{2\pi \times C_{OUT} \times f_c}}{\mathbf{G_{EA} \times G_{CS}}} \times \frac{\mathbf{V_{OUT}}}{\boldsymbol{V_{FB}}} \quad \ldots(\mathbf{14})$$

   Here, fc is the desired Cross-over Frequency. It is made about 1/20 and below of the Normal Switching Frequency (fs).

2. Phase compensation Capacitor (C3) is selected in order to achieve the desired phase margin.
   In an application that has a representative Inductance value (about several 4.7µH～33µH), by matching zero of compensation to 1/4 and below of the Cross-over Frequency, sufficient Phase margin can be acquired. C3 can be calculated using the following formula.

   $$\mathbf{C3} > \frac{\mathbf{4}}{\mathbf{2\pi \times R3 \times f_c}} \quad \ldots(\mathbf{15})$$

3. Examination whether the second Phase compensation Capacitor C8 is necessary or not is done.
   If the ESR zero of Output Capacitor exists in a place that is smaller than half of the Switching Frequency, a second Phase compensation Capacitor is necessary. In other words, it is the case wherein the formula below happens.

$$\frac{1}{2\pi \times C_{OUT} \times R_{ESR}} < \frac{f_s}{2} \quad \ldots(16)$$

In this case, add the second Phase compensation Capacitor C8, and match the frequency of the third pole to the Frequency fp3 of ESR zero.

$$C8 = \frac{C_{OUT} \times R_{ESR}}{R3} \quad \ldots(17)$$

8. Frequency setting

Arbitrary internal oscillator frequency setup is possible by connecting R4 resistance. Recommended frequency range is 50 kHz to 750 kHz.
For setting frequency f [Hz] 、R4 resistance is looked for using the following formula.

$$R4 = \frac{\frac{1}{f} - 400 \times 10^{-9}}{96.48 \times 10^{-12}} \quad [\Omega] \ldots (18)$$

If setting frequency is 200kHz, R4 is 47kΩ.
R4 resistance is related to frequency as shown in Figure15.

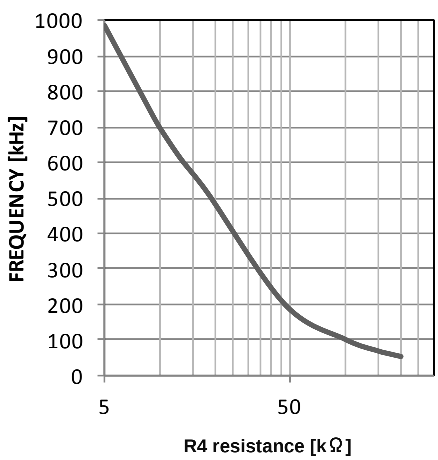


Fig.15 Oscillator Frequency – R4 resistance

9. External UVLO threshold

The high precision reset function is built in EN terminal of BD9G341AEFJ, and arbitrary low-voltage malfunction prevention setup is possible by connecting EN pin to resistance division of input voltage.
When you use, please set R1 and R2 to arbitrary voltage of IC turned on (Vuv) and hysteresis (Vuvhys) like below.

$$R1 = \frac{Vuvhys}{IEN} \quad [ohm]$$

$$R2 = \frac{VEN \times R1}{Vuv\text{-}VEN} \quad [ohm]$$

IEN:EN pin source current 10uA(typ) VEN: EN pin output on threshold 2.6V(typ)
As an example in typical sample, When Vcc voltage which IC turned on 15V, Hysteresis width 1V, The resistance divider set to R1=100kΩ,R2=20kΩ.

- **Evaluation Board BOM**

  Below is a table with the build of materials. Part numbers and supplier references are provided.

Item	Qty.	Ref	Description	Manufacturer	Part Number
1	1	C1	CAP CER 10UF 100V 20% X7R SMD	Murata Electronics North America	KRM55TR72A106MH01K
2	1	C3	CAP CER 6800PF 50V 10% X7R 0603	Murata Electronics North America	GRM188R71H682KA01D
3	1	C4	CAP CER 0.1UF 50V 10% X7R 0603	Murata Electronics North America	GRM188R71H104KA93D
4	1	C5	CAP CER 100UF 6.3V 20% X5R 1206	Murata Electronics North America	GRM31CR60J107ME39L
5	1	D2	DIODE SCHOTTKY 90V 3A CPD	Rohm	RB095B-90TL
6	1	J1	CONN HEADER VERT .100 3POS 15AU	FCI	68000-103HLF
7	1	L1	INDUCTOR POWER 33UH 4.2A SMD	Wurth Electronics Inc	7447709330
8	1	R1	RES 110K OHM 1/10W 1% 0603 SMD	Rohm	MCR03ERTF1103
9	1	R2	RES 27K OHM 1/10W 1% 0603 SMD	Rohm	MCR03ERTF2702
10	1	R3	RES 10K OHM 1/10W 1% 0603 SMD	Rohm	MCR03ERTF1002
11	1	R4	RES 47K OHM 1/10W 1% 0603 SMD	Rohm	MCR03ERTF4702
12	1	R5	RES 3K OHM 1/10W 1% 0603 SMD	Rohm	MCR03ERTF3001
13	1	R6	RES 750 OHM 1/10W 1% 0603 SMD	Rohm	MCR03ERTF7500
14	2	TP1,TP3	TEST POINT PC MULTI PURPOSE RED	Keystone Electronics	5010
15	2	TP2,TP4	TEST POINT PC MULTI PURPOSE BLK	Keystone Electronics	5011
16	1	U1	IC REG BUCK SYNC ADJ 3A HTSOP-J8	Rohm	BD9G341AEFJ-E2

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