

LAPIS Semiconductor Errata

ML620Q500H Series

Issue date: Oct. 16th 2015



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1. Introduction

A part of functions on ML620Q500H Series (ML620Q503H/504H) has a bug. And User's manual has defective descriptions. This document describes the details and the workaround.

Target User's manual : FEUL620Q504H-01

1.1 Issue List

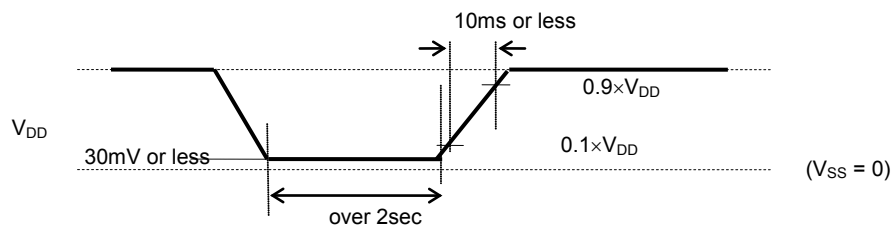
No.	Issue Date	Update	Subject
1	2015.10.16	-	Power-down/on Procedures
2	2015.10.16	-	Memory mapping of ML620Q503H

2. Detail Description

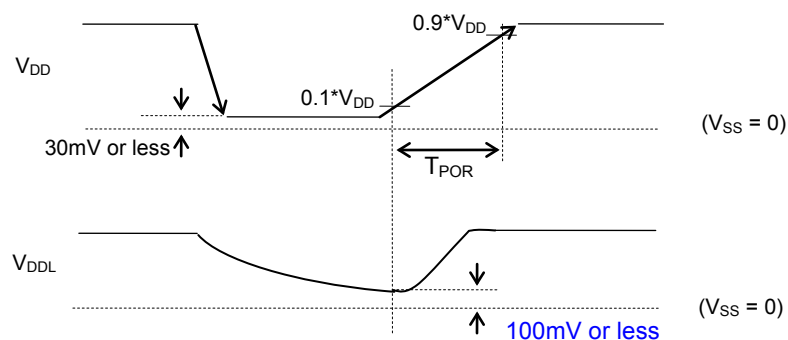
2.1 Power-down/on Procedures

A Power-on procedures and constraints are modified (in Appendix C. of the User's manual).

(Previous procedures and constraints)



(Modified procedures and constraints)



Note:

If V_{DDL} level is 100mV or more over, reset the IC by RESET_N pin after power-on.

2.2 Memory mapping of ML620Q503H

Memory mapping of ML620Q503H is modified (in section 2. CPU and Memory Space of the User's manual).

(Previous mapping) :

CSR:PC	Code segment 0
0:0000H	Vector table or
0:00FFH	Program code
0:0100H	Program code
0:7BFFH	Program code
0:7C00H	Test data area (Rewritable)
0:7DFFH	Test data area (Not rewritable)
0:7E00H	Test data area (Not rewritable)
0:7FFFH	Test data area (Not rewritable)
8bit	

(Modified mapping) :

CSR:PC	Code segment 0
0:0000H	Vector table or
0:00FFH	Program code
0:0100H	Program code
0:7BFFH	Program code
0:7C00H	Unused area
0:0FBFFH	Unused area
0:0FC00H	Test data area (Rewritable)
0:0FDFFH	Test data area (Rewritable)
0:0FE00H	Test data area (Not rewritable)
0:0FFFFH	Test data area (Not rewritable)
8bit	

Revision History

Document No.	Issue date	Page		Description
		Before revised	After revised	
15LD-1070-01E	2015.10.16	–	–	First revision