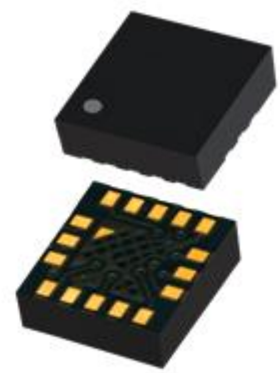
Digital Tri-axis Gyroscope/ Tri-axis Accelerometer PRELIMINARY Specifications

PART NUMBER:

KXG03
Rev. 0.1
Mar 15

Product Description



KXG03 is a 6 Degrees-of-Freedom inertial sensor system that features digital outputs accessed through I^{2}C or SPI communication. The KXG03 sensor consists of a tri-axial micro machined gyroscope plus a tri-axial accelerometer and an ASIC packaged in a 3x3x0.9mm 16pin Land Grid Array (LGA) package. The ASIC is realized in standard CMOS technology and features flexible user programmable gyroscope full scale ranges of ±256, ±512, ±1024, and ±2048º/sec and user-programmable ±2g/±4g/±8g/±16g full scale range for the accelerometer. An auxiliary I^{2}C master serial interface exists for communication to up to 2 other sensors to access data that can be accumulated in an internal 1024 byte FIFO buffer and transmitted to the application processor. In addition, the KXG03 has an embedded temperature sensor.

During operation, the gyroscope sensor elements are forced into vibration. When angular velocities are applied about the sensing axes, vibration is transferred to sensing elements, causing capacitance changes at the sensor electrodes. Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element, which utilizes common mode cancellation to decrease errors from process variation, temperature, and environmental stress. Capacitance changes are amplified and converted into digital signals which are processed by a dedicated digital signal processing unit. The digital signal processor applies filtering, bias and sensitivity adjustment, as well as temperature compensation. The DSP also feeds back the driving signal to ensure the proper sensor excitation.

The KXG03 series is designed to strike a balance between current consumption and noise performance with excellent bias stability over temperature. These sensors can accept supply and digital communication voltages between 1.8 and 3.3V.

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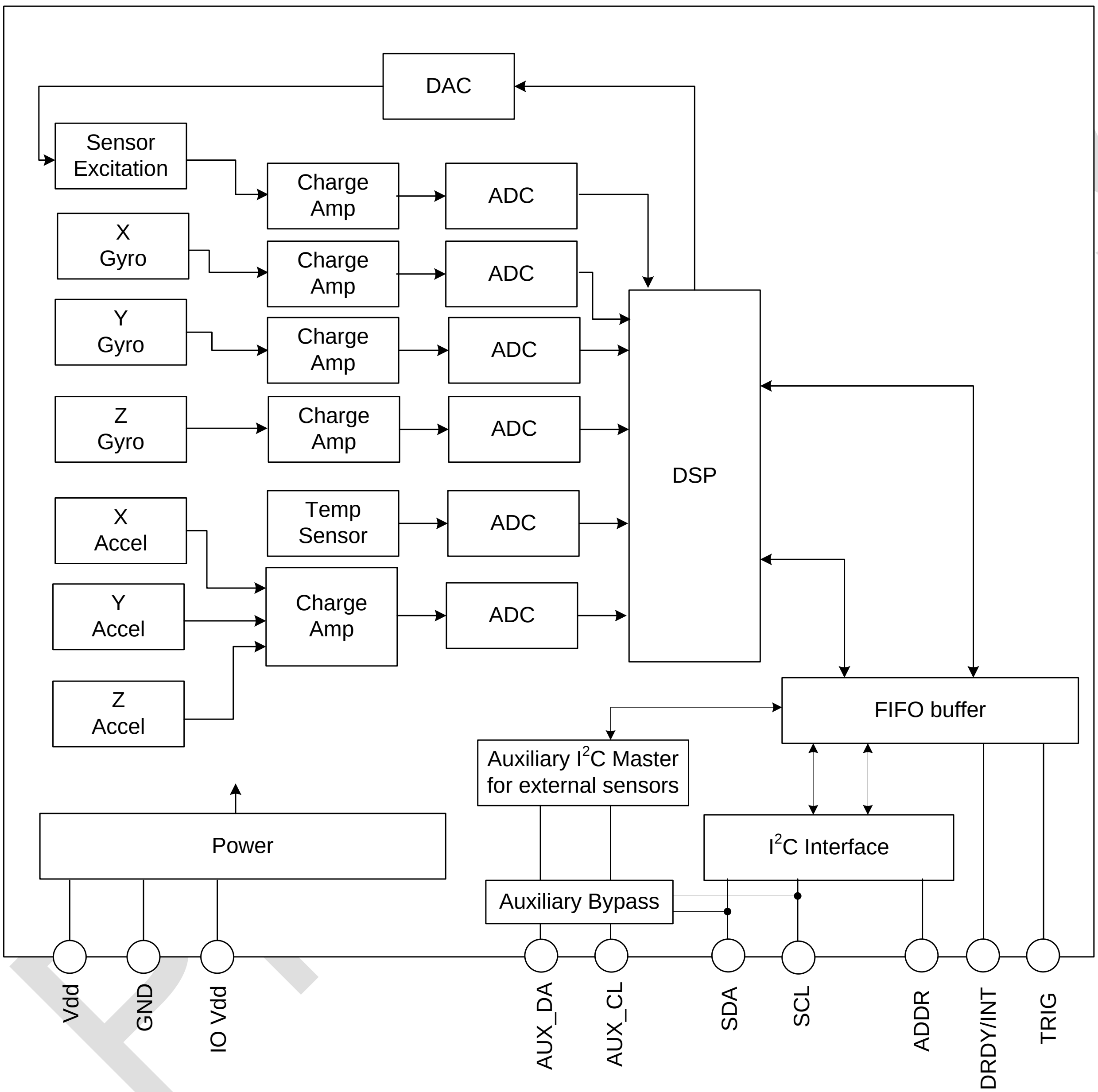

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Product Specifications

Table 1. Gyroscope Mechanical

(specifications are for operation at Vdd = 2.5V and T = 25ºC unless stated otherwise)

Parameters		Units	Min	Typical	Max
Operating Temperature Range		ºC	-40	-	85
Zero Rate Output, Digital		counts		0	
Zero Rate Output Stability		± % of FS		1	
Zero Rate Output Variation over Temperature		± deg/ sec		5	
Sensitivity (16-bit)	RSEL1 = 0, RSEL0 = 0, ±256 deg/sec	counts/deg/sec		128	
	RSEL1 = 0, RSEL0 = 1, ±512 deg/sec			64	
	RSEL1 = 1, RSEL0 = 0, ±1024 deg/sec			32	
	RSEL1 = 1, RSEL0 = 1, ±2048 deg/sec			16	
Sensitivity Variation over Temperature		%		5	
Noise Density		deg/sec/√Hz		0.03	
Output Noise (10 Hz BW)		dps-rms		0.23	
Non-Linearity		% of FS		0.5	
Cross Axis Sensitivity		± %		1	

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Table 2. Accelerometer Mechanical

(specifications are for operation at 2.5V and T = 25C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Operating Temperature Range		ºC	-40	-	85
Zero-g Offset		mg	-	±25	
Zero-g Offset Variation from RT over Temp.		± mg/ºC		0.25	
Sensitivity (16-bit)[1]	GSEL1=1, GSEL0=1 (± 2g)	counts/g		16384	
	GSEL1=0, GSEL0=0 (± 4g)			8192	
	GSEL1=0, GSEL0=1 (± 8g)			4096	
	GSEL1=1, GSEL0=0 (± 16g)			2048	
Sensitivity Variation from RT over Temp.		± %/ºC		0.01 (xy) 0.03 (z)	
Self Test Output		g		0.5	
Mechanical Resonance (-3dB)[2]		Hz		3500 (xy) 1800 (z)	
Non-Linearity		% of FS		0.5	
Cross Axis Sensitivity		%		2	
Noise Density		ug/rtHz		150	

Notes:

1. Resolution and acceleration ranges are user selectable.
2. Resonance as defined by the dampened mechanical sensor.

Table 3. Electrical

(specifications are for operation at V_{dd} = 3.0V and T = 25ºC unless stated otherwise)

Parameters		Units	Min	Typical	Max
Supply Voltage (Vdd)	Operating	V	1.8	3.0	3.3
I/O Pads Supply Voltage (Vio)		V	1.7		Vdd
Current Consumption	Operating (gyro + accel)	mA		2.1	
	Gyroscope only	mA		1.85	
	Accelerometer only 12 bit High Res Mode	µA		250	
	Accelerometer only 8 bit Low Res Mode and Sleep Mode (3.1Hz)[7]	µA		5	
	Standby	µA		1	
Output Low Voltage[1]		V	-	-	0.3 * Vio
Output High Voltage		V	0.9 * Vio	-	-
Input Low Voltage		V	-	-	0.2 * Vio
Input High Voltage		V	0.8 * Vio	-	-
Turn on Time (Power on Reset Time)[2]		ms			50
Sensor Start-Up Time[3]	Gyroscope	ms		30	
	Accelerometer (100Hz)	ms		20	
I²C Communication Rate[4,5]		MHz			3.4
I²C Address				4Eh / 4Fh	
SPI communication Rate		MHz			10
Bandwidth (-3dB)[6]		Hz			

Notes:
1. Assuming I²C communication and minimum 1.5kΩ pull-up resistor on SCL and SDA.
2. From Off to Standby mode after Vdd and Vio are valid
3. Time to valid sensor output (within 90% of final value) after sensor enable command executed (standby mode to operating mode). Accelerometer time varies with accelerometer Output Data Rate (ODR) per table below.
4. Assuming max bus capacitance load of 20pF.
5. The I²C bus supports Standard-Mode, Fast-Mode and High Speed Mode.
6. User selectable via control register
7. Accelerometer only in 8 bit Low Res Mode or Sleep current varies with accelerometer Output Data Rate (ODR) and Output Wake Up Function (OWUF) per table below. Note total current is determined by the highest setting or either ODR or OWUF. Start Up time is determined by OWUF.

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Accelerometer Start Up Profile (typical values)	
ODR (Hz)	**Accel Start Up Time (ms)**
12.5	80
25	41
50	21
100	11
200	6.4
400	3.9
800	2.7
1600	2.1

Accelerometer 8 bit Low Res Mode or Sleep Current Profile (typical values)	
8 Bit ODR or OWUF (Hz)	**Total Current (µA)**
0.781	5
1.563	5
3.125	5
6.25	7
12.5	11
25	18
50	32
100	62
200 ODR (100 OWUF)	118

Table 4. Temperature Sensor

(specifications are for operation at V_{dd} = 3.0V and T = 25ºC unless stated otherwise)

Parameters	Units	Min	Typical	Max
Operating Temperature Range	ºC	-40	-	85
Output Accuracy	± ºC		1	
Sensitivity (8-bit digital)	counts/ ºC		128	

KXG03 I²C Timing Diagram

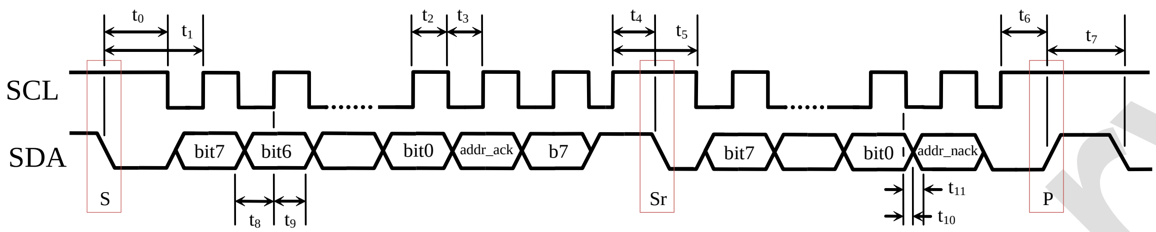

Table 5. I²C Timing (Fast Mode)

Number	Description	MIN	MAX	Units
t_0	SDA low to SCL low transition (Start event)	50	-	ns
t_1	SDA low to first SCL rising edge	100	-	ns
t_2	SCL pulse width: high	100	-	ns
t_3	SCL pulse width: low	100	-	ns
t_4	SCL high before SDA falling edge (Start Repeated)	50	-	ns
t_5	SCL pulse width: high during a S/Sr/P event	100	-	ns
t_6	SCL high before SDA rising edge (Stop)	50	-	ns
t_7	SDA pulse width: high	25	-	ns
t_8	SDA valid to SCL rising edge	50	-	ns
t_9	SCL rising edge to SDA invalid	50	-	ns
t_{10}	SCL falling edge to SDA valid (when slave is transmitting)	-	100	ns
t_{11}	SCL falling edge to SDA invalid (when slave is transmitting)	0	-	ns
Note	Recommended I²C CLK	2.5	-	us

Table 6. Environmental

Parameters		Units	Min	Typical	Max
Supply Voltage (Vdd)	Absolute Limits	V	-0.3	-	3.6
Operating Temperature Range		ºC	-40	-	85
Storage Temperature Range		ºC	-55	-	150
Mech. Shock (powered and unpowered)		g	-	-	5000 for 0.5ms 10000 for 0.2ms
ESD	HBM	V	-	-	2000

Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.

RoHS 2002/95/EC

This product conforms to Directive 2002/95/EC of the European Parliament and of the Council of the European Union (RoHS). Specifically, this product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), or polybrominated diphenyl ethers (PBDE) above the maximum concentration values (MCV) by weight in any of its homogenous materials. Homogenous materials are "of uniform composition throughout."

HF

This product is halogen-free per IEC 61249-2-21. Specifically, the materials used in this product contain a maximum total halogen content of 1500 ppm with less than 900-ppm bromine and less than 900-ppm chlorine.

Soldering

Soldering recommendations are available upon request or from www.kionix.com.

Floor Life

Factory floor life exposure of the KXCJK reels removed from the moisture barrier bag should not exceed a maximum of 168 hours at 30C/60%RH. If this floor life is exceeded, the parts should be dried per the IPC/JEDEC J-STD-033A standard.

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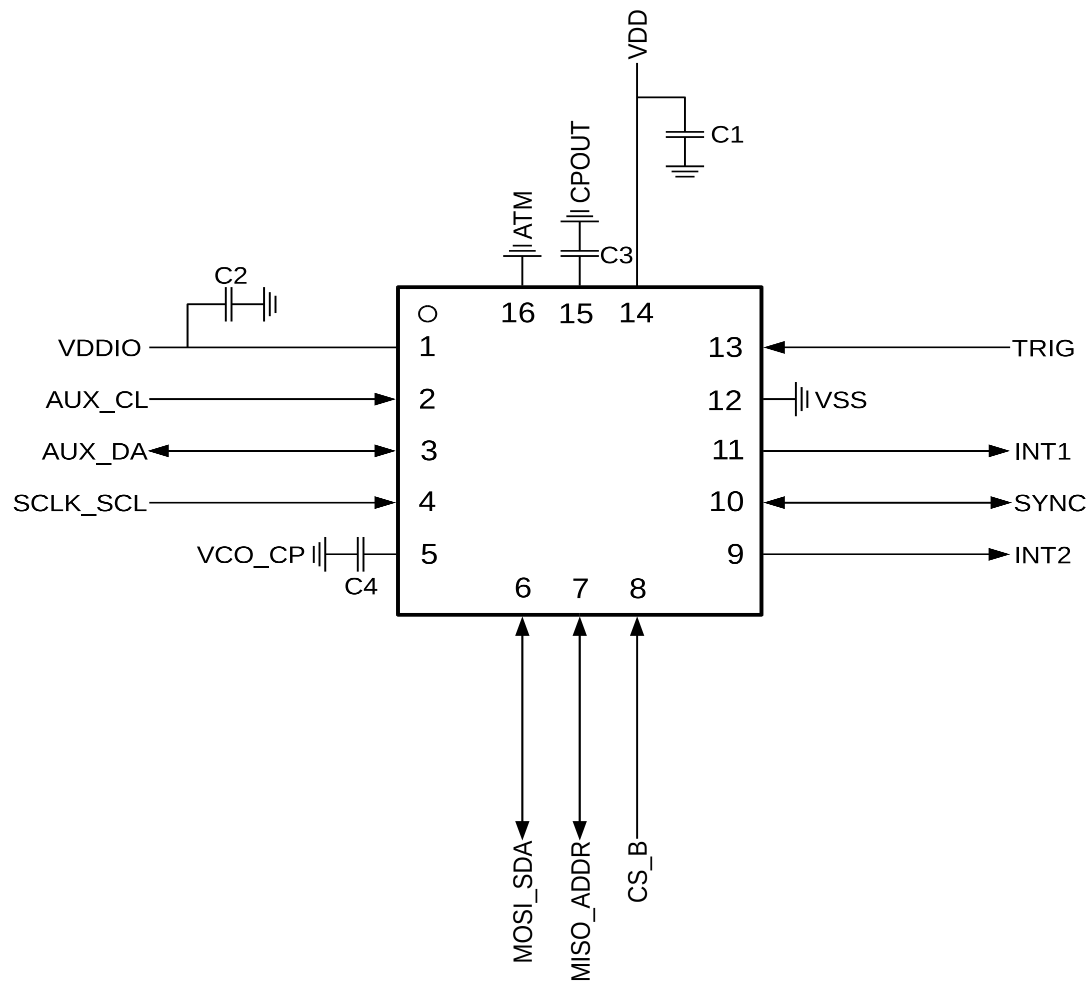
Application Schematic



Designation	Op Stress	Application	Value	Suggested Rating	Suggested Type
C1	3 V	VDD Bypass	0.1 uF	16 V	Y5V
C2	3 V	VDDIO Bypass	0.1 uF	16 V	Y5V
C3	20 V	QP Reservoir	2.2 nF	50 V	Y5V
C4	TBD	PLL Compensation	10 nF **1	16 V	Y5V

Table 7. KXG03 Pin Descriptions

Pin #	Pin Name	Description
1	VDDIO	External supply for IO ring.
2	AUX_CL	Auxiliary I2C master serial clock.
3	AUX_DA	Auxiliary I2C master serial data.
4	SCLK_SCL	SPI/I2C serial clock.
5	VCO_CP	PLL compensation cap.
6	MOSI_SDA	SPI MOSI / I2C serial data.
7	MISO_ADDR	SPI MISO / I2C slave_addr[0]
8	CS_B	SPI CS_B / I2C mode select
9	INT2	Programmable interrupt output.
10	SYNC	Sync input or output or … tbd
11	INT1	Programmable interrupt output.
12	VSS	GND.
13	TRIG	External trigger input for buffer actions.
14	VDD	External supply.
15	CPOUT	External charge pump reservoir cap.
16	ATM	Reserved. (Pin is tri-stated in user mode.)

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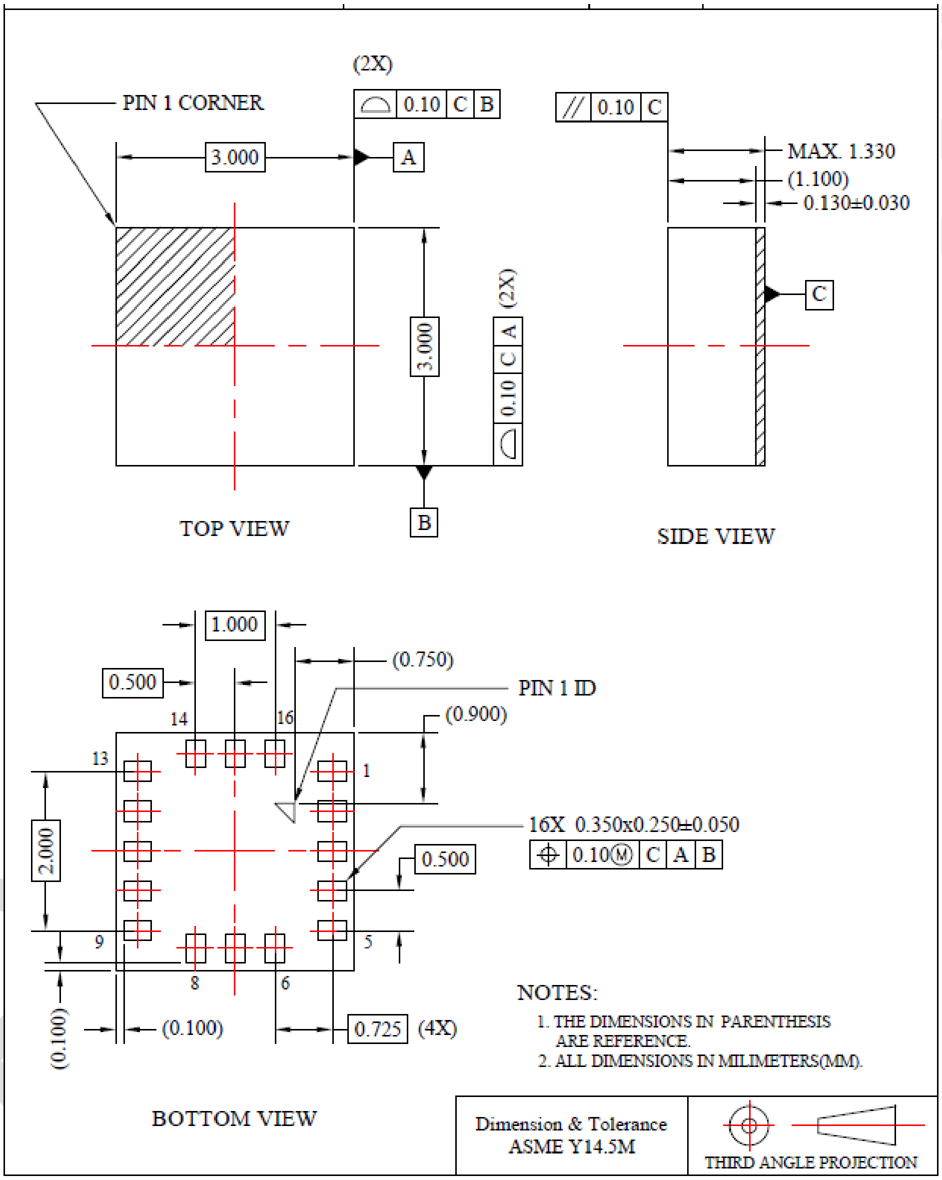
Package Dimensions and Orientation:

Dimensions

3 x 3 x 0.9 mm LGA



All dimensions and tolerances conform to ASME Y14.5M-1994

Orientation

When the device is accelerated or rotated in +X, +Y, or +Z direction, the corresponding output will increase.

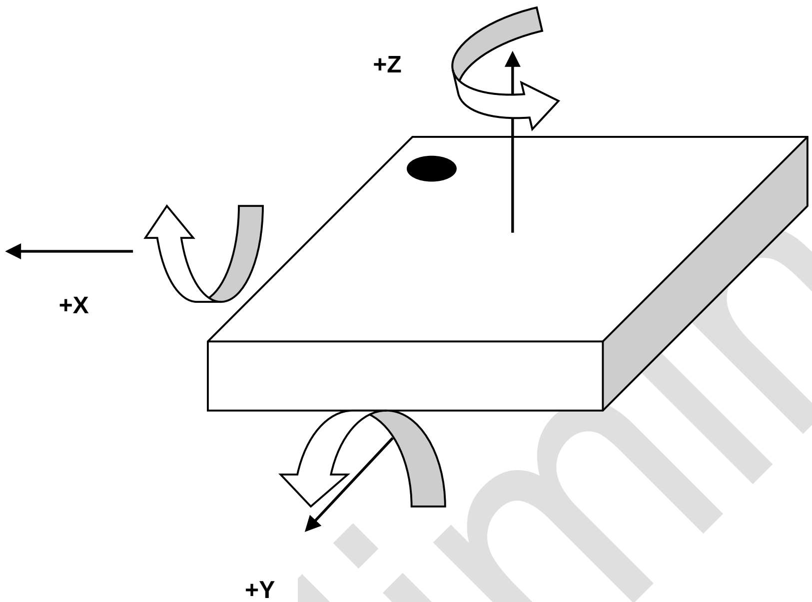


Figure 1 KXG03 Orientation

KXG03 Digital Interface

The Kionix KXG03 digital sensor has the ability to communicate on the I^2C digital serial interface bus. This flexibility allows for easy system integration by eliminating analog-to-digital converter requirements and by providing direct communication with system processors.

The serial interface terms and descriptions as indicated in Table 8 below will be observed throughout this document.

Term	Description
Transmitter	The device that transmits data to the bus.
Receiver	The device that receives data from the bus.
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer.
Slave	The device addressed by the Master.

Table 8. Serial Interface Terminologies

I^2C Serial Interface

As previously mentioned, the KXG03 has the ability to communicate on an I^2C bus. I^2C is primarily used for synchronous serial communication between a Master device and one or more Slave devices. The system Master provides the serial clock signal and addresses Slave devices on the bus. The KXG03 always operates as a Slave device during standard Master-Slave I^2C operation.

I^2C is a two-wire serial interface that contains a Serial Clock (SCL) line and a Serial Data (SDA) line. SCL is a serial clock that is provided by the Master, but can be held low by any Slave device, putting the Master into a wait condition. SDA is a bi-directional line used to transmit and receive data to and from the interface. Data is transmitted MSB (Most Significant Bit) first in 8-bit per byte format, and the number of bytes transmitted per transfer is unlimited. The I^2C bus is considered free when both lines are high. The I2C interface is compliant with high-speed mode, fast mode and standard mode I2C standards.

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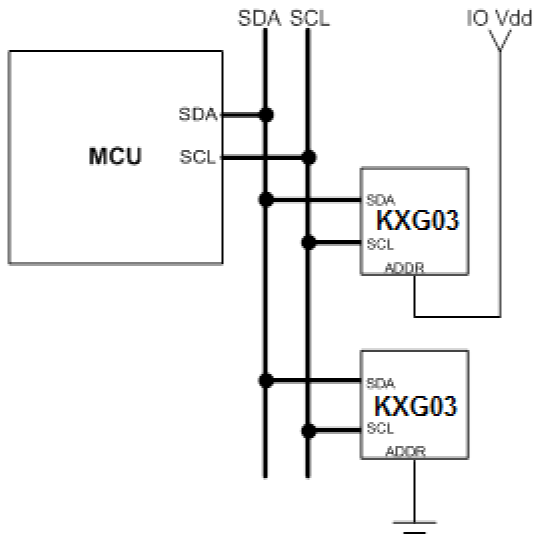

Figure 2 Multiple KXG03 I^{2}C Connection

I^{2}C Operation

Transactions on the I^{2}C bus begin after the Master transmits a start condition (S), which is defined as a high-to-low transition on the data line while the SCL line is held high. The bus is considered busy after this condition. The next byte of data transmitted after the start condition contains the Slave Address (SAD) in the seven MSBs (Most Significant Bits), and the LSB (Least Significant Bit) tells whether the Master will be receiving data '1' from the Slave or transmitting data '0' to the Slave. When a Slave Address is sent, each device on the bus compares the seven MSBs with its internally-stored address. If they match, the device considers itself addressed by the Master. The KXG03's Slave Address is comprised of a programmable part and a fixed part, which allows for connection of multiple KXG03's to the same I^{2}C bus. The Slave Address associated with the KXG03 is 100111X, where the programmable bit X is determined by the assignment of ADDR (pin 9) to GND or IO Vdd. Figure 2 above shows how two KXG03's would be implemented on an I^{2}C bus.

It is mandatory that receiving devices acknowledge (ACK) each transaction. Therefore, the transmitter must release the SDA line during this ACK pulse. The receiver then pulls the data line low so that it remains stable low during the high period of the ACK clock pulse. A receiver that has been addressed, whether it is Master or Slave, is obliged to generate an ACK after each byte of data has been received. To conclude a transaction, the Master must transmit a stop condition (P) by transitioning the SDA line from low to high while SCL is high. The I^{2}C bus is now free.

Writing to a KXG03 8-bit Register

Upon power up, the Master must write to the KXG03's control registers to set its operational mode. Therefore, when writing to a control register on the I^{2}C bus, as shown Sequence 1 on the following page, the following protocol must be observed: After a start condition, SAD+W transmission, and the KXG03 ACK has been returned, an 8-bit Register Address (RA) command is transmitted by the Master. This command is telling the KXG03 to which 8-bit register the Master will be writing the data. Since this is I^{2}C mode, the MSB of the RA command should always be zero (0). The KXG03 acknowledges the RA and the Master transmits the data to be stored in the 8-bit register. The KXG03 acknowledges that it has received the data and the Master transmits a stop condition (P) to end the data transfer. The data sent to the KXG03 is now stored in the appropriate register. The KXG03 automatically increments the received RA commands and, therefore, multiple bytes of data can be written to sequential registers after each Slave ACK as shown in Sequence 2 on the following page.

Reading from a KXG03 8-bit Register

When reading data from a KXG03 8-bit register on the I^{2}C bus, as shown in Sequence 3 on the next page, the following protocol must be observed: The Master first transmits a start condition (S) and the appropriate Slave Address (SAD) with the LSB set at '0' to write. The KXG03 acknowledges and the Master transmits the 8-bit RA of the register it wants to read. The KXG03 again acknowledges, and the Master transmits a repeated start condition (Sr). After the repeated start condition, the Master addresses the KXG03 with a '1' in the LSB (SAD+R) to read from the previously selected register. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NACK) it received the transmitted data, but transmits a stop condition to end the data transfer. Note that the KXG03 automatically increments through its sequential registers, allowing data to be read from multiple registers following a single SAD+R command as shown below in Sequence 4 on the following page. The 8-bit register data is transmitted using a left-most format, first bit shifted/clocked out being the MSB bit.

If a receiver cannot transmit or receive another complete byte of data until it has performed some other function, it can hold SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases SCL.

Data Transfer Sequences

The following information clearly illustrates the variety of data transfers that can occur on the I^{2}C bus and how the Master and Slave interact during these transfers. Table 9 defines the I^{2}C terms used during the data transfers.

Term	Definition
S	Start Condition
Sr	Repeated Start Condition
SAD	Slave Address
W	Write Bit
R	Read Bit
ACK	Acknowledge
NACK	Not Acknowledge
RA	Register Address
Data	Transmitted/Received Data
P	Stop Condition

Table 9. I^{2}C Terms

Sequence 1. The Master is writing one byte to the Slave.

Master	S	SAD + W		RA		DATA		P
Slave			ACK		ACK		ACK	

Sequence 2. The Master is writing multiple bytes to the Slave.

Master	S	SAD + W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

Sequence 3. The Master is receiving one byte of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Sequence 4. The Master is receiving multiple bytes of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

HS-mode

To enter the 3.4MHz high speed mode of communication, the device must receive the following sequence of conditions from the master: a Start condition followed by a Master code (00001XXX) and a Master Non-acknowledge. Once recognized, the device switches to HS-mode communication. Read/write data transfers then proceed as described in the sequences above. Devices return to the FS-mode after a STOP occurrence on the bus.

Sequence 5. HS-mode data transfer of the Master writing one byte to the Slave.

Speed	FS-mode			HS-mode								FS-mode
Master	S	M-code	NACK	S	SAD + W		RA		DATA		P	
Slave						ACK		ACK		ACK		

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Auxiliary I²C Operation

The KXG03 has an auxiliary I²C bus for communicating to external I²C-supported sensors. This bus has an I²C Host Mode where the KXG03 acts as a host to external sensors, and a Bypass Mode where the KXG03 directly connects the primary and auxiliary I²C buses together. This allows the system processor to directly communicate with the external sensors. Maximum data rate for this bus is 400kHz Fast Mode.

Auxiliary I²C Host Mode

This mode allows the KXG03 to directly access the data registers of any external sensors connected to the auxiliary I²C bus. In this mode, the KXG03 directly obtains data from the auxiliary sensors and packages them with its own sensor data inside the internal FIFO buffer.

In Host Mode the KXG03 is easily configured to read up to six successive registers from up to two different auxiliary devices. The user simply configures KXG03 control registers with up to two different I²C SAD's, starting register addresses and the number of bytes to be read back via auto-increment.

Auxiliary I²C Bypass Mode

This mode allows an external processor to act as host and directly communicate to the auxiliary devices. This allows the host to initialize the auxiliary sensors for operation, or to access them directly while the KXG03 is disabled.

Internal Pull-up Resistor

The KXG03 has an internal 1.5kΩ pull-up resistor to V_{io} on the AUX_SDA line. When Bypass Mode is activated, this internal pull-up resistor is automatically disengaged so as not to create a parallel resistance with the main I²C bus pull-up resistor. There is also a control bit in a control register to allow for manual disengaging of the pull-up resistor.

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Power Modes

The KXG03 has three power modes: Off, Stand-by, and Active. The part exists in one of these three modes at any given time. Off and Stand-by modes have very low current consumptions.

Power Mode	Bus State	V_{IO}	V_{dd}	Function	Outputs
Off	-	OFF	OFF	No sensor activity	Not available
Off	-	ON	OFF	No sensor activity	Not available
Off	-	OFF	ON	No sensor activity	Not available
Stand-by	Active	ON	ON	Waiting activation command	Not available
Sleep	Active	ON	ON	Accelerometer active looking for motion wake up	Accel registers only – no buffer, no DRDY int
Active	Active	ON	ON	All functionalities available	All sensors available

Off mode

One or both of the power supplies (V_{dd} or V_{IO}) are not powered. The sensor is completely inactive and not reporting or communicating. Bus communication actions of other devices are not disturbed if they are using the same bus interface as this component.

Initial Startup

The preferred startup sequence is to turn on V_{IO} before V_{dd}, but if V_{dd} is turned on first, the component will not affect the bus communications (no latch-up or other problems during engine system level wake-up).

Power On Reset (POR) is performed every time when:

1. V_{IO} supply is valid
2. V_{dd} power supply is going to valid level

OR

1. V_{IO} power supply is going to valid level
2. V_{dd} supply is valid

When POR occurs, the registers are loaded from OTP and the part is put into Stand-by mode.

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Stand-by mode

The primary function of the stand-by mode is to ensure fast wake-up to active mode and to minimize current consumption. This mode is set as default when both power supplies are applied and the POR function occurs. A Soft Reset command also performs the POR function and puts the part into Stand-by mode.

Stand-by mode is a low power waiting state for fast turn on time. Bus communication actions of other components are not disturbed if they are using the same bus. There is only one possible way to change to active mode – a register command from the external application processor via the I^2C bus.

Active mode

Stand-by-mode can be changed to Active mode by writing to register STBY_REG.

Active mode engages the full functionality of accelerometer and/or gyroscope measurements. The host also has the ability to change settings in the control register back to Stand-by mode for either or both the accelerometer and gyroscope.

Sleep mode

While in sleep mode, the accelerometer is periodically taking a measurement to detect if there is any motion. Data in the accelerometer registers is being updated, however, there is no data ready interrupt being reported. Also, no data is being sent to the buffer.

KXG03 Embedded Wake Up and Back To Sleep Function

The KXG03 contains an interrupt engine that can be configured by the user to report when qualified changes detected by the acceleration occur. The user has the option to enable or disable specific accelerometer axes and specific directions, as well as to specify the delay time. An example use case for the engine would be to detect motion on any axis to signal an event and wake up or put back to sleep the KXG03 or other devices. For Wake Up, this can be achieved by configuring the engine to detect when the acceleration on any axis is *greater* than the user-defined threshold for a user-defined amount of time. For Back To Sleep, this can be achieved by configuring the engine to detect when the acceleration on any axis is *less* than the user-defined threshold for a user-defined amount of time. Equations 1 and 2 show how to calculate the engine threshold and delay time register values for the desired result.

WAKEUP_THRESHOLD (counts) = Desired Threshold (g) x 16 (counts/g)

Equation 1. Wake Up Threshold

BTS_THRESHOLD (counts) = Desired Threshold (g) x 16 (counts/g)

Equation 2. Back To Sleep Threshold

WAKEUP_TIMER (counts) = Desired Delay Time (sec) x OWUF (Hz)

Equation 3. Wake Up Delay Time

BTS_TIMER (counts) = Desired Delay Time (sec) x OSA (Hz)

Equation 4. Back To Sleep Delay Time

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KXG03 Embedded Registers

The KXG03 has 55 embedded 8-bit registers that are accessible by the user. This section contains the addresses for all embedded registers and also describes bit functions of each register. Table 10 below provides a listing of the accessible 8-bit registers and their addresses.

Register Name	Type Read/Write	I²C Address Hex	I²C Address Binary
GYRO_XOUT_L	R	0x00	0000 0000
GYRO_XOUT_H	R	0x01	0000 0001
GYRO_YOUT_L	R	0x02	0000 0010
GYRO_YOUT_H	R	0x03	0000 0011
GYRO_ZOUT_L	R	0x04	0000 0100
GYRO_ZOUT_H	R	0x05	0000 0101
ACC_XOUT_L	R	0x06	0000 0110
ACC_XOUT_H	R	0x07	0000 0111
ACC_YOUT_L	R	0x08	0000 1000
ACC_YOUT_H	R	0x09	0000 1001
ACC_ZOUT_L	R	0x0A	0000 1010
ACC_ZOUT_H	R	0x0B	0000 1011
TEMP_OUT_L	R	0x0C	0000 1100
TEMP_OUT_H	R	0x0D	0000 1101
Reserved	R	0x0E – 0x1F	
WHO_AM_I	R	0x20	0010 0000
SN_1	R	0x21	0010 0001
SN_2	R	0x22	0010 0010
SN_3	R	0x23	0010 0011
SN_4	R	0x24	0010 0100
INS1	R	0x25	0010 0101
INS2	R	0x26	0010 0110
STATUS_REG	R	0x27	0010 0111
INL	R	0x28	0010 1000
STBY_REG	R/W	0x29	0010 1001
CTRL_REG1	R/W	0x2A	0010 1010
CTRL_REG2	R/W	0x2B	0010 1011
ODCTRL	R/W	0x2C	0010 1100
INC1	R/W	0x2D	0010 1101
INC2	R/W	0x2E	0010 1110
Reserved	R	0x2F	0010 1111

AUX_I2C_CTRL_REG1	R/W	0x30	0011 0000
AUX_I2C_CTRL_REG2	R/W	0x31	0011 0001
AUX_I2C_SAD1	R/W	0x32	0011 0010
AUX_I2C_REG1	R/W	0x33	0011 0011
AUX_I2C_CNTL1	R/W	0x34	0011 0100
AUX_I2C_BIT1	R/W	0x35	0011 0101
AUX_I2C_DELAY1	R/W	0x36	0011 0110
AUX_I2C_SAD2	R/W	0x37	0011 0111
AUX_I2C_REG2	R/W	0x38	0011 1000
AUX_I2C_CNTL2	R/W	0x39	0011 1001
AUX_I2C_BIT2	R/W	0x3A	0011 1010
AUX_I2C_DELAY2	R/W	0x3B	0011 1011
SRT	R	0x3C	0011 1100
WAKEUP_THRESHOLD	R/W	0x3D	0011 1101
WAKEUP_TIMER	R/W	0x3E	0011 1110
BTS_THRESHOLD	R/W	0x3F	0011 1111
BTS_TIMER	R/W	0x40	0100 0000
Reserved	R	0x41 - 0x76	-
BUF_THRESH_H	R/W	0x77	0111 0111
BUF_THRESH_L	R/W	0x78	0111 1000
BUF_CTRL1	R/W	0x79	0111 1001
BUF_CTRL2	R/W	0x7A	0111 1010
BUF_STATUS_H	R	0x7B	0111 1011
BUF_STATUS_L	R	0x7C	0111 1100
BUF_STATUS_REG	R	0x7D	0111 1101
BUF_CLEAR	W	0x7E	0111 1110
BUF_READ	R	0x7F	0111 1111

Table 10. I^2C Register Map

Gyroscope Outputs

These registers contain 16-bits of valid angular rate data for each axis. The data is protected from overwrite during each read, and can be converted from digital counts to angular rate (deg/sec) per Table 11 below.

16-bit Data (2's complement)	Equivalent Counts in decimal	Range = +/-2048 deg/sec	Range = +/-1024 deg/sec	Range = +/-512 deg/sec	Range = +/-256 deg/sec
0111 1111 1111 1111	32767	+2047.9375	+1023.9688	+511.9844	+255.9922
0111 1111 1111 1110	32766	+2047.8750	+1023.9376	+511.9688	+255.9844
…	…	…	…	…	…
0000 0000 0000 0001	1	+0.0625	+0.0312	+0.0156	+0.0078
0000 0000 0000 0000	0	0 deg/sec	0 deg/sec	0 deg/sec	0 deg/sec
1111 1111 1111 1111	-1	-0.0625	-0.0312	-0.0156	-0.0078
…	…	…	…	…	…
1000 0000 0000 0001	-32767	-2047.9375	-1023.9688	-511.9844	-255.9922
1000 0000 0000 0000	-32768	-2048.0000	-1024.0000	-512.0000	-256.0000

Table 11. Angular Rate (deg/sec) Calculation

Accelerometer Outputs

These registers contain up to 12-bits of valid acceleration data for each axis depending on the setting of the RES bit in CTRL_REG1, where the acceleration outputs are represented in 12-bit valid data when RES = '1' and 8-bit valid data when RES = '0'. . The data is updated every user-defined ODR period, is protected from overwrite during each read, and can be converted from digital counts to acceleration (g) per Table 12 below.

12-bit Register Data (2's complement)	Equivalent Counts in decimal	Range = +/-2g	Range = +/-4g	Range = +/-8g
0111 1111 1111	2047	+1.999g	+3.998g	+7.996g
0111 1111 1110	2046	+1.998g	+3.996g	+7.992g
…	…	…	…	…
0000 0000 0001	1	+0.001g	+0.002g	+0.004g
0000 0000 0000	0	0.000g	0.000g	0.000g
1111 1111 1111	-1	-0.001g	-0.002g	-0.004g
…	…	…	…	…
1000 0000 0001	-2047	-1.999g	-3.998g	-7.996g
1000 0000 0000	-2048	-2.000g	-4.000g	-8.000g

8-bit Register Data (2's complement)	Equivalent Counts in decimal	Range = +/-2g	Range = +/-4g	Range = +/-8g
0111 1111	127	+1.984g	+3.968g	+7.936g
0111 1110	126	+1.968g	+3.936g	+7.872g
…	…	…	…	…
0000 0001	1	+0.016g	+0.032g	+0.064g
0000 0000	0	0.000g	0.000g	0.000g
1111 1111	-1	-0.016g	-0.032g	-0.064g
…	…	…	…	…
1000 0001	-127	-1.984g	-3.968g	-7.936g
1000 0000	-128	-2.000g	-4.000g	-8.000g

Table 12. Acceleration (g) Calculation

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Register Descriptions

GYRO_XOUT_L

X-axis gyro output least significant byte

R	R	R	R	R	R	R	R
GYRO_X7	GYRO_X6	GYRO_X5	GYRO_X4	GYRO_X3	GYRO_X2	GYRO_X1	GYRO_X0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I²C Address: 0x00h		

GYRO_XOUT_H

X-axis gyro output most significant byte

R	R	R	R	R	R	R	R
GYRO_X15	GYRO_X14	GYRO_X13	GYRO_X12	GYROX11	GYRO_X10	GYRO_X9	GYRO_X8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I²C Address: 0x01h		

GYRO_YOUT_L

Y-axis gyro output least significant byte

R	R	R	R	R	R	R	R
GYRO_Y7	GYRO_Y6	GYRO_Y5	GYRO_Y4	GYRO_Y3	GYRO_Y2	GYRO_Y1	GYRO_Y0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I²C Address: 0x02h		

GYRO_YOUT_H

Y-axis gyro output most significant byte

R	R	R	R	R	R	R	R
GYRO_Y15	GYRO_Y14	GYRO_Y13	GYRO_Y12	GYRO_Y11	GYRO_Y10	GYRO_Y9	GYRO_Y8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I²C Address: 0x03h		

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GYRO_ZOUT_L

Z-axis gyro output least significant byte

R	R	R	R	R	R	R	R
GYRO_Z7	GYRO_Z6	GYRO_Z5	GYRO_Z4	GYRO_Z3	GYRO_Z2	GYRO_Z1	GYRO_Z0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x04h		

GYRO_ZOUT_H

Z-axis gyro output most significant byte

R	R	R	R	R	R	R	R
GYRO_Z15	GYRO_Z14	GYRO_Z13	GYRO_Z12	GYRO_Z11	GYRO_Z10	GYRO_Z9	GYRO_Z8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x05h		

ACCEL_XOUT_L

X-axis accelerometer output least significant byte

R	R	R	R	R	R	R	R
ACCEL_X3	ACCEL_X2	ACCEL_X1	ACCEL_X0	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x06h		

ACCEL_XOUT_H

X-axis accelerometer output most significant byte

R	R	R	R	R	R	R	R
ACCEL_X11	ACCEL_X10	ACCEL_X9	ACCEL_X8	ACCEL_X7	ACCEL_X6	ACCEL_X5	ACCEL_X4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x07h		

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ACCEL_YOUT_L
Y-axis accelerometer output least significant byte

R	R	R	R	R	R	R	R
ACCEL_Y3	ACCEL_Y2	ACCEL_Y1	ACCEL_Y0	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x08h		

ACCEL_YOUT_H
Y-axis accelerometer output most significant byte

R	R	R	R	R	R	R	R
ACCEL_Y11	ACCEL_Y10	ACCEL_Y9	ACCEL_Y8	ACCEL_Y7	ACCEL_Y6	ACCEL_Y5	ACCEL_Y4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x09h		

ACCEL_ZOUT_L
Z-axis accelerometer output least significant byte

R	R	R	R	R	R	R	R
ACCEL_Z3	ACCEL_Z2	ACCEL_Z1	ACCEL_Z0	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x0Ah		

ACCEL_ZOUT_H
Z-axis accelerometer output most significant byte

R	R	R	R	R	R	R	R
ACCEL_Z11	ACCEL_Z10	ACCEL_Z9	ACCEL_Z8	ACCEL_Z7	ACCEL_Z6	ACCEL_Z5	ACCEL_Z4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x0Bh		

TEMP_OUT_L

Temperature Output least significant byte

R	R	R	R	R	R	R	R
Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x0Ch		

TEMP_OUT_H

Temperature Output most significant byte

R	R	R	R	R	R	R	R
Temp15	Temp14	Temp13	Temp12	Temp11	Temp10	Temp9	Temp8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x0Dh		

WHO_AM_I

This register can be used for supplier recognition, as it can be factory written to a known byte value. The default value is 0x0Dh.

R	R	R	R	R	R	R	R	
WIA7	WIA6	WIA5	WIA4	WIA3	WIA2	WIA1	WIA0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00001101
					I^2C Address:		0x20h	

SN_1

Individual Identification (serial number) least significant byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SN7	SN6	SN5	SN4	SN3	SN2	SN1	SN0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x21h		

SN_2

Individual Identification (serial number) second byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SN15	SN14	SN13	SN12	SN11	SN10	SN9	SN8

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I²C Address: 0x22h		

SN_3

Individual Identification (serial number) third byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SN23	SN22	SN21	SN20	SN19	SN18	SN17	SN16
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I²C Address: 0x23h		

SN_4

Individual Identification (serial number) most significant byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SN31	SN30	SN29	SN28	SN27	SN26	SN25	SN24
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I²C Address: 0x24h		

INS1

Interrupt source register 1 –This Register tells which function caused an interrupt. Reading from the interrupt release register (INL 0x28h) will clear the contents of this register.

R	R	R	R	R	R	R	R
Reserved	BFI	WMI	DRDY	Reserved	Reserved	WUFS	BTS
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I²C Address: 0x25h		

BFI - *indicates that the internal 1024 byte FIFO buffer is full. This bit is cleared when the data is read or the interrupt release register (INL 0x28h) is read.*
BFI = 0 – Buffer is not full
BFI = 1 – Buffer is full

WMI - *indicates that user-defined buffer watermark has been reached. This bit is cleared when the data is read or the interrupt release register (INL 0x28h) is read.*
BFI = 0 – Buffer watermark not reached
BFI = 1 – Buffer watermark reached

DRDY *- indicates that new sensor data (00h to 0Dh) is available. This bit is cleared when sensor data is read or the interrupt release register (INL, 0x28h).*
DRDY = 0 – New sensor data not available
DRDY = 1 – New sensor data available

WUFS *- Wake up. This bit is cleared when the interrupt source latch register (INL, 0x28h) is read.*
WUFS = 1 – Motion has activated the interrupt
WUFS = 0 – No motion

BTS *– Back to Sleep interrupt. This bit is cleared when the interrupt source latch register (INL, 0x28h) is read.*
BTS = 0 – normal operating mode, motion is occurring
BTS = 1 – No motion is occurring and sensors can be shutdown

INS2

Interrupt source register 2 –This Register reports the axis and direction of the motion that triggered the wakeup interrupt. This register is cleared when the interrupt source latch register (INL, 0x28h) is read.

R	R	R	R	R	R	R	R
0	0	XNWU	XPWU	YNWU	YPWU	ZNWU	ZPWU
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I²C Address: 0x26h		

XNWU *- x negative (x-)*
XPWU *- x positive (x+)*
YNWU *- y negative (y-)*
YPWU *- y positive (y+)*
ZNWU *- z negative (z-)*
ZPWU *- z positive (z+)*

STATUS_REG

Status register. Note that AGC_LOCK and PLL_LOCK bits are '0' at system startup and goes to '1' as the output rate signals become valid; permanent AGC_LOCK = '0' and/or PLL_LOCK = '0' indicate a damage in the device.

R	R	R	R	R	R	R	R
Reserved	Reserved	Reserved	INT	Reserved	AGC_LOCK	PLL_LOCK	STARTUP
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I²C Address: 0x27h		

INT *reports the combined (OR) interrupt information of DRDY, WUFS, and BTS in the interrupt source register (INS1, 0x25h). This bit is cleared when the interrupt release register (INL, 0x28h) is read.*

0 = no interrupt event

1 = interrupt event has occurred

AGC_LOCK *indicates the state of the AGC*

AGC_LOCK = 0 – not ready state

AGC_LOCK = 1 – AGC loop has been locked and ready for use

PLL_LOCK *indicates the state of the PLL*

PLL_LOCK = 0 – not ready state

PLL_LOCK = 1 – PLL loop has been locked and ready for use

STARTUP *indicates the condition of system initialization*

STARTUP = 0 – operating mode

STARTUP = 1 – KXG03 is in startup mode

INL

Interrupt Latch Release – Latched interrupt source information (at INS1 0x25h, INS2 0x26h and STATUS_REG 0x27 bit INT) is cleared and physical interrupt latched pin (12) is changed to its inactive state when this register is read.

R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x28h		

STBY_REG

Stand-by and operational control register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ACT_STBY	Reserved	Reserved	Reserved	AUX2_STBY	AUX1_STBY	GYRO_STBY	ACCEL_STBY	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	01111111
					I^2C Address: 0x29h			

ACCEL_STBY *controls the operating mode of the KXG03's accelerometer*
ACCEL_STBY = 0 – operating mode
ACCEL_STBY = 1 – stand-by mode. WUF and BTS engines will not function.

GYRO_STBY *controls the operating mode of the KXG03's gyroscope.*
GYRO_STBY = 0 – operating mode. Sensor will respond to WUF and BTS engines if those engines are enabled and ACT_STBY=1.
GYRO_STBY = 1 – stand-by mode. Sensor will not respond to WUF and BTS engines if those engines are enabled.
AUX1_STBY*: controls the operating mode of the KXG03's auxiliary sensor 1*
AUX1_STBY = 0: operating mode. Sensor will respond to WUF and BTS engines if those engines are enabled and ACT_STBY=1.
AUX1_STBY = 1: stand-by mode. Sensor will not respond to WUF and BTS engines.
AUX2_STBY*: controls the operating mode of the KXG03's auxiliary sensor 2*
AUX2_STBY = 0: operating mode. Sensor will respond to WUF and BTS engines if those engines are enabled and ACT_STBY=1.
AUX2_STBY = 1: stand-by mode. Sensor will not respond to WUF and BTS engines.
ACT_STBY*: allows the KXG03 to control the operating mode of all of the connected devices based on the activity state of the device*
ACT_STBY = 0: feature disabled
ACT_STBY = 1: connected devices will be enabled when the internal accelerometer measures activity and disabled when the internal accelerometer measures inactivity.

CTRL_REG1

Read/Write control register 1. Note that to properly change the value of this register, the ACCEL_STBY bit and/or GYRO_STBY bit must first be set to "1".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
BTSE	WUFE	DRDYE	RES	Rsel1	Rsel0	Gsel1	Gsel0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I²C Address: 0x2Ah			

BTSE *enables the Back to Sleep engine. Note that to change the value of this bit, the ACCEL_STBY bit must first be set to "1".*
BTSE = 0 – disabled
BTSE = 1 – enabled

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WUFE *enables the Wake up engine. Note that to change the value of this bit, the ACCEL_STBY bit must first be set to "1".*

WUFE = 0 – disabled
WUFE = 1 – enabled

DRDYE *enables the reporting of the availability of new sensor data as an interrupt. Note that to change the value of this bit, the ACCEL_STBY bit must first be set to "1".*

DRDYE = 0 – disabled
DRDYE = 1 – enabled

RES *controls the resolution of the accelerometer and analog sensor ADC. Note that to change the value of this bit, the ACCEL_STBY bit must first be set to "1".*

RES = 0 – lower power, low resolution (8-bit) mode. Only available for ODR <= 200 Hz. Bandwidth (Hz) = 800
RES = 1 – higher power, high resolution (12-bit or 14bit) mode. Bandwidth (Hz) = ODR/2

If STBY_REG, GYRO_STBY = 0 (gyroscope is operating), then RES is automatically set to RES=1 mode.

If STBY_REG, GYRO_STBY = 1 (gyroscope is in standby), then RES can be RES=0 or RES = 1 as defined by the user. ***Note****, if RES=0, then the buffer is not active – only the data registers contain valid sensor data.*

GSEL1, GSEL0 *selects the acceleration range of the accelerometer outputs per the following table. Note that to change the value of this bit, the ACCEL_STBY bit and GYRO_STBY bit must first be set to "1".*

GSEL1	GSEL0	Range
0	0	+/-2g
0	1	+/-4g
1	0	+/-8g
1	1	+/-8g 14bit RES = 1

Selected Acceleration Range

RSEL1, RSEL0 *selects the angular velocity range of the gyroscope outputs per the following table. Note that to change the value of this bit, the ACCEL_STBY bit must first be set to "1".*

RSEL1	RSEL0	Range
0	0	+/-256
0	1	+/-512
1	0	+/-1024
1	1	+/-2048

Selected Angular Velocity Range

CTRL_REG2

Read/Write control register. Note that to properly change the value of this register, the ACCEL_STBY bit must first be set to “1”

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
SRST	Reserved	Reserved	COTC	Reserved	OWUFA	OWUFB	OWUFC	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I²C Address: 0x2Bh			

SRST *Software Reset function initiates software reset, which performs the RAM reboot routine. This bit will remain 1 until the RAM reboot routine is finished. Note that to change the value of this bit, the ACCEL_STBY bit must first be set to “1”.*

SRST = 0 – no action

SRST = 1 – start reboot routine

COTC *initiates the digital communication self-test function. Note that to change the value of this bit, the ACCEL_STBY bit must first be set to “1”.*

COTC= 0 – no action

COTC = 1 – sets 0xAAh to SRT 0x3Ch register, when the STR register is read, COTC is cleared and STR = 0x55h.

OWUF(2:0): *sets the Output Data Rate for the wake up (motion detection) per table below. Note that to change the value of these bits, the ACCEL_STBY bit must first be set to “1”*

OWUFA	OWUFB	OWUFC	Output Data Rate (Hz)
0	0	0	0.781
0	0	1	1.563
0	1	0	3.125

0	1	1	6.25
1	0	0	12.5
1	0	1	25
1	1	0	50
1	1	1	100

ODCNTL

Output data control register. Note that to properly change the value of this register, the ACCEL_STBY bit and GYRO_STBY bit must first be set to "1".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ACCEL_BW1	ACCEL_BW0	GYRO_BW1	GYRO_BW0	OSAA	OSAB	OSAC	OSAD	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000010
					I²C Address: 0x2Ch			

OSAA, OSAB, OSAC, OSAD: *Rate at which data samples from enabled sources will be updated in the register map and FIFO buffer. Note that to change the value of these bits, the ACCEL_STBY bit and GYRO_STBY bit must first be set to "1".*

OSAA	OSAB	OSAC	OSAD	Output Data Rate
1	0	0	0	0.781Hz
1	0	0	1	1.563Hz
1	0	1	0	3.125Hz
1	0	1	1	6.25Hz
0	0	0	0	12.5Hz
0	0	0	1	25Hz
0	0	1	0	50Hz
0	0	1	1	100Hz
0	1	0	0	200Hz
0	1	0	1	400Hz
0	1	1	0	800Hz
0	1	1	1	1600Hz

Table 13. Sampling Rate
Note: Output Data Rates >= 400Hz will force device into Full Power mode

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ACCEL_BW(1:0): *Accelerometer bandwidth selection*

ACCEL_BW1	ACCEL_BW0	Range
X	X	ODR/2

Table 14. Accelerometer Bandwidth in High Power Mode

GYRO_BW(1:0): *Gyroscope bandwidth selection. Note that to change the value of these bits, the ACCEL_STBY bit and GYRO_STBY bit must first be set to "1".*

GYRO_BW1	GYRO_BW0	Range
0	0	10 Hz
0	1	20 Hz
1	0	40 Hz
1	1	160 Hz

Table 15. Gyroscope Bandwidth

INC1

This register controls the settings for the physical interrupt pin (12). Note that to properly change the value of this register, the ACCEL_STBY bit and GYRO_STBY bit must first be set to "1".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reserved	Reserved	IEN	IEA	IEL	Reserved	Reserved	Reserved	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00010000
					I²C Address: 0x2Dh			

IEN *enables/disables the physical interrupt pin (12)*
IEN = 0 – physical interrupt pin (12) is disabled
IEN = 1 – physical interrupt pin (12) is enabled

IEA *sets the polarity of the physical interrupt pin (12)*
IEA = 0 – polarity of the physical interrupt pin (12) is active low
IEA = 1 – polarity of the physical interrupt pin (12) is active high

IEL *sets the response of the physical interrupt pin (12)*
IEL = 0 – the physical interrupt pin (12) latches until it is cleared by reading INL 0x28h

IEL = 1 – the physical interrupt pin (12) will transmit one 50us pulse

INC2

Interrupt control 2 – This register controls which axis and direction of detected motion can cause an interrupt. Note that to properly change the value of this register, the ACCEL_STBY bit and GYRO_STBY bit must first be set to “1”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reserved	Reserved	XNWUE	XPWUE	YNWUE	YPWUE	ZNWUE	ZPWUE	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00111111
					I²C Address: 0x2Eh			

NXWUE *- x negative (x-) mask for WUF, 0=disable, 1=enable.*
PXWUE *- x positive (x+) mask for WUF, 0=disable, 1=enable.*
NYWUE *- y negative (y-) mask for WUF, 0=disable, 1=enable.*
PYWUE *- y positive (y+) mask for WUF, 0=disable, 1=enable.*
NZWUE *- z negative (z-) mask for WUF, 0=disable, 1=enable.*
PZWUE *- z positive (z+) mask for WUF, 0=disable, 1=enable.*

AUX_I2C_CTRL_REG1

Read/Write control register: Factory programmed power up/reset default value (0x00h)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reserved	Reserved	DATA2_2	DATA2_1	DATA2_0	DATA1_2	DATA1_1	DATA1_0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^2C Address: 0x30h			

DATA1(2:0): *Number of bytes read back via Auxiliary I^2C bus from device 1*

DATA1_2	DATA1_1	DATA1_0	No. of Bytes
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	DNE

Table 16. Number of Bytes to Read from Device 1

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DATA2(2:0): *Number of bytes read back via Auxiliary I^2C bus from device 2*

DATA2_2	DATA2_1	DATA2_0	No. of Bytes
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	DNE

Table 17. Number of Bytes to Read from Device 2

AUX_I2C_CTRL_REG2

Read/Write control register: Factory programmed power up/reset default value (0x00h)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reserved	Reserved	Reserved	Reserved	Reserved	PULL_UP	BYPASS	AUX_EN	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000010
					I^2C Address: 0x31h			

PULL_UP *indicates the state of the internal pull-up resistor on the Auxiliary I^2C Bus*

PULL_UP = 0 – Internal 1.5kΩ pull-up resistor disengaged

PULL_UP = 1 – Internal 1.5kΩ pull-up resistor engaged

BYPASS *indicates the state of the Auxiliary I^2C Bus*

BYPASS = 0 – Auxiliary I^2C Bus is in Host Mode

BYPASS = 1 – Auxiliary I^2C Bus is in Bypass Mode

AUX_EN *enables or disables the Auxiliary I^2C Bus*

AUX_EN = 0 – Auxiliary I^2C Bus is disabled

AUX_EN = 1 – Auxiliary I^2C Bus is enabled

AUX_I2C_SAD1

Read/Write that should be used to store the SAD for auxiliary I^2C device 1.

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R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
SAD1_6	SAD1_5	SAD1_4	SAD1_3	SAD1_2	SAD1_1	SAD1_0	-	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^2C Address: 0x32h			

AUX_I2C_REG1

Read/Write that should be used to store the starting data register address for auxiliary I^2C device 1.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
REG1_7	REG1_6	REG1_5	REG1_4	REG1_3	REG1_2	REG1_1	REG1_0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^2C Address: 0x33h			

AUX_I2C_CNTL1

Register address for enable/disable control register for auxiliary I^2C device 1.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
CNTL1_7	CNTL1_6	CNTL1_5	CNTL1_4	CNTL1_3	CNTL1_2	CNTL1_1	CNTL1_0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^2C Address: 0x34h			

AUX_I2C_BIT1

Bit that controls the enable/disable in the control register for auxiliary I^2C device 1.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
BIT1_7	BIT1_6	BIT1_5	BIT1_4	BIT1_3	BIT1_2	BIT1_1	BIT1_0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^2C Address: 0x35h			

AUX_I2C_DELAY1

Bit that controls the delay for auxiliary I^2C device 1.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
BIT1_7	BIT1_6	BIT1_5	BIT1_4	BIT1_3	BIT1_2	BIT1_1	BIT1_0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^2C Address: 0x36h			

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AUX_I2C_SAD2

Read/Write that should be used to store the SAD for auxiliary I²C device 2.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
SAD2_6	SAD2_5	SAD2_4	SAD2_3	SAD2_2	SAD2_1	SAD2_0	Reserved	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I²C Address: 0x37h			

AUX_I2C_REG2

Read/Write that should be used to store the starting data register address for auxiliary I²C device 2.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
REG2_7	REG2_6	REG2_5	REG2_4	REG2_3	REG2_2	REG2_1	REG2_0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I²C Address: 0x38h			

AUX_I2C_CNTL2

Register address for enable/disable control register for auxiliary I²C device 2.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
CNTL2_7	CNTL2_6	CNTL2_5	CNTL2_4	CNTL2_3	CNTL2_2	CNTL2_1	CNTL2_0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I²C Address: 0x39h			

AUX_I2C_BIT2

Bit that controls the enable/disable in the control register for auxiliary I²C device 2.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
BIT2_7	BIT2_6	BIT2_5	BIT2_4	BIT2_3	BIT2_2	BIT2_1	BIT2_0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I²C Address: 0x3Ah			

AUX_I2C_DELAY2

Bit that controls the delay for auxiliary I²C device 2.

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R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
BIT2_7	BIT2_6	BIT2_5	BIT2_4	BIT2_3	BIT2_2	BIT2_1	BIT2_0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I²C Address: 0x3Bh			

SRT

This register has the value of 55h normally. When COTC bit in CTRL_REG2 0x2Bh is set, this value changes to 0xAAh. After reading this register it is changed back to value 0x55h and COTC cleared.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ATH_7	ATH_6	ATH_5	ATH_4	ATH_3	ATH_2	ATH_1	ATH_0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	01010101
					I²C Address: 0x3Ch			

WAKEUP_THRESHOLD

This register sets the Active Threshold for wake-up (motion detect) interrupt. The KXG03 will ship from the factory with this value set to correspond to a change in acceleration of 0.5g. Note that to change the value of this register, the ACCEL_STBY bit must first be set to “1”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ATH_7	ATH_6	ATH_5	ATH_4	ATH_3	ATH_2	ATH_1	ATH_0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00001000
					I²C Address: 0x3Dh			

WAKEUP_TIMER

This register sets the time motion must be present before a wake-up interrupt is set. Every count is calculated as 1/OWUF delay period. OWUF is set in CTRL_REG2. Note that to change the value of this register the ACCEL_STBY bit must first be set to “1”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
WUTH7	WUTH6	WUTH5	WUTH4	WUTH3	WUTH2	WUTH1	WUTH0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I²C Address: 0x3Eh			

BTS_THRESHOLD

This register sets the threshold for back to sleep (motion detect) interrupt. The KXG03 will ship from the factory with this value set to correspond to a change in acceleration of 0.5g. Note that to change the value of this register, the ACCEL_STBY bit must first be set to “1”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
BTH_7	BTH_6	BTH_5	BTH_4	BTH_3	BTH_2	BTH_1	BTH_0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00001000
					I²C Address: 0x3Fh			

BTS_TIMER

This register sets the time motion must be present before a back to sleep interrupt is set. Every count is calculated as 16/OSA delay period. OSA is set in ODCNTL. Note that to change the value of this register the ACCEL_STBY bit must first be set to “1”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
BTSC7	BTSC6	BTSC5	BTSC4	BTSC3	BTSC2	BTSC1	BTSC0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I²C Address: 0x40h			

BUF_THRESH_H

Read/write control register that controls the buffer sample threshold.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
SMP_TH9	SMP_TH8	SMP_TH7	SMP_TH6	SMP_TH5	SMP_TH4	SMP_TH3	SMP_TH2	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I²C Address: 0x77h			

BUF_THRESH_L

Read/write control register that controls the buffer sample threshold.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	SMP_TH1	SMP_TH0	Reset Value

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I²C Address: 0x78h			

SMP_TH[9:0] Sample Threshold*; determines the number of data bytes that will trigger a watermark interrupt or will be saved prior to a trigger event. The maximum number of data bytes is 1024.*

Buffer Model	Sample Function
Bypass	None
FIFO	Specifies how many buffer samples are needed to trigger a watermark interrupt.
Stream	Specifies how many buffer samples are needed to trigger a watermark interrupt.
Trigger	Specifies how many buffer samples before the trigger event are retained in the buffer.
FILO	Specifies how many buffer samples are needed to trigger a watermark interrupt.

Table 18. Sample Threshold Operation by Buffer Mode

BUF_CTRL1

Read/write control register that controls sample buffer operation.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
BUFE	Reserved	BUF_FIE	BUF_YAS	Reserved	Reserved	BUF_M1	BUF_M0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I²C Address: 0x79h			

BUFE *controls activation of the sample buffer.*
BUFE = 0 – sample buffer inactive
BUFE = 1 – sample buffer active (only if RES=1)

BUF_FIE *controls the buffer full interrupt*
BUF_FIE = 0 – the buffer full interrupt, BFI is disabled
BUF_FIE = 1 – the buffer full interrupt, BFI will be triggered when the buffer is full

BUF_YAS *controls the data format from AUX_IN1 into the buffer*
BUF_RES = 0 – data is passed into the buffer as read back from AUX_IN1

BUF_RES = 1 – expected data is from YAS530 and is accordingly reformatted prior to entry into the buffer

BUF_M1, BUF_M0 *selects the operating mode of the sample buffer per Table 19.*

BUF_M1	BUF_M0	Mode	Description
0	0	FIFO	The buffer collects 1024 bytes of data until full, collecting new data only when the buffer is not full.
0	1	Stream	The buffer holds the last 1024 bytes of data. Once the buffer is full, the oldest data is discarded to make room for newer data.
1	0	Trigger	When a trigger event occurs (logic high input on TRIG pin), the buffer holds the last data set of SMP[6:0] samples before the trigger event and then continues to collect data until full. New data is collected only when the buffer is not full.
1	1	FILO	The buffer holds the last 1024 bytes of data. Once the buffer is full, the oldest data is discarded to make room for newer data. Reading from the buffer in this mode will return the most recent data first.

Table 19. Selected Buffer Mode

BUF_CTRL2

Read/write control register that controls sample buffer operation.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
BUF_GYR	BUF_ACC	Reserved	Reserved	Reserved	Reserved	Reserved	BUF_TEMP	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^2C Address: 0x7Ah			

BUF_GYR *controls the Gyroscope input into the sample buffer.*
BUF_GYR = 0 – Gyroscope data is not input into the sample buffer
BUF_GYR = 1 – Gyroscope data is input into the sample buffer

BUF_ACC *controls the Accelerometer input into the sample buffer.*
BUF_ACC = 0 – Accelerometer data is not input into the sample buffer
BUF_ACC = 1 – Accelerometer data is input into the sample buffer

BUF_TEMP *controls the Temperature input into the sample buffer.*

BUF_TEMP = 0 – Temperature data is not input into the sample buffer
BUF_TEMP = 1 – Temperature data is input into the sample buffer

BUF_STATUS_H

This register reports the status of the sample buffer.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SMP_LEV9	SMP_LEV8	SMP_LEV7	SMP_LEV6	SMP_LEV5	SMP_LEV4	SMP_LEV3	SMP_LEV2
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x7Bh		

BUF_STATUS_L

This register reports the status of the sample buffer.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	SMP_LEV1	SMP_LEV0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x7Ch		

SMP_LEV[9:0] Sample Level*; reports the number of data bytes that have been stored in the sample buffer. If this register reads 0, no data has been stored in the buffer.*

BUF_STATUS_REG

This register reports the status of the sample buffer trigger function.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BUF_TRIG	0	0	0	0	0	0	0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x7Dh		

BUF_TRIG *reports the status of the buffer's trigger function if this mode has been selected. When using trigger mode, a buffer read should only be performed after a trigger event.*

BUF_CLEAR

Latched buffer status information and the entire sample buffer are cleared when any data is written to this register.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	X	X	X	X	X	X

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Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I²C Address: 0x7Eh		

BUF_READ

Data in the buffer can be read according to the BUF_RES and BUF_M settings in BUF_CTRL2 by executing this command. More samples can be retrieved by continuing to toggle SCL after the read command is executed. Data should by using auto-increment. Additional samples cannot be written to the buffer while data is being read from the buffer using auto-increment mode. Output data is in 2's Complement format.

R	R	R	R	R	R	R	R
X	X	X	X	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I²C Address: 0x7Fh		

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Sample Buffer Feature Description

The 1024 byte sample buffer feature of the KXG03 accumulates and outputs data based on how it is configured. There are 4 buffer modes available. Data is collected at the ODR specified by OSAA:OSAD in the Output Data Control Register. Each buffer mode accumulates data, reports data, and interacts with status indicators in a slightly different way.

FIFO Mode

Data Accumulation

Sample collection stops when the buffer is full.

Data Reporting

Data is reported with the oldest byte of the oldest sample first (X_L or X based on resolution).

Status Indicators

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or reading greater than SMPX.

BUF_RES=0:
SMPX = SMP_LEV[9:0] – SMP_TH[9:0]

Equation 5. Samples Above Sample Threshold

Stream Mode

Data Accumulation

Sample collection continues when the buffer is full; older data is discarded to make room for newer data.

Data Reporting

Data is reported with the oldest sample first (uses FIFO read pointer).

Status Indicators

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or explicitly reading greater than SMPX samples (calculated with Equation 5).

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Trigger Mode

Data Accumulation

When a logic high signal occurs on the TRIG pin, the trigger event is asserted and SMP[9:0] samples prior to the event are retained. Sample collection continues until the buffer is full.

Data Reporting

Data is reported with the oldest sample first (uses FIFO read pointer).

Status Indicators

When a physical interrupt occurs and there are at least SMP[9:0] samples in the buffer, BUF_TRIG in BUF_STATUS_REG2 is asserted.

FILO Mode

Data Accumulation

Sample collection continues when the buffer is full; older data is discarded to make room for newer data.

Data Reporting

Data is reported with the newest byte of the newest sample first (Z_H or Z based on resolution).

Status Indicators

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or explicitly reading greater than SMPX samples (calculated with Equation 5).

Buffer Operation

The following diagrams illustrate the operation of the buffer conceptually. Actual physical implementation has been abstracted to offer a simplified explanation of how the different buffer modes operate. Figure 3 represents a high-resolution 3-axis sample within the buffer. Figures 4-12 represent a 10-sample version of the buffer (for simplicity), with Sample Threshold set to 8.

Regardless of the selected mode, the buffer fills sequentially, one byte at a time. Figure 3 shows one 6-byte data sample. Note the location of the FILO read pointer versus that of the FIFO read pointer.

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	Index	Byte	
	0	X_L	<---- FIFO read pointer
	1	X_H	
	2	Y_L	
	3	Y_H	
	4	Z_L	
	5	Z_H	<---- FILO read pointer
buffer write pointer ---->	6		

Figure 3. One Buffer Sample

Regardless of the selected mode, the buffer fills sequentially, one sample at a time. Note in Figure 4 the location of the FILO read pointer versus that of the FIFO read pointer. The buffer write pointer shows where the next sample will be written to the buffer.

	Index	Sample	
	0	Data0	⟵ FIFO read pointer
	1	Data1	
	2	Data2	⟵ FILO read pointer
buffer write pointer ⟶	3		
	4		
	5		
	6		
	7		⟵ Sample Threshold
	8		
	9		

Figure 4. Buffer Filling

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The buffer continues to fill sequentially until the Sample Threshold is reached. Note in Figure 5 the location of the FILO read pointer versus that of the FIFO read pointer.

	Index	Sample	
	0	Data0	← FIFO read pointer
	1	Data1	
	2	Data2	
	3	Data3	
	4	Data4	
	5	Data5	
	6	Data6	← FILO read pointer
buffer write pointer →	7		← Sample Threshold
	8		
	9		

Figure 5. Buffer Approaching Sample Threshold

In FIFO, Stream, and FILO modes, a watermark interrupt is issued when the number of samples in the buffer reaches the Sample Threshold. In trigger mode, this is the point where the oldest data in the buffer is discarded to make room for newer data.

	Index	Sample	
	0	Data0	← FIFO read pointer
	1	Data1	
	2	Data2	
	3	Data3	
	4	Data4	
	5	Data5	
	6	Data6	
	7	Data7	← Sample Threshold/FILO read pointer
buffer write pointer →	8		
	9		

Figure 6. Buffer at Sample Threshold

In trigger mode, data is accumulated in the buffer sequentially until the Sample Threshold is reached. Once the Sample Threshold is reached, the oldest samples are discarded when new samples are collected. Note in Figure 7 how Data0 was thrown out to make room for Data8.

	Index	Sample	
	0	Data1	← Trigger read pointer
	1	Data2	
	2	Data3	
	3	Data4	
	4	Data5	
	5	Data6	
	6	Data7	
Trigger write pointer →	7	Data8	← Sample Threshold
	8		
	9		

Figure 7. Additional Data Prior to Trigger Event

After a trigger event occurs, the buffer no longer discards the oldest samples, and instead begins accumulating samples sequentially until full. The buffer then stops collecting samples, as seen in Figure 8. This results in the buffer holding SMP_TH[9:0] samples prior to the trigger event, and SMPX samples after the trigger event.

Index	Sample	
0	Data1	← Trigger read pointer
1	Data2	
2	Data3	
3	Data4	
4	Data5	
5	Data6	
6	Data7	
7	Data8	← Sample Threshold

8	Data9
9	Data10

Figure 8. Additional Data After Trigger Event

In FIFO, Stream, FILO, and Trigger (after a trigger event has occurred) modes, the buffer continues filling sequentially after the Sample Threshold is reached. Sample accumulation after the buffer is full depends on the selected operation mode. FIFO and Trigger modes stop accumulating samples when the buffer is full, and Stream and FILO modes begin discarding the oldest data when new samples are accumulated.

Index	Sample	
0	Data0	← FIFO read pointer
1	Data1	
2	Data2	
3	Data3	
4	Data4	
5	Data5	
6	Data6	
7	Data7	← Sample Threshold
8	Data8	
9	Data9	← FILO read pointer

Figure 9. Buffer Full

After the buffer has been filled in FILO or Stream mode, the oldest samples are discarded when new samples are collected. Note in Figure 10 how Data0 was thrown out to make room for Data10.

Index	Sample	
0	Data1	← FIFO read pointer
1	Data2	
2	Data3	
3	Data4	
4	Data5	
5	Data6	

6	Data7	
7	Data8	← Sample Threshold
8	Data9	
9	Data10	← FILO read pointer

Figure 10. Buffer Full – Additional Sample Accumulation in Stream or FILO Mode

In FIFO, Stream, or Trigger mode, reading one sample from the buffer will remove the oldest sample and effectively shift the entire buffer contents up, as seen in Figure 11.

	Index	Sample	
	0	Data1	← FIFO read pointer
	1	Data2	
	2	Data3	
	3	Data4	
	4	Data5	
	5	Data6	
	6	Data7	
	7	Data8	← Sample Threshold
	8	Data9	← FILO read pointer
buffer write pointer →	9		

Figure 11. FIFO Read from Full Buffer

In FILO mode, reading one sample from the buffer will remove the newest sample and leave the older samples untouched, as seen in Figure 12.

Index	Sample	
0	Data0	← FIFO read pointer
1	Data1	
2	Data2	
3	Data3	
4	Data4	
5	Data5	

6	Data6	
7	Data7	⟵ Sample Threshold
8	Data8	⟵ FILO read pointer
buffer write pointer ⟶ 9		

Figure 12. FILO Read from Full Buffer

Revision History

REVISION	DESCRIPTION	DATE
0.1	Initial preliminary release	26 Mar 2015