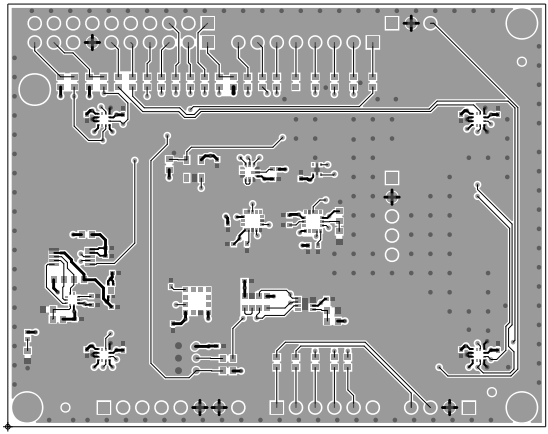
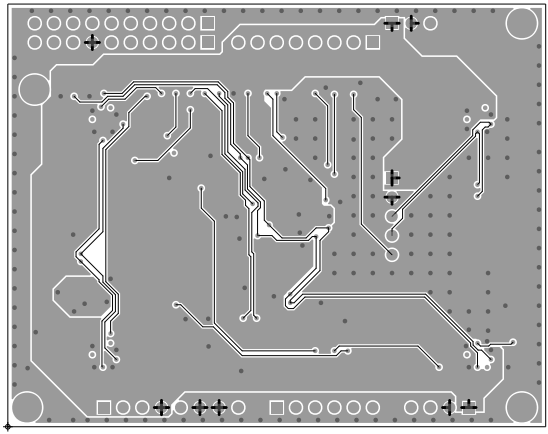
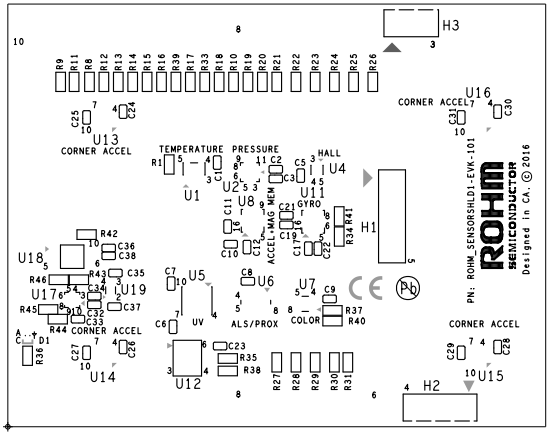


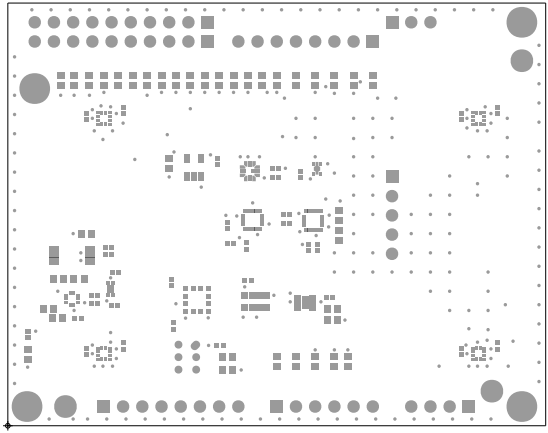
ROHM SEMICONDUCTOR	LAYER: 01 PRIMARY-SIDE	COMPANY NAME: ROHM SEMICONDUCTOR USA		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMAL X ±.1 XX ±.03 XXX ±.010 ANGLE ±30 MACH FINISH ✓
	DESIGNER: PTEC	PROJECT NAME: SENSORSHLD1-EVK-101		
	CHECKER: ROHM SEMICONDUCTOR			
	DATE: 2016-03-24	PROJECT NUMBER: NUMBER	REV. 01	
	JOB#:			



ROHM SEMICONDUCTOR	LAYER:02 SECONDARY-SIDE	COMPANY NAME: ROHM SEMICONDUCTOR USA	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
	DESIGNER: PTEC	PROJECT NAME: SENSORSHLD1-EVK-101	TOLERANCES
	CHECKER:ROHM SEMICONDUCTOR		DECIMAL ANGLE
	DATE: 2016-03-24	PROJECT NUMBER: NUMBER	REV. 01
	JOB#:		X ±.1 ±30 XX ±.03 MACH FINISH XXX±.010 √

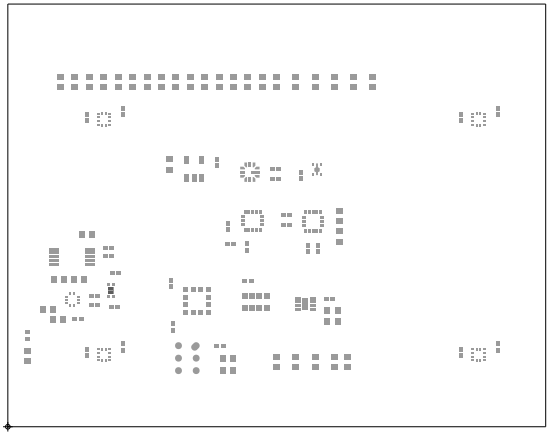


ROHM SEMICONDUCTOR	SILKSCREEN PRIMARY-SIDE	COMPANY NAME: ROHM SEMICONDUCTOR USA		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
	DESIGNER: PTEC	PROJECT NAME: SENSORSHLD1-EVK-101		TOLERANCES DECIMAL X±.1 XX±.03 XXX±.010 ANGLE ±30 MACH FINISH ✓
	CHECKER: ROHM SEMICONDUCTOR			
	DATE: 2016-03-24	PROJECT NUMBER:	REV.	
	JOB#:	NUMBER	01	



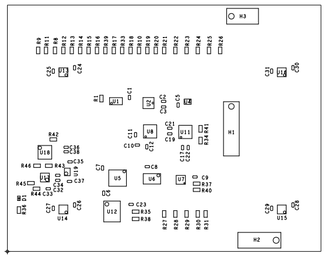
ROHM SEMICONDUCTOR	SOLDERMASK PRIMARY-SIDE	COMPANY NAME: ROHM SEMICONDUCTOR USA	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
	DESIGNER: PTEC	PROJECT NAME: SENSORSHLD1-EVK-101	TOLERANCES DECIMAL X±.1 XX±.03 XXX±.010 ANGLE ±30 MACH FINISH ✓
	CHECKER: ROHM SEMICONDUCTOR		
	DATE: 2016-03-24	PROJECT NUMBER: NUMBER / REV. 01	
	JOB#:		

ROHM SEMICONDUCTOR	SOLDERMASK SECONDARY-SIDE	COMPANY NAME: ROHM SEMICONDUCTOR USA	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
	DESIGNER: PTEC	PROJECT NAME: SENSORSHLD1-EVK-101	TOLERANCES
	CHECKER: ROHM SEMICONDUCTOR		DECIMAL ANGLE
	DATE: 2016-03-24	PROJECT NUMBER: NUMBER	REV. 01
	JOB#:		X ±.1 ±30
			XX ±.03 MACH FINISH
			XXX ±.010 √



ROHM SEMICONDUCTOR	PASTEMASK PRIMARY-SIDE	COMPANY NAME: ROHM SEMICONDUCTOR USA		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMAL ANGLE X ±.1 ±30 XX ±.03 MACH FINISH XXX ±.010 ✓
	DESIGNER: PTEC	PROJECT NAME: SENSORSHLD1-EVK-101		
	CHECKER: ROHM SEMICONDUCTOR			
	DATE: 2016-03-24	PROJECT NUMBER: NUMBER	REV. 01	
	JOB#:			

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



ASSEMBLY
PRIMARY-SIDE

ROHM SEMICONDUCTOR	ASSEMBLY TOP	COMPANY NAME: ROHM SEMICONDUCTOR USA		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
	DESIGNER: PTEC	PROJECT NAME: SENSORSHLD1-EVK-101		TOLERANCES
	CHECKER: INITIAL			DECIMAL ANGLE
	DATE: 2016-03-24	ASSEMBLY NUMBER: NUMBER	REV. 01	SHEET: 1 OF 2
	JOB#:			X.X ±.1 ±30 XX ±.03 MACH FINISH XXX ±.010

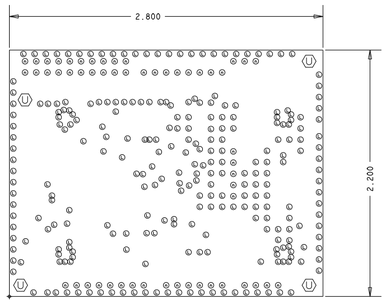
LAYER STACKING DETAIL

Layer #	Layer Type	Copper Weight (Oz)	Copper Thickness (Mils)	Material Type - Ply	Dielectric Thickness (Mils)
Plating			1.35		
1	SIG	0.5	0.65		
				Prepreg	58.00
2	SIG	0.5	0.65		
Plating			1.35		

Total Overal Thickness: 62.00+/-10%Mils

Material Ordering Info (used in lieu of Fasttrak data)

Panel Size	------
Number Up	------
Number of Parts Due	------
Prepregs Construction Added?	------
Material Ply Specified	------
Material Type (ie Nelco-29, 370 HR, ...)	FR4



FAB NOTE

DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
⊙	12.0	+3.0/-10.0	PLATED	264
⊙	40.0	+3.0/-3.0	PLATED	54
Ⓤ	125.0	+3.0/-3.0	PLATED	4

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

NOTES:

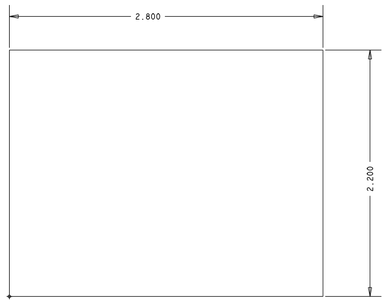
1. Specifications.
   A. Fabricate IAW IPC600, latest revision.
   B. Producibility study - It is the respondsibility of the supplier to conduct a thorough review of the artwork and media for manufacturability in the supplier's process compliance to all applicable specifications. Customer must be advised in writing (in advance of manufacturing) of any changes, revisions,or corrections made or recommendations to ensure conformance to standards, and of any specifications that cannot be met.
   D. This drawing is to be used in conjunction with the provided gerber and drill data when applicable.
   E. All notes are "Unless Otherwise Specified."
2. Material
   A. FR4.
   B. Color to be opaque.
3. Soldermask
   Solder mask both sides with (green color) liquid photoimageable soldermask, 003 max. thickness.
   Soldermask over bare copper.
   Soldermask is allowed in via holes.
4. Drilling
   A. All hole diameters are finished sizes.
   B. All hole to be +/- .003 from true position unless otherwise specified.
   C. All hole diameters to be +/- .003 unless otherwise specified.
   D. An NC drill file has been supplied - see drill table.
5. Finish
   A. Plate thru with copper .0010 min to .002 max. thickness drill size dimension apply after plating.
   B. Use gold immersion over nickel.
   C. Finished boards shall not have nicks, scratches, voids, exposed copper, poor plating, all misdrilled holes.
6. Silkscreen
   A. Silkscreen using white non-conductive epoxy or equivalent (both sides).
   B. No silkscreen allowed on exposed lands.
   C. Silkscreen must be a minimum of 3mm away form fiducial marks.
   D. Minimum clearance between silkscreen legend and vias, pads, or holes to be .005.
   E. Silkscreen is allowed in via holes.
7. Electrical Test
   A. All boards shall be 100% electrically tested for opens/short at 10 volts. MIL-SPEC boards to be tested at 40 volts.
   B. Apply test stamp in non-legend area on solder side of PCB.
   C. Test is required on both sides of the board.
8. Cleanliness
   A. Boards shall be free of fiber glass dust or any other foreign material.
   B. Finished boards must conform to 0.01 MG/IN max NAcL ionic contamination as meaxured by the omega meter 600SMD.
9. Packaging
   There shall be a max of 25 units per package, individually wrapped, and shipped in cardboard cratons with sufficient surrounding material to prevend shipping damage.
10. Bow and Twist
    Bow and twist to be .007 IN/IN or .090 max according to IPC-A-600D.
11. Inspection
    A.Automatic optical inspection of all layers required.
    B.The impedance should be controlled by stackup layer.
12. Inside corners should be rounded-off
13. Changes to board geometries and apertures are not allowed unless they are approved by customer.
14. Rounding is allowed on 90 degree corners with the size of standard routing bit.

ROHM SEMICONDUCTOR

FAB DRAWING	COMPANY NAME: ROHM SEMICONDUCTOR USA		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DESIGNER: PTEC	PROJECT NAME: SENSORSHLD1-EVK-101		TOLERANCES DECIMAL ANGLE X ± .1 ± .30 XX ± .03 MACH FINISH XXX ± .010 ✓
CHECKER: INITIAL			
DATE: 2016-03-24	FAB NUMBER: NUMBER	REV. 01	SHEET: 1 OF 2
JOB#:			

ART FILM - PANEL

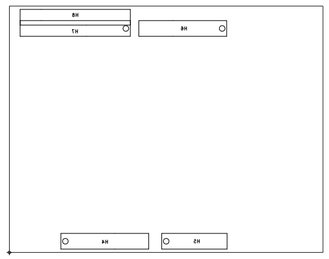
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



ROHM SEMICONDUCTOR	PANEL DRAWING	COMPANY NAME: ROHM SEMICONDUCTOR USA	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
	DESIGNER: PTEC	PROJECT NAME: SENSORSHLD1-EVK-101	TOLERANCES DECIMAL ANGLE X ± 1 ± 30 XX ± .03 MACH FINISH XXX ± .010
	CHECKER: INITIAL		
	DATE: 2016-03-24	FAB NUMBER: NUMBER / REV.: 01 / SHEET: 2 OF 2	
	JOB#:		

ART FILM - PANEL

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



ASSEMBLY
SECONDARY-SIDE

DESIGNER: PTEC	ASSEMBLY SECONDARY-SIDE
CHECKER: INITIAL	
DATE: 2016-03-24	
JOB#:	

ROHM SEMICONDUCTOR

COMPANY NAME: ROHM SEMICONDUCTOR USA

PROJECT NAME: SEMISOR5HL01-EVK-101

REV. 01 | SHEET: 2 OF 2

TOLERANCES
DECIMAL X.X ±.1 ANGLE ±3.0
XXX ±.010 MACH FINISH

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

ROHM SEMICONDUCTOR	SILKSCREEN SECONDARY-SIDE	COMPANY NAME : ROHM SEMICONDUCTOR USA	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
	DESIGNER : PTEC	PROJECT NAME : SENSORSHLD1-EVK-101	TOLERANCES
	CHECKER : ROHM SEMICONDUCTOR		DECIMAL ANGLE
	DATE : 2016-03-24	PROJECT NUMBER :	REV . X ±.1 ±30
	JOB# :	NUMBER	01 XX ±.03 MACH FINISH XXX±.010 √