

ROHM
SEMICONDUCTOR

LAYER: 01
PRIMARY-SIDE

DESIGNER: PTEC

CHECKER: ROHM SEMICONDUCTOR

DATE: 2016-02-26

JOB#:

COMPANY NAME:

ROHM SEMICONDUCTOR USA

PROJECT NAME:

EVK1 PN: BM92T30-HOST-EVK-101

PROJECT NUMBER:

NUMBER

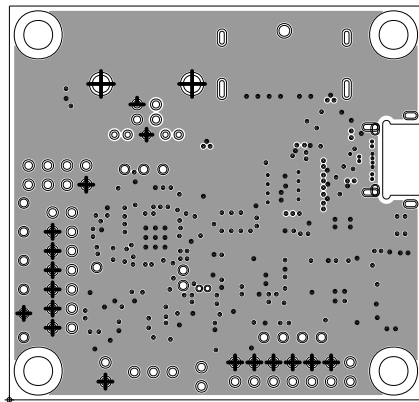
REV.


03

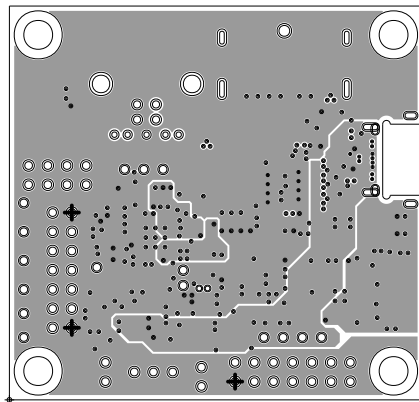
UNLESS OTHERWISE
SPECIFIED DIMENSIONS
ARE IN INCHES


TOLERANCES

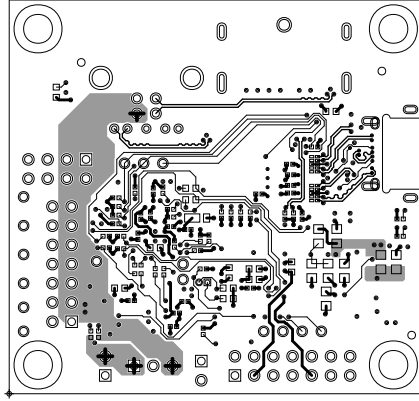
DECIMAL	ANGLE
X ± .1	± 30
XX ± .03	MACH FINISH
XXX ± .010	✓



	L2_GND	COMPANY NAME: ROHM SEMICONDUCTOR USA		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMAL ANGLE X ± .1 ± 30 XX ± .03 MACH FINISH XXX ± .010 ✓
	DESIGNER: PTEC	PROJECT NAME:		
	CHECKER: ROHM SEMICONDUCTOR	EVK1 PN:BM92T30-HOST-EVK-101		
	DATE: 2016-02-26	PROJECT NUMBER:		
	JOB#:	NUMBER		
			REV. 03	



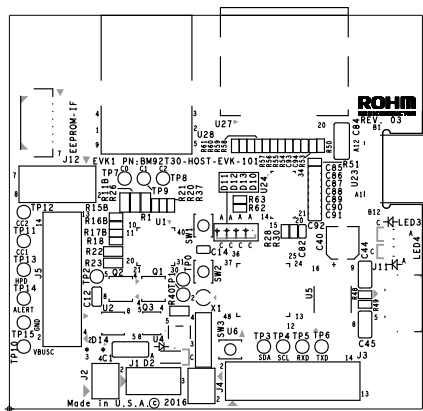
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	DESIGNER: PTEC	PROJECT NAME:		
	CHECKER: ROHM SEMICONDUCTOR	EVK1 PN:BM92T30-HOST-EVK-101		
	DATE: 2016-02-26	PROJECT NUMBER:		
	JOB#:	NUMBER		
			REV. 03	



ROHM
SEMICONDUCTOR

TOLERANCES DECIMAL X ±.1 ANGLE .30 H212H XX ±.03 MACH FINISH XXX ±.010	NUMBER		PROJECT NUMBER:	REV. 03
	EVK1 PN:BM95T30-H02T-EVK-101		PROJECT NAME:	
	ROHM SEMICONDUCTOR USA		COMPANY NAME:	
	SECONDARY-SIDE		LAYER: 04	
	JOB#:		DATE: 2018-05-28	
		CHECKER: ROHM SEMICONDUCTOR	DESIGNER: PTEC	

UNLESS OTHERWISE
SPECIFIED DIMENSIONS
ARE IN INCHES



ROHM
SEMICONDUCTOR

SILKSCREEN
PRIMARY-SIDE

DESIGNER: PTEC

CHECKER: ROHM SEMICONDUCTOR

DATE: 2016-02-26

JOB#:

COMPANY NAME:

ROHM SEMICONDUCTOR USA

PROJECT NAME:

EVK1 PN:BM92T30-HOST-EVK-101

PROJECT NUMBER:

NUMBER


REV.

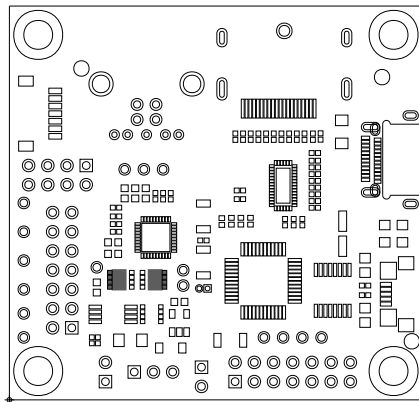
03


UNLESS OTHERWISE
SPECIFIED DIMENSIONS
ARE IN INCHES

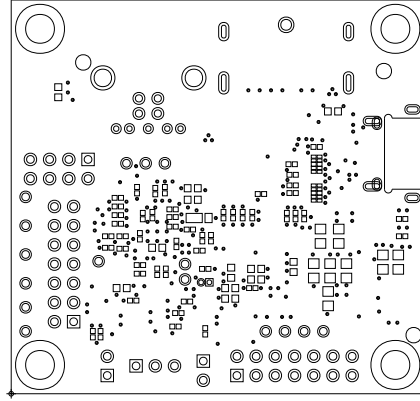
TOLERANCES


DECIMAL	ANGLE
X ± .1	± 30
XX ± .03	MACH FINISH
XXX ± .010	✓

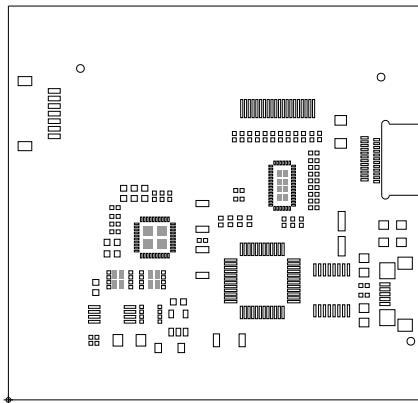
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	NUMBER		PROJECT NUMBER:		REV.		EVAL PN: BM5T30-H02T-EVK-101		PROJECT NAME:
	03								ROHM SEMICONDUCTOR USA
	XXX ± 0.10 XX ± 0.03 X ± 0.01 FINISH MACH ANGLE DECIMAL TOLERANCES ARE IN INCHES UNLESS OTHERWISE SPECIFIED								




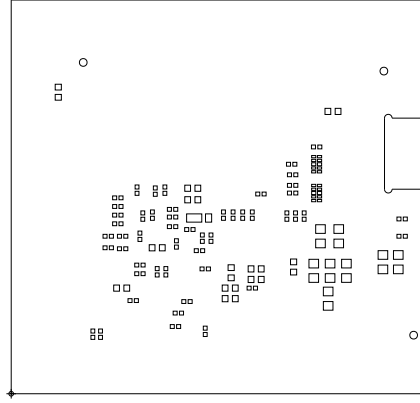
	SOLDERMASK PRIMARY-SIDE	COMPANY NAME: ROHM SEMICONDUCTOR USA		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMAL ANGLE X ± .1 ±30 XX ± .03 MACH FINISH XXX ± .010 ✓
	DESIGNER: PTEC	PROJECT NAME:		
	CHECKER: ROHM SEMICONDUCTOR	EVK1 PN:BM92T30-HOST-EVK-101		
	DATE: 2016-02-26	PROJECT NUMBER:		
	JOB#:	NUMBER		
			REV. 03	




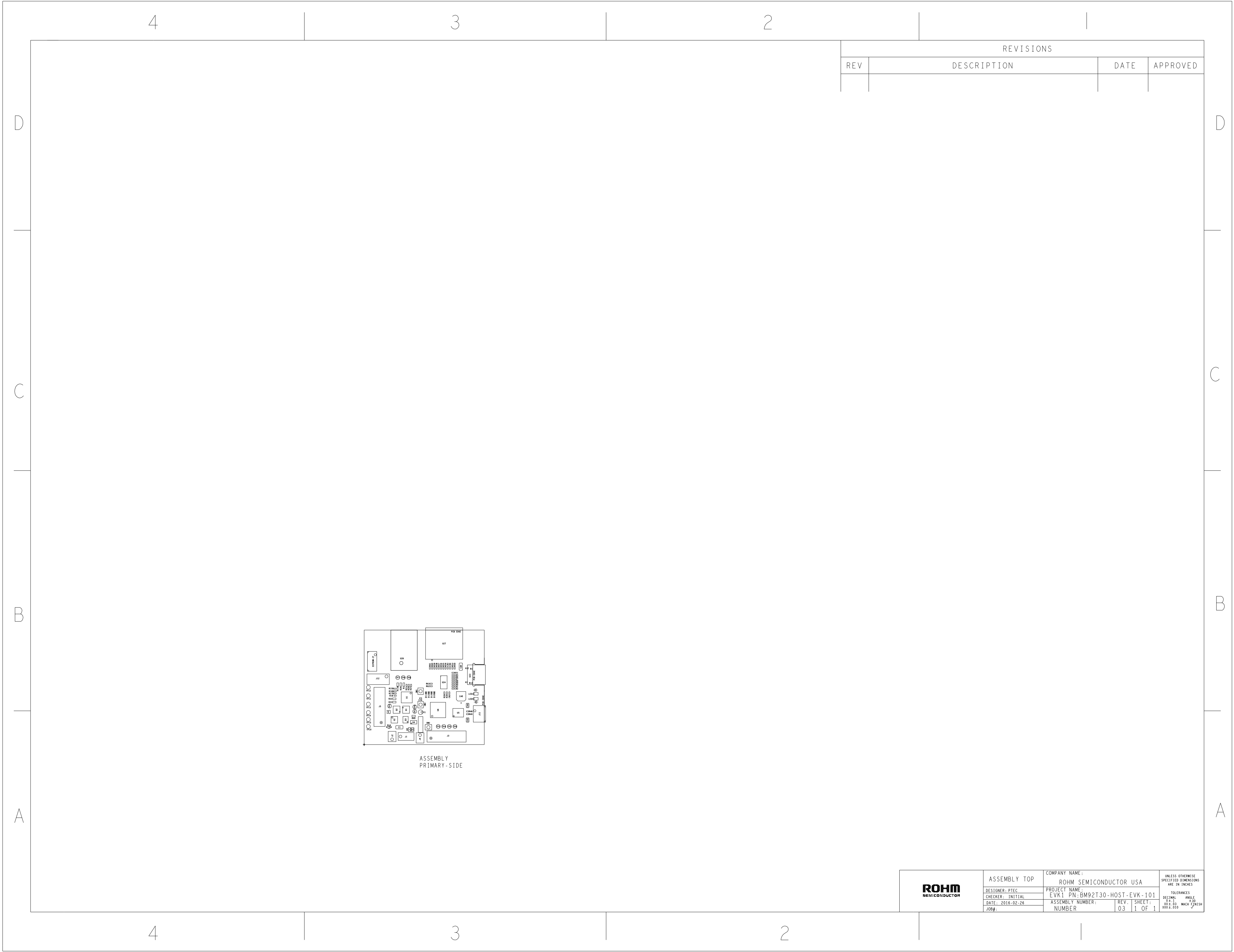
	JOB#:		COMPANY NAME: ROHM SEMICONDUCTOR USA		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
	DATE: 2010-05-20		PROJECT NAME: EVK1 PN: BM05T30-H02T-EVK-101		
	CHECKER: ROHM SEMICONDUCTOR		PROJECT NUMBER: 03		
	DESIGNER: PTEC		REV. 03		
TOLERANCES DECIMAL X ± .1 X ± .03 XX ± .010 MACH FINISH ✓					



	PASTEMASK PRIMARY-SIDE	COMPANY NAME: ROHM SEMICONDUCTOR USA		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMAL ANGLE X ± .1 ±30 XX ± .03 MACH FINISH XXX ± .010 ✓
	DESIGNER: PTEC	PROJECT NAME:		
	CHECKER: ROHM SEMICONDUCTOR	EVK1 PN:BM92T30-HOST-EVK-101		
	DATE: 2016-02-26	PROJECT NUMBER:		
	JOB#:	NUMBER		
			REV. 03	

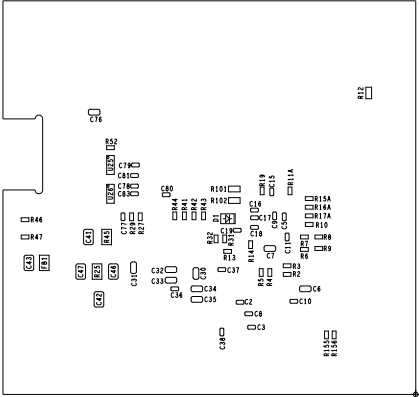
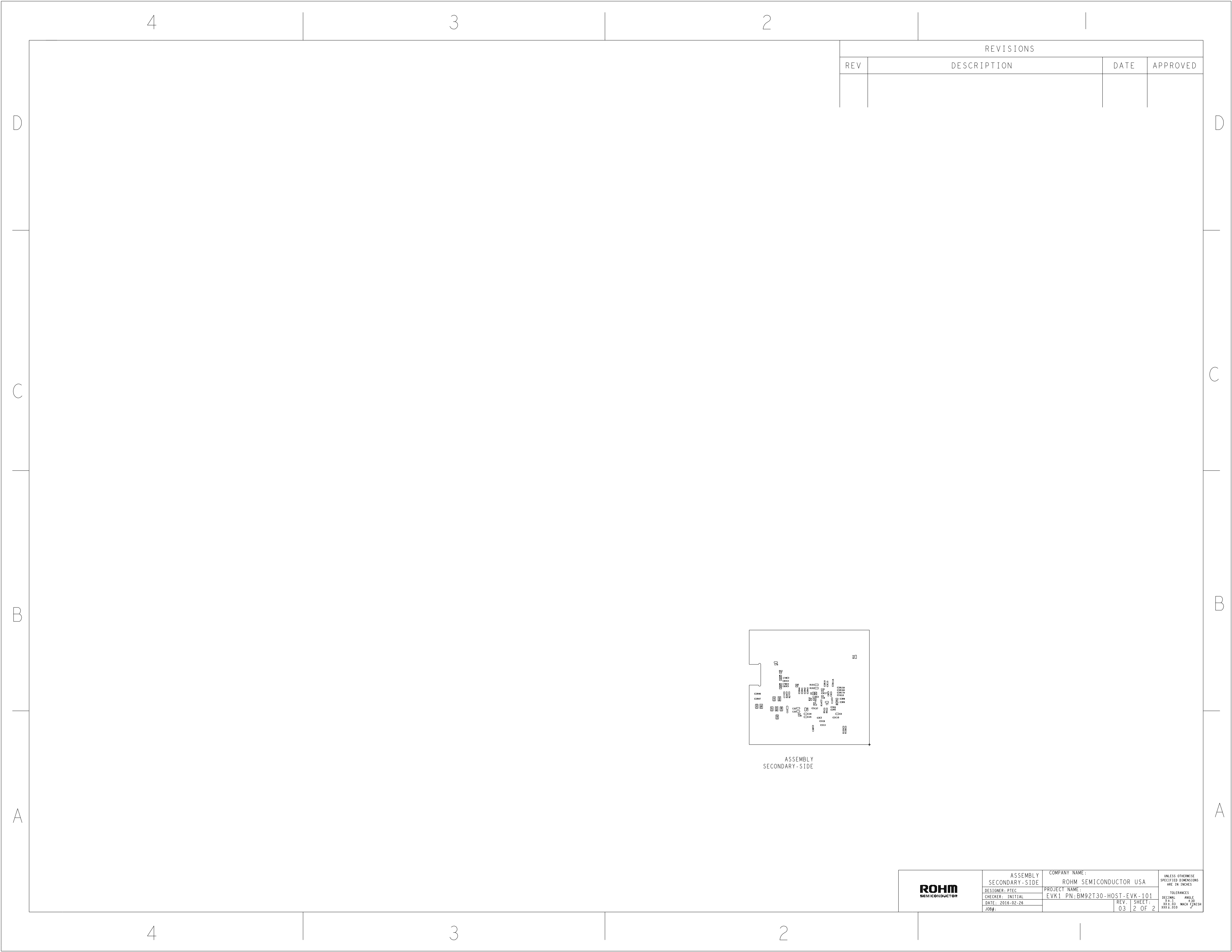


	JOB#:		PROJECT NUMBER:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMAL X ± .1 ANGLE ± 30 MACH FINISH XXX ± .010 ✓
	DATE: 2018-02-28		PROJECT NAME:		
	CHECKER: ROHM SEMICONDUCTOR		COMPANY NAME:		
	DESIGNER: PTEC		PROJECT NAME:		
	SECONDARY-SIDE PASTER MASK		ROHM SEMICONDUCTOR USA		
NUMBER		03	REV.	EVK1 PN: BM92T30-H02T-EVK-101	




REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ROHM SEMICONDUCTOR	ASSEMBLY TOP		COMPANY NAME: ROHM SEMICONDUCTOR USA		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS ANGLE XX ± .01 XX ± .03 MAC ± .015
	DESIGNER: PTEC		PROJECT NAME: EVK1 PN:BM92T30-HOST-EVK-101		
	CHECKER: INITIAL		ASSEMBLY NUMBER: NUMBER		
	DATE: 2016-02-26		REV. SHEET: 03 1 OF 1		
	JOB#:				



ASSEMBLY
SECONDARY - SIDE

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

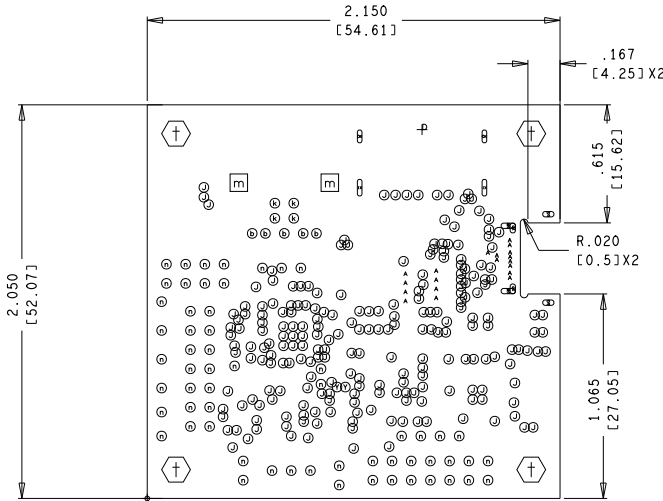
	ASSEMBLY SECONDARY - SIDE		COMPANY NAME : ROHM SEMICONDUCTOR USA		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	
	DESIGNER: PTEC		PROJECT NAME : EVK1 PN:BM92T30-HOST-EVK-101			
	CHECKER: INITIAL				TOLERANCES DECIMAL ANGLE XX ± .03 MAC ± .010	
	DATE: 2016-02-26					
	JOB#:		REV. 03 SHEET: 2 OF 2			

LAYER STACKING DETAIL

Ref. Layer	Layer #	Layer Type	Copper Weight (Oz)	Copper Thickness (Mils)	Material Type - Ply	Dielectric Thickness (Mils)	Finished Line (Mils)	Diff. Gap (Mils)	Required Impedance (Ohms)
Solder Mask				1.2					
Plating				1.2					
2	1	TOP	0.5	0.7			7	7	85
					Prepreg	4.4			
	2	GND	1	1.4					
					Core	47			
	3	PWR	1	1.4					
					Prepreg	4.4			
3	4	BOT	0.5	0.7			7	7	85
Plating				1.2					
Solder Mask				1.2					

Total Overall Thickness: 64.8 +/- 10%
Material Type FR4

DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
•	8.0	+0.0/-8.0	PLATED	19
◉	10.0	+3.0/-3.0	PLATED	225
◉	25.0	+3.0/-3.0	PLATED	2
◉	28.0	+3.0/-0.0	PLATED	5
◉	37.0	+3.0/-0.0	PLATED	4
◉	40.0	+3.0/-3.0	PLATED	59
⌈	91.0	+3.0/-3.0	PLATED	2
⊕	150.0	+3.0/-3.0	PLATED	4
⋈	56.0	+2.0/-2.0	NON-PLATED	1
⊗	51.181x27.559	+3.0/-3.0	PLATED	2
⊗	59.0x28.0	+3.0/-3.0	PLATED	2
⊗	67.0x24.0	+3.0/-3.0	PLATED	2
⊗	74.803x27.559	+3.0/-3.0	PLATED	2
⊗	87.0x24.0	+3.0/-3.0	PLATED	2



FAB NOTE

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

NOTES:

- Specifications.
 - Fabricate IAW IPC600, latest revision.
 - Producibility study - It is the responsdibility of the supplier to conduct a thorough review of the artwork and media for manufacturability in the supplier's process compliance to all applicable specifications. Customer must be advised in writing (in advance of manufacturing) of any changes, revisions,or corrections made or recommendations to ensure conformance to standards, and of any specifications that cannot be met.
 - This drawing is to be used in conjunction with the provided gerber and drill data when applicable.
 - All notes are "Unless Otherwise Specified."
- Material
 - FR4.
 - Color to be opaque.
- Soldermask

Solder mask both sides with (green color) liquid photoimageable soldermask, 003 max. thickness.
Soldermask over bare copper.
Soldermask is allowed in via holes.
- Drilling
 - All hole diameters are finished sizes.
 - All hole to be +/- .003 from true position unless otherwise specified.
 - All hole diameters to be +/- .003 unless otherwise specified.
 - An NC drill file has been supplied - see drill table.
- Finish
 - Plate thru with copper .0010 min to .002 max. thickness drill size dimension apply after plating.
 - Use gold immersion over nickel.
 - Finished boards shall not have nicks, scratches, voids, exposed copper, poor plating, all misdrilled holes.
- Silkscreen
 - Silkscreen using white non-conductive epoxy or equivalent (both sides).
 - No silkscreen allowed on exposed lands.
 - Silkscreen must be a minimum of 3mm away form fiducial marks.
 - Minimum clearance between silkscreen legend and vias, pads, or holes to be .005.
 - Silkscreen is allowed in via holes.
- Electrical Test
 - All boards shall be 100% electrically tested for opens/short at 10 volts. MIL-SPEC boards to be tested at 40 volts.
 - Apply test stamp in non-legend area on solder side of PCB.
 - Test is required on both sides of the board.
- Cleanliness
 - Boards shall be free of fiber glass dust or any other foreign material.
 - Finished boards must conform to 0.01 MG/IN max NaCl ionic contamination as measured by the omega meter 600SMD.
- Packaging

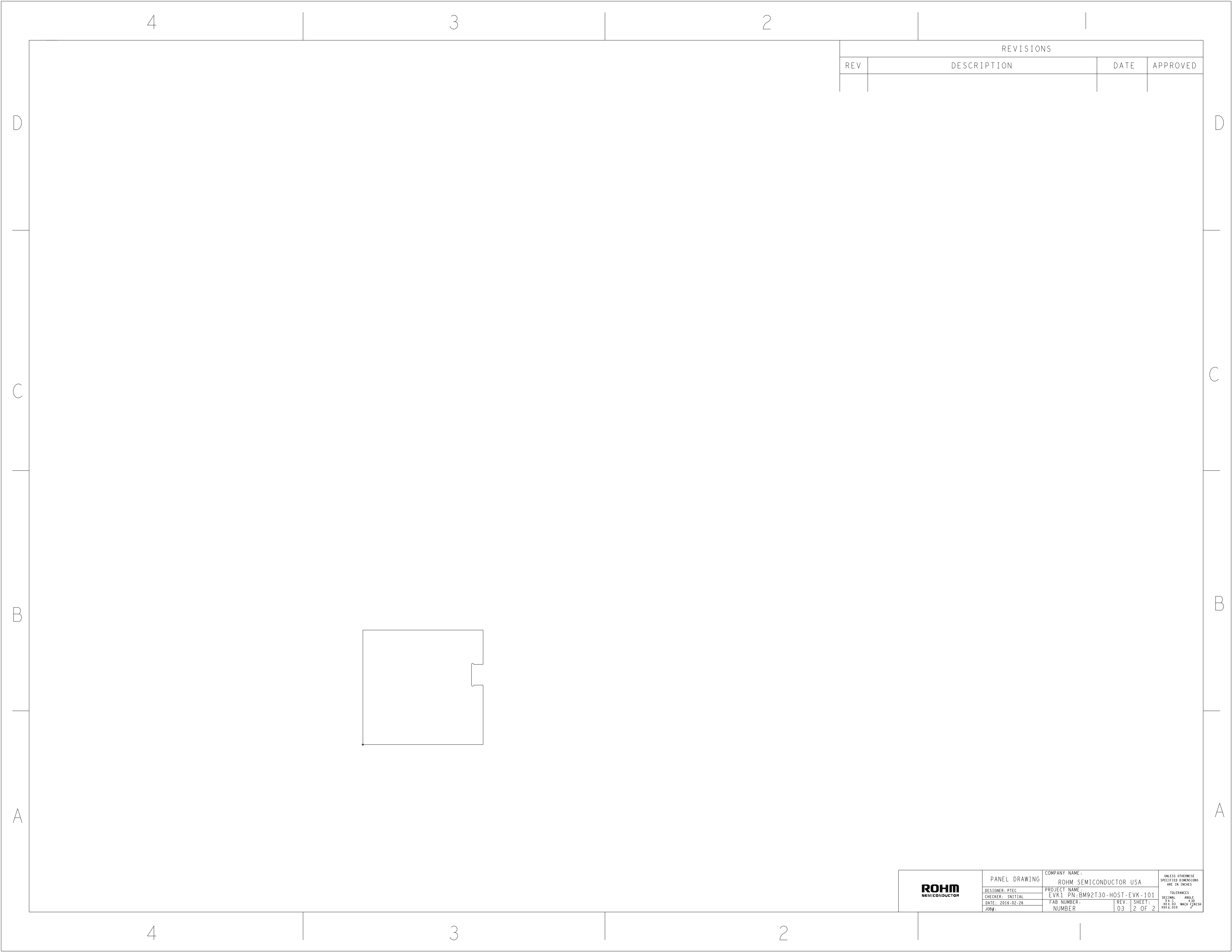
There shall be a max of 25 units per package, individually wrapped, and shipped in cardboard cratons with sufficient surrounding material to prevent shipping damage.
- Bow and Twist

Bow and twist to be .007 IN/IN or .090 max according to IPC-A-600D.
- Inspection
 - Automatic optical inspection of all layers required.
 - The impedance should be controlled by stackup layer.
- Inside corners should be rounded-off
- Changes to board geometries and apertures are not allowed unless they are approved by customer.
- Rounding is allowed on 90 degree corners with the size of standard routing bit.

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SEMICONDUCTOR

FAB DRAWING		COMPANY NAME:	
DESIGNER: PTEC		ROHM SEMICONDUCTOR USA	
CHECKER: INITIAL		PROJECT NAME: EVK1 PN:BM92T30-HOST-EVK-101	
DATE: 2016-02-26		FAB NUMBER:	REV. SHEET: 03 1 OF 2
JOB#:		NUMBER	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DIM. FIN. ANGLE
XX ±.01 XX ±.01 XX ±.01



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

	PANEL DRAWING	COMPANY NAME: ROHM SEMICONDUCTOR USA		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	
	DESIGNER: PTEC	PROJECT NAME: EVK1 PN:BM92T30-HOST-EVK-101			
	CHECKER: INITIAL	FAB NUMBER: NUMBER		TOLERANCES DECIMAL ANGLES X ± .1 X ± .03 MAC ± .015 XXX ± .010	
	DATE: 2016-02-26	REV: 03	SHEET: 2 OF 2		
	JOB#:				