REVISIONS LAYER STACKING DETAIL REV DESCRIPTION DATE APPROVED Finished Diff. Gap Dielectric Required Copper Material Layer Weight Thickness Thickness Line Impedance NOTES: Ref. Layer | Layer # (Mils) (Mils) Type - Ply (Öhms) (Mils) Туре (Oz)(Mils) 1. Specifications. Solder Mask 1.2 A. Fabricate IAW IPC600, latest revision. Plating 1.2 B. Producibility study - It is the respondsibility of the supplier to conduct a thorough review of the artwork and media for TOP 0.5 0.7 7 85 manufacturability in the supplier's process compliance to all applicable specifications. Customer must be advised in Prepreg 4.4 writing (in advance of manufacturing) of any changes, revisions, or GND 1.4 corrections made or recommendations to ensure conformance to 47 Core standards, and of any specifications that cannot be met. D. This drawing is to be used in conjunction with the provided gerber and drill data when applicable. PWR 1.4 3 Prepreg 4.4 E. All notes are "Unless Otherwise Specified." ВОТ 0.5 0.7 85 2. Material A. FR4. Plating 1.2 B. Color to be opaque. Solder Mask 1.2 3. Soldermask Solder mask both sides with (green color) liquid 64.8 +/- 10% Total Overal Thickness: DRILL CHART: TOP to BOTTOM photoimageable soldermask, 003 max. thickness. Material Type FR4 Soldermask over bare copper. ALL UNITS ARE IN MILS Soldermask is allowed in via holes. FIGURE TOLERANCE SIZE PLATED QTY 4. Drillina +0.0/-8.0 PLATED 8.0 19 A. All hole diameters are finished sizes. 10.0 PLATED 225 + 3 . 0 / - 3 . 0 B. All hole to be +/- .003 from true position unless otherwise specified. 25.0 + 3 . 0 / - 3 . 0 PLATED 2 C. All hole diameters to be +/- .003 unless otherwise specified. D. An NC drill file has been supplied - see drill table. PLATED 28.0 + 3 . 0 / - 0 . 0 5 5. Finish + 3 . 0 / - 0 . 0 PLATED 37.0 4 A. Plate thru with copper .0010 min to .002 max. thickness drill size 59 40.0 + 3 . 0 / - 3 . 0 PLATED dimension apply after plating. + 3 . 0 / - 3 . 0 91.0 PLATED 2 m B. Use gold immersion over nickel. C. Finished boards shall not have nicks, $\langle \dagger \rangle$ 150.0 + 3 . 0 / - 3 . 0 PLATED scratches, voids, exposed copper, poor plating, all misdrilled holes. + 2 . 0 / - 2 . 0 NON-PLATED 56.0 6. Silkscreen + 3 . 0 / - 3 . 0 51.181x27.559 PLATED A. Silkscreen using white non-conductive epoxy or equivalent (both sides). 59.0x28.0 + 3 . 0 / - 3 . 0 PLATED 2 B. No silkscreen allowed on exposed lands. 67.0x24.0 + 3 . 0 / - 3 . 0 PLATED C. Silkscreen must be a minimum of 3mm away form fiducial marks. 74.803x27.559 + 3 . 0 / - 3 . 0 PLATED D. Minimum clearance between silkscreen legend and vias, pads, or holes to be .005. 87.0x24.0 + 3 . 0 / - 3 . 0 PLATED E. Silkscreen is allowed in via holes. 7. Electrical Test A. All boards shall be 100% electrically tested for opens/short at 10 volts. MIL-SPEC boards to be tested at 40 volts. B. Apply test stamp in non-legend area on solder side of PCB. C. Test is required on both sides of the board. 8. Cleanliness A. Boards shall be free of fiber glass dust or any other foreign material. B. Finished boards must conform to 0.01 MG/IN max NAcL ionic contamination m 8 0000 00 6 as meaxured by the omega meter 600SMD. 9. Packaging There shall be a max of 25 units per package, individually wrapped, and shipped in cardboard cratons with sufficient surrounding material to prevend shipping damage. 10. Bow and Twist Bow and twist to be .007 IN/IN or .090 max according to IPC-A-600D. 000000 11. Inspection A. Automatic optical inspection of all layers required. B. The impedance should be controlled by stackup layer. 12. Inside corners should be rounded-off 13. Changes to board geometries and apertures are not allowed unless they are approved by customer. 14. Rounding is allowed on 90 degree corners with the size of standard routing bit. FAB NOTE FAB DRAWING ROHM SEMICONDUCTOR USA ROHM PROJECT NAME: EVK1 PN:BM92T30-HOST-EVK-101 TOLERANCES CHECKER: INITIAL
DATE: 2016-02-26 FAB NUMBER NUMBER 4

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