Automotive Body, Power Management LSI Series

12ch LED Driver IC

BD8377FV-M

Rev.A

●Description

The BD8377FV-M is a serial-in parallel-out controlled LED driver with 35V output voltage rating.
With the input of 3-line serial data, it turns the 12ch open drain output on/off.
Due to its compact size, it is optimal for small space.

●Features

1) Open Drain Output
2) 3-line Serial Control + Enable Signal
3) Cascade Connection Compatible
4) SSOP-B20
5) Internal 12ch Power Transistor

●Applications

These ICs can be used with car and consumer electronics.

●Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Value	Unit
Power Supply Voltage	VCC	7	V
Output Voltage（Pin No : 3～8, 13～18）	VDmax	35	V
Input Voltage（Pin No : 2, 9, 10, 12, 19）	VIN	-0.3～VCC	V
Power Dissipation	Pd	940*	mW
Operating Temperature Range	Topr	-40～+105	℃
Storage Temperature Range	Tstg	-55～+150	℃
Drive Current (DC)	IomaxD	50	mA
Drive Current（Pulse）	IomaxP	150**	mA
Junction Temperature	Tjmax	150	℃

* Pd decreased at 7.5mW/℃ for temperatures above Ta=25℃, mounted on 70×70×1.6mm Glass-epoxy PCB.
** Do not however exceed Pd. Time to impress≦200msec

●Operational Conditions (Ta=-40~105℃)

Item	Symbol	Standard Value			Unit
		Min	Typ	Max	
Power Supply Voltage	VCC	3.0	5.0	5.5	V

●Electrical Characteristics (Unless specified, Ta=-40~105℃ Vcc=3.0~5.5V)

Item	Symbol	Standard Value			Unit	Conditions
		Min	Typ	Max		
【Output D0～D11】(Pin No : 3～8, 13～18)						
ON Resistor 1	RON1	-	6	12	Ω	I_D=20mA, VCC=4.5~5.5V
ON Resistor 2	RON2	-	9	18	Ω	I_D=20mA, VCC=3.0~4.5V
Output leakage current 1	IDL1	-	-	5	uA	V_D=34V
Output leakage current 2	IDL2	-	-	0.5	uA	V_D=16V,Ta=25℃,
【Logic input】(Pin No : 2, 9, 10, 12, 19)						
Upper limit threshold voltage1	VTH1	VCC x 0.5	-	-	V	VCC=4.5~5.5V
Upper limit threshold voltage2	VTH2	VCC x 0.6	-	-	V	VCC=3.0~4.5V
Bottom limit threshold voltage1	VTL1	-	-	VCC x 0.2	V	VCC=4.5~5.5V
Bottom limit threshold voltage2	VTL2	-	-	VCC x 0.3	V	VCC=3.0~4.5V
OEN_B terminal Hysteresis width	VHYS	0.15	0.30	0.5	V	VCC=5V
Serial clock frequency	FCLK	-	-	1.25	MHz	
Input leakage Current L	IINLL	-5	-	-	uA	VIN=0V
Input leakage Current H	IINLH	-	-	5	uA	VIN=5V
【WHOLE】						
Circuit Current	ICC	-	0.3	1	mA	Serial Data Input, VCC=5V,CLK=500KHz, SEROUT=OPEN
Static Current	ISTN	-	-	50	uA	RST_B=OPEN, SEROUT=OPEN
【SER OUT】(Pin No. : 11)						
Output Voltage High 1	VOH1	4.6	4.8	-	V	VCC=5V, ISO=-4mA
Output voltage Low 1	VOL1	-	0.2	0.4	V	VCC=5V, ISO=4mA
Output Voltage High 2	VOH2	2.7	3.0	-	V	VCC=3.3V, ISO=-4mA
Output voltage Low 2	VOL2	-	0.3	0.6	V	VCC=3.3V, ISO=4mA

* This product is not designed for protection against radioactive rays.

●Electrical Characteristic Diagrams (Unless otherwise specified Ta=25℃)

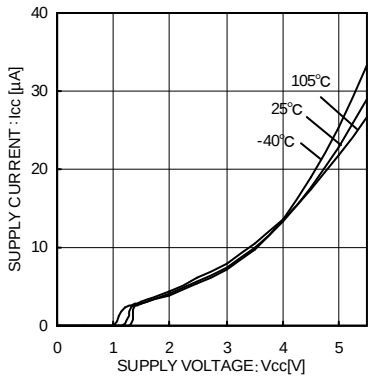


Fig.1 Circuit current
（VCC characteristic）

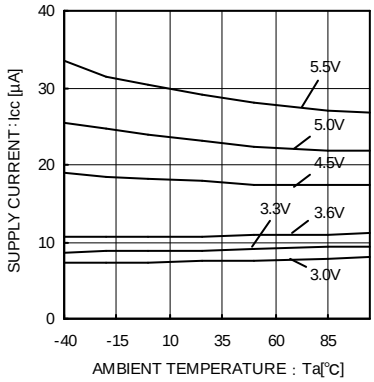


Fig.2 Circuit current
（Temperature characteristic）

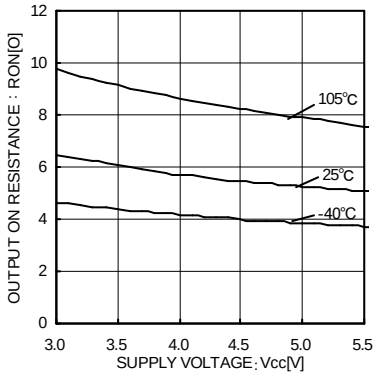


Fig.3 Output ON resistance
（VCC characteristic @ ID=20mA）

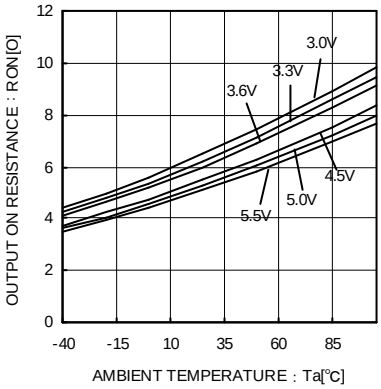


Fig.4 Output ON resistance
（Temperature characteristic @ ID=20mA）

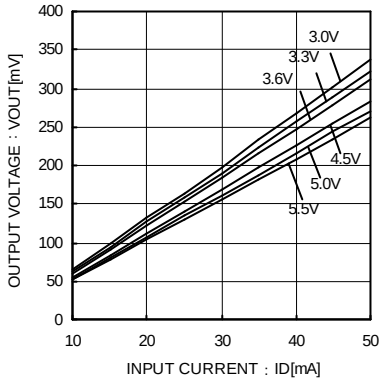


Fig.5 Output ON resistance
（ID characteristic）

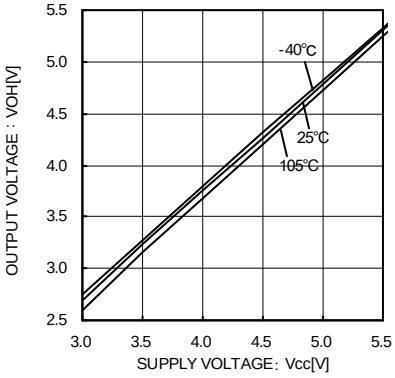


Fig.6 SEROUT high side voltage
（VCC characteristic @ ISO=-4mA）

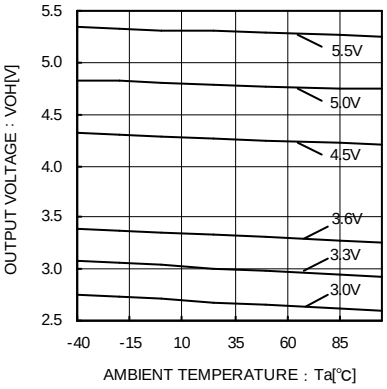


Fig.7 SEROUT high side voltage
（Temperature characteristic @ ISO=-4mA）

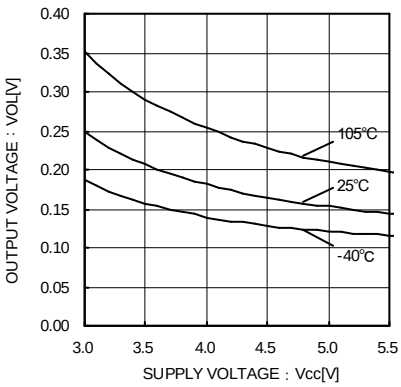


Fig.8 SEROUT low side voltage
（VCC characteristic @ ISO=4mA）

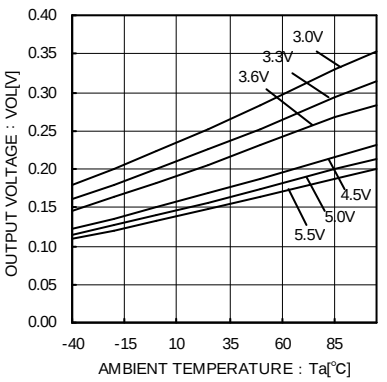


Fig.9 SEROUT low side voltage
（Temp characteristic @ ISO=4mA）

●Block Diagram

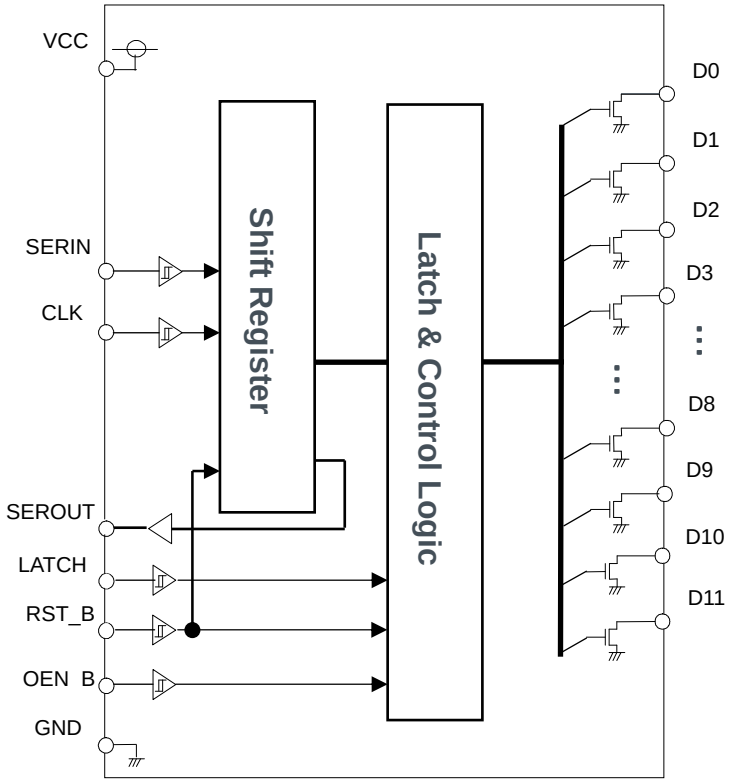


Fig.10

●Pin Setup Diagram

BD8377FV-M（SSOPB20）

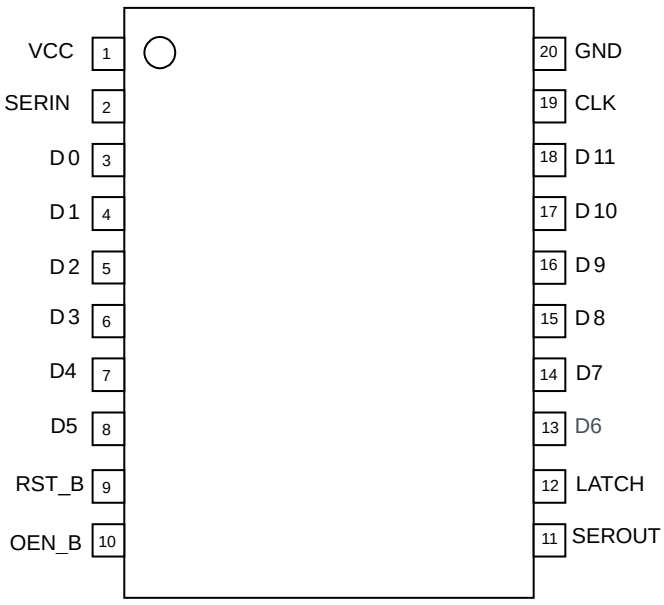


Fig.11

●Terminal Number・Terminal Name

Pin Number	Terminal Name	Function
1	VCC	Power supply voltage input
2	SERIN	Serial data input
3	D0	Drain output 0
4	D1	Drain output 1
5	D2	Drain output 2
6	D3	Drain output 3
7	D4	Drain output 4
8	D5	Drain output 5
9	RST_B	Reset return input (L:FF data 0)
10	OEN_B	Output enable (H: Output OFF)
11	SEROUT	Serial data output
12	LATCH	Latch signal input (H: Data latch)
13	D6	Drain output 6
14	D7	Drain output 7
15	D8	Drain output 8
16	D9	Drain output 9
17	D10	Drain output 10
18	D11	Drain output 11
19	CLK	Clock input
20	GND	GND

●Block Operation

1）Serial I/F

This I/F is a 3-line serial (LATCH, CLK, SERIN) style.

12-bit output ON/OFF can be set-up. This is composed of 12-bit shift registers and latch registers.

2）Driver

It is a 12-bit open drain output.

●Application Circuit

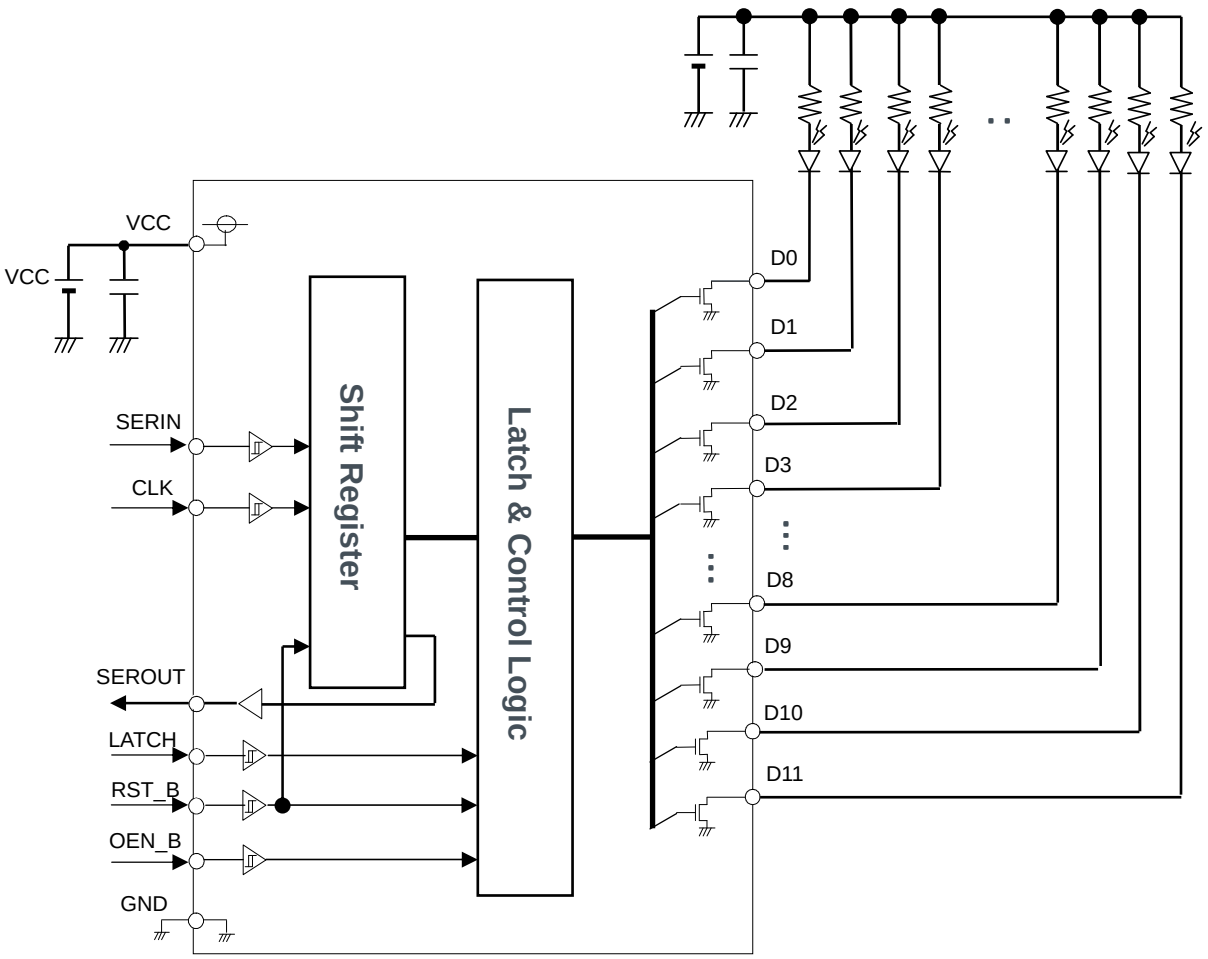


Fig.12

●Serial Communication

The serial I/F is composed of a shift register which changes the CLK and SERIN serial signals to parallel signals, and a register to store those signals with a LATCH signal. The registers are reset by applying a voltage below VTL voltage to the RST_B terminal, and D11~D0 become open. To prevent erroneous LED lighting, please apply voltage below VTL voltage to RST_B during start-up.

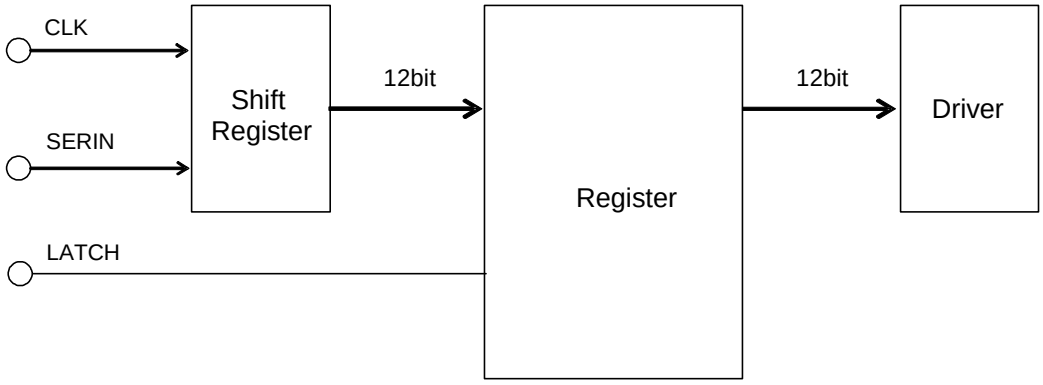


Fig.13

1）Serial Communication Timing

The 12-bit serial data input from SERIN is taken into the shift register by the rising edge of the CLK signal, and is recorded in the register by the rising edge of the LATCH signal. The recorded data is valid until the next rising edge of the LATCH signal.

2）Serial Communication Data

The serial data input configuration of SERIN terminal is shown below:

First →　　→Last

d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0
Data											

Terminal Name	Output Status	Data											
		d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0
D11	ON	1	*	*	*	*	*	*	*	*	*	*	*
	OFF	0	*	*	*	*	*	*	*	*	*	*	*
D10	ON	*	1	*	*	*	*	*	*	*	*	*	*
	OFF	*	0	*	*	*	*	*	*	*	*	*	*
D9	ON	*	*	1	*	*	*	*	*	*	*	*	*
	OFF	*	*	0	*	*	*	*	*	*	*	*	*
D8	ON	*	*	*	1	*	*	*	*	*	*	*	*
	OFF	*	*	*	0	*	*	*	*	*	*	*	*
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
D3	ON	*	*	*	*	*	*	*	*	1	*	*	*
	OFF	*	*	*	*	*	*	*	*	0	*	*	*
D2	ON	*	*	*	*	*	*	*	*	*	1	*	*
	OFF	*	*	*	*	*	*	*	*	*	0	*	*
D1	ON	*	*	*	*	*	*	*	*	*	*	1	*
	OFF	*	*	*	*	*	*	*	*	*	*	0	*
D0	ON	*	*	*	*	*	*	*	*	*	*	*	1
	OFF	*	*	*	*	*	*	*	*	*	*	*	0

* represents “Don’t care”.

3）Enable Signal

By applying voltage at least VTH voltage or more to the OEN_B terminal, D11~D0 become open forcibly.
D11～D0 become PWM operation by having the PWM signal to the OEN_B terminal.

4）SEROUT

A cascade connection can be made (connecting at least 2 or more IC's in serial).
Serial signal input from SERIN is transferred into receiver IC by the falling edge of the CLK signal.
Since this functionality gives enough margins for the setup time prior to the rising edge of the CLK signal on the receiver IC (using the exact same CLK signal of sender IC), the application reliability can be improved as cascade connection functionality.

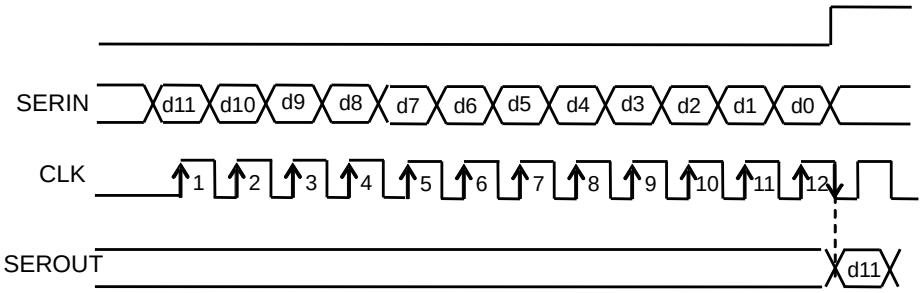


Fig.14

●Cascade Connection

By using (at least) 2 ICs, each IC's D11~D0, at (at least) 24ch, can be controlled by the 24-bit SERIN signal. The serial data input to the sender IC can be transferred to the receiver IC by inputting 12CLK to the CLK terminal.

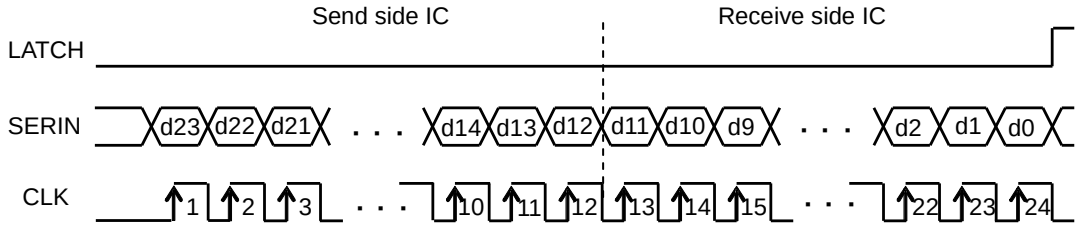


Fig.15

●INPUT SIGNAL'S TIMING CHART

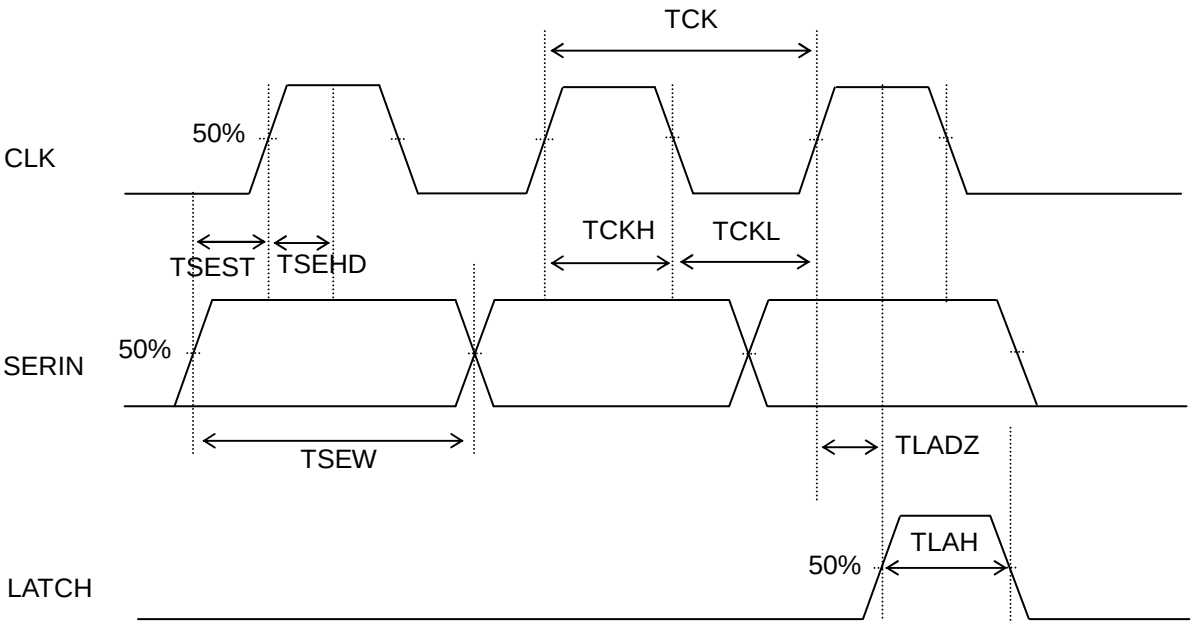


Fig.16

●INPUT SIGNAL'S TIMING RULE（Ta=-40～105℃ Vcc=4.5～5.5V）

Parameter	Symbol	Min	Unit
CLK period	TCK	800	ns
CLK high pulse width	TCKH	380	ns
CLK low pulse width	TCKL	380	ns
SERIN high and low pulse width	TSEW	780	ns
SERIN setup time prior to CLK rise	TSEST	150	ns
SERIN hold time after CLK rise	TSEHD	150	ns
LATCH high pulse time	TLAH	380	ns
Last CLK rise to LATCH rise	TLADZ	200	ns

●OUTPUT SIGNAL'S DELAY CHART

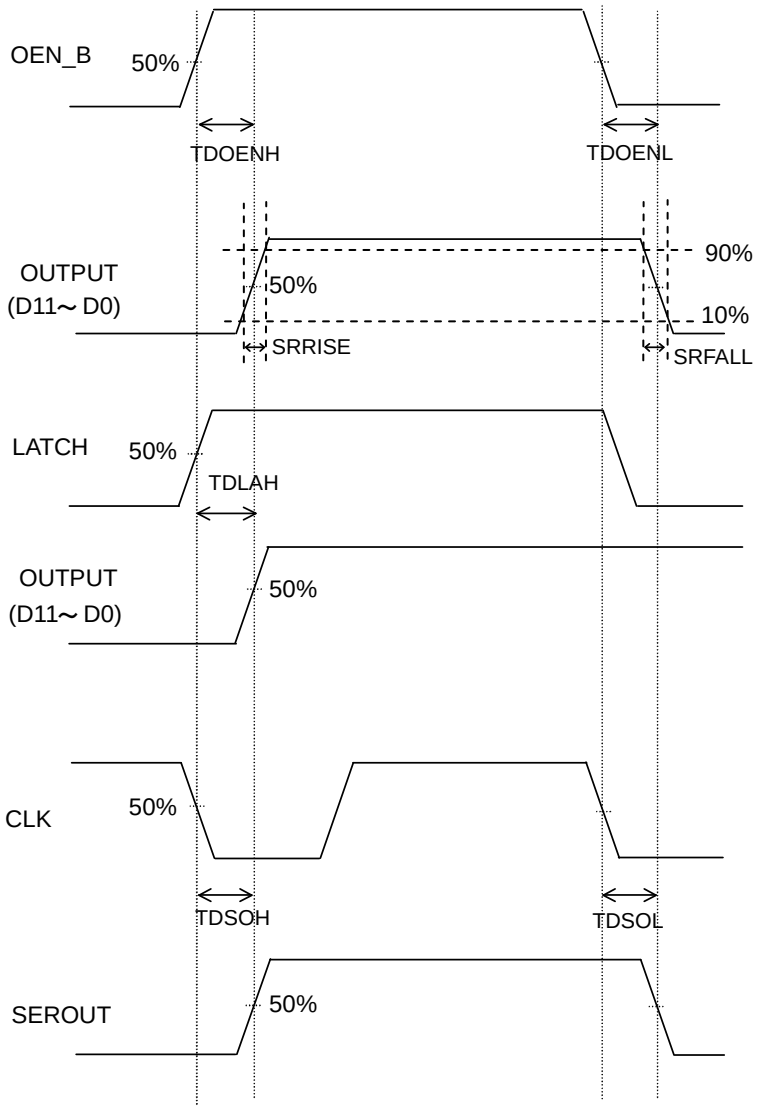


Fig.17

●OUTPUT SIGNAL'S DELAY TIME（Ta=-40～105℃ Vcc=4.5～5.5V）

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
OEN_B Switching Time(L→H)	TDOENH	-	-	3000	ns	
OEN_B Switching Time(H→L)	TDOENL	-	-	1000	ns	
LATCH Switching Delay Time	TDLAH	-	-	3000	ns	
SEROUT Propagation Delay Time(L→H)	TDSOH	-	-	350	ns	
SEROUT Propagation Delay Time (H→L)	TDSOL	-	-	350	ns	
Rising Slew Rate	SRRISE	10	20	40	V/us	Ta=25℃,VCC=5V, RL=500ohm,VBAT=10V
Falling Slew Rate	SRFALL	10	20	40	V/us	Ta=25℃,VCC=5V, RL=500ohm,VBAT=10V

●INPUT/OUTPUT EQUIVALENT CIRCUIT（PIN NAME）

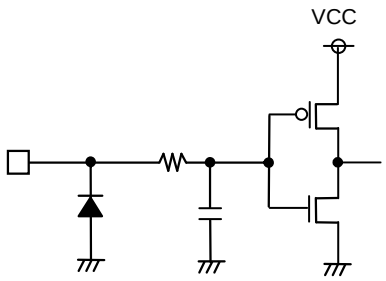
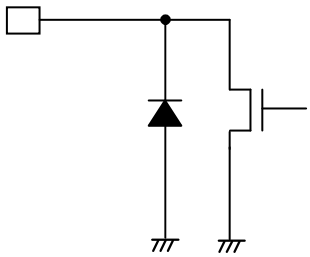
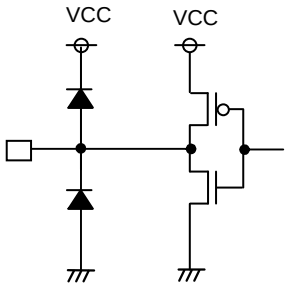
2PIN (SERIN) 9PIN (RST_B) 10PIN (OEN_B) 12PIN (LATCH) 19PIN (CLK)	18PIN (D11), 17PIN (D10), 16PIN (D9), 15PIN (D8), 14PIN (D7), 13PIN (D6), 8PIN (D5), 7PIN (D4) , 6PIN (D3), 5PIN (D2), 4PIN (D1), 3PIN (D0)	11PIN (SEROUT)
		

Fig.18

●Operation Notes

(1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered.

A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

(2) Reverse connection of a power supply connector

If the connector of power is wrong connected, it may result in IC breakage. In order to prevent the breakage from the wrong connection, the diode should be connected between external power and the power terminal of IC as protection solution.

(3) GND potential

Ensure a minimum GND pin potential in all operating conditions.

(4) Setting of heat

Use a setting of heat that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

(5) Pin short and mistake fitting

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage.

(6) Actions in strong magnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

(7) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress.

Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process

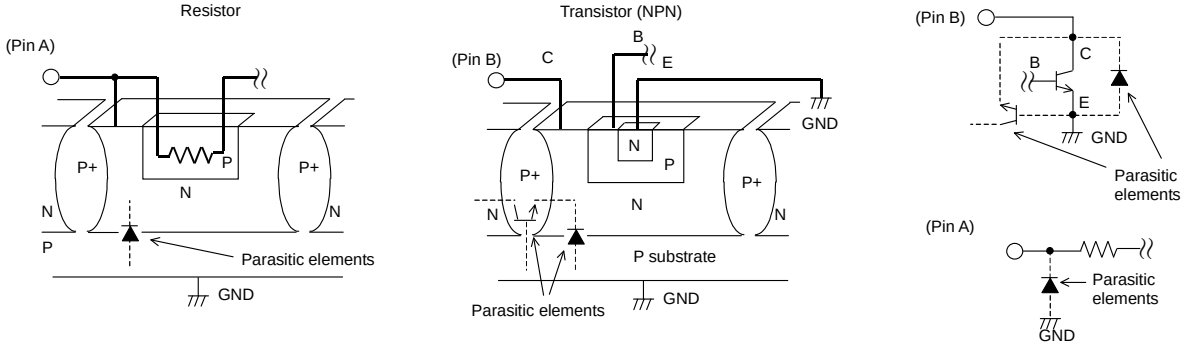
(8) IC terminal input

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.

For example, a resistor and transistor are connected to pins. (See the chart below.)

- ○The P/N junction functions as a parasitic diode when GND > (Pin A) for the resistor or GND > (Pin B) for the transistor (NPN).
- ○Similarly, when GND > (Pin B) for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (PCB) voltage to input pins.



(9) Ground wiring patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.

●**Ordering part number**

B	D	8	3	7	7	F	V	-	M	E	2

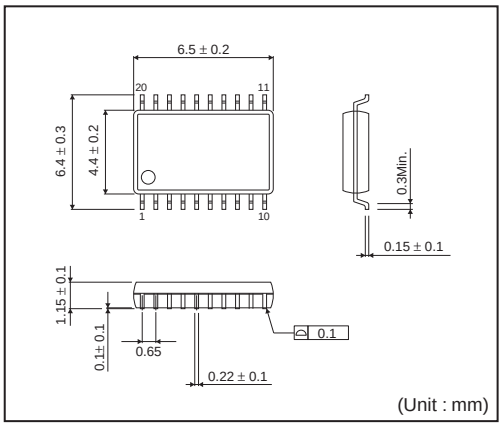
Part No. (BD)

Part No. (8377)

Package
FV: SSOPB20

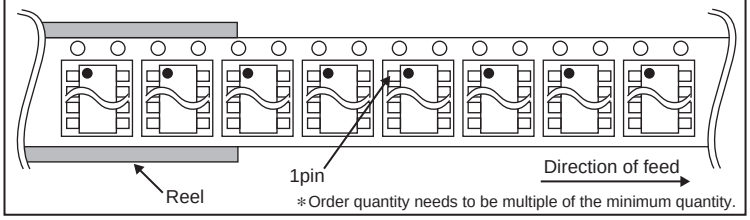
Packaging and forming specification
ME2: Embossed tape and reel

SSOP-B20



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.