INDIAN INSTITUTE OF ENGINEERING SCIENCE AND TECHNOLOGY, SHIBPUR
4TH SEMESTER (CS) FINAL EXAMINATION, April 2019
Computer Architecture and Organization - I (CS 402)

FULL MARKS: 70 TIME: 3 Hrs

1. Answer any ten questions with the necessary explanation. 2x10

(A) How many input-output data lines and address lines are needed for each of the following memories?

(i) 8Kx32 (ii) 256Kx64 (iii) 32Mx32 (iv) 4Gx8

(B) Match the followings (left hand side with right hand side) in the context of memory hierarchy from top to bottom

| | |
|---|---|
| (i) Size | (1) Increases |
| (ii) Cost/bit | (2) Decreases |
| (iii) Access time | (3) No change |
| (iv)Frequency of access | |

Choose the correct option: (a) (i)1(ii)1(iii)2(iv)2, (b) (i)2(ii)1(iii)2(iv)1, (c) (i)1(ii)2(iii)1(iv)2, (d) (i)2(ii)2(iii)1(iv)1

(C) Relative mode of addressing is most relevant for writing (i) Position independent code (ii) Sharable code (iii) Interrupt handler (iv)None

(D) Match the followings (left hand side with right hand side) in the context of RAID organization.

| RAID levels | Number of disks |
|---|---|
| (i) RAID 0 | (1) N+1 |
| (ii) RAID 1 | (2) N+2 |
| (iii) RAID 5 | (3) N |
| (iv) RAID 6 | (4) 2N |

(E) Match the followings (left hand side with right hand side) in the context of control unit design.

| | |
|---|---|
| (i) Horizontal microprogramming | (1) Fastest |
| (ii) Hardwired control unit design | (2) Maximum parallelism |
| (iii) Vertical microprogramming | (3) Encoded control signals |

(F) In set associative mapping if set size is one then it is (i) 1 way set associative (ii) Direct mapping (iii) Both

(G) IO devices can't be connected directly to the system because of (i) Speed mismatch (ii) Different data format (iii) Both

(H) Daisy chain is for

(i) Connecting number of devices to a computer

(ii) Connecting number of controllers to a device

(iii) Interconnecting number of devices to number of controllers

(I) If one instruction is executed in 4 nsec then what is the throughput of the system?

(J) The number of instructions which may possibly be executed by a computer depends upon the size of (i) Opcode (ii) PC (iii) MAR (iv) Word

(K) The address of the location of the operand is given explicitly as a part of the instruction in (i) Absolute mode (ii) Immediate mode (iii) Indirect mode (iv)Index mode

(L) The performance of two computers A and B are 1000 MIPS and 2000 MIPS respectively. Two programs of length 250 and 500 instructions are executed in A and B respectively. Which one will complete the execution first and why?

2. Answer any ten questions with the necessary explanation. 3x10

(A) The microinstruction stored in the control memory of a processor has a width of 20 bits. Each microinstruction is divided into 2 fields: a control field of size 9 bits and next address field of size X bits. Total number of micro operations is 46 and degree of parallelism is 2. Find the size of each control field, value of X and the size of control memory.

(B) What is the maximum speed up factor of n stage pipeline and why? Why it is not possible to achieve maximum speed up?

(C) What is the decimal value of the following floating point number?
0 10000011 00101000000000000000000
Why normalization is used in floating point number system?
(D) How many memory reference is required by a CPU to execute immediate address instruction and why?
(E) Consider a computer having 12 bit memory cell. How many bytes of memory can be accessed using 12 bit address? If a single memory cell is used to store a single character how many different characters could be represented by a cell?
(F) How many characters per second (7 bits+parity) can be transmitted over 2400 bps line in asynchronous mode having one start bit and one stop bit?
(G) If a disk rotates at 6000 rpm and track on the disk has 1024 sectors, what is the data transfer rate if the sector size is 1024 bits?
(H) How many 32Kx8 RAM chips are needed to provide a memory capacity of 1M bytes? How many address lines are needed? How many lines must be decoded for the chip select inputs? Specify the size of the decoder.
(I) A computer has a cache with access time 10 ns, a hit ratio of 80% and average memory access time is 24 ns. Then what is the access time for physical memory?
(J) What do you mean by conflict miss, capacity miss and compulsory miss?
(K) How much time a two stage pipeline takes to complete the execution of the following loop?
for I=1 to 100 do A[I]=B[I]*C[I]+D[I]
First stage of the pipeline is for multiplication (10 ns) and the second stage of the pipeline is for addition (10 ns). How the execution time of the above loop is affected in presence of latch (2 ns) in the pipeline?
(L) Consider a machine with a byte addressable main memory of $2^{16}$ bytes and block size of 8 bytes. Assume that a direct memory cache consists of 32 blocks is used with this machine. How 16 bit memory address is divided into tag, block number and byte number? How many total bytes of memory can be stored in the cache?

3. Answer any four questions.
(A) Derive an expression to show the relation between speed up, efficiency and throughput of a k-stage pipeline. What is the maximum possible value of efficiency of this pipeline? What are the basic differences between asynchronous and synchronous model of linear pipeline processor? [2+1+2]
(B) What are the drawbacks of programmed IO? How the interrupt request and DMA request eliminate these drawbacks? [2+1.5+1.5]
(C) Discuss the followings in the context of memory.
(i) Access time (ii) Access mode (iii) Relation between access time and access mode [1.5+1.5+2]
(D) Show the advantage of using carry save adder in the multiplier circuit with suitable example. [5]
(E) Compare the performance of direct mapping, fully associative mapping, set associative mapping in the context of hardware requirement. [5]
(F) What do you mean by transceiver? What are the advantages of using transceiver in the bus line? [2+3]