Lecture 25: April 13, 2021
Computer Architecture and Organization-I
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0.3.1 DMA transfer steps

Data counter (DC) of Figure 7 contains number of words to be transferred.

IO addr register (IOAR) contains base address of MM considered for data transfer.

Input output data register (IODR) temporarily stores data that is to be transferred.

Following steps realize a DMA data transfer from an input device to MM.

Step 1. CPU initializes the DC and IOAR

Step 2. DMAC checks status of Input device. If device is ready to transmit data, DMAC activates DMA request (DMAR).

Step 3. As soon as CPU senses DMAR, CPU waits for next DMA breakpoint. It then relinquishes control of buses and activates DMA acknowledge (DMAack).

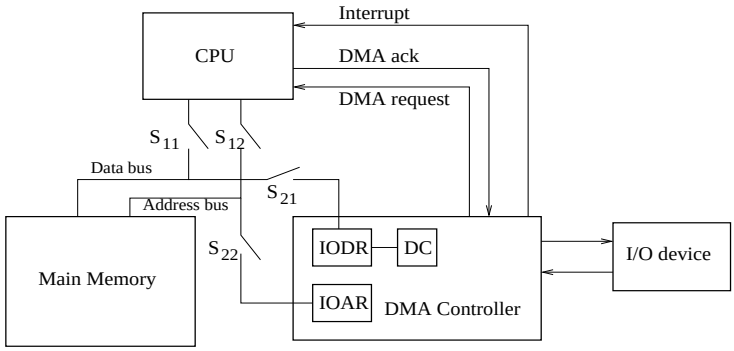
Step 4. Upon receiving DMAack, DMAC transfers data directly to MM.

Step 5. After a word is transferred, IOAR and DC are updated.

$$\text{IOAR} \leftarrow \text{IOAR} + 1$$
$$\text{DC} \leftarrow \text{DC} - 1$$
If DC> 0, then go to step 2

Step 6. If DC=0, then DMAC relinquishes control of system bus, and sends an interrupt to signal end of data transfer.

DMA data transfer from main memory to output device follows similar process.



Two types of DMA data transfer techniques are used in microprocessors:

1. Microprocessor halt DMA. It either implements

   a. Block transfer or
   b. Cycle stealing

   while stopping the processor.

2. Interleaved DMA - without stopping the processor.

   Interleaved DMA: each data transfer includes one byte per instruction cycle.

   Example: when processor is decoding instruction or performing ALU operations, DMAC can transfer a byte.

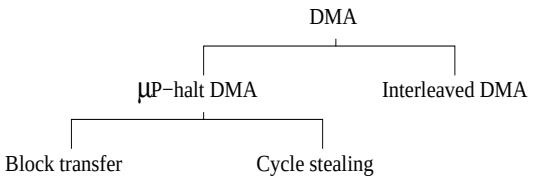


Figure 9: DMA classification

0.3.2 Bulk DMA

CPU is suspended for entire duration for extremely fast I/O device.

It is needed by secondary memory devices where data transfer cannot be stopped.

With block DMA, maximum IO data transmission rates can be achieved.

It may require the CPU to remain inactive for comparatively long periods.

0.3.3 Cycle stealing

Bus cycles are stolen only when CPU is not using system bus.

CPU is operated by an external clock - this is accomplished by not providing clock signal to CPU. An INHIBIT signal is used for this purpose.

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