Indian Institute of Engineering Science and Technology, Shibpur

BTech (CST) 4th Semester Mid Semester Examination, March 2022

Computer Architecture and Organization I (CS-2202)

Full marks: 30 Time: 45 Minutes

Answer all questions

1. Consider a hypothetical 32-bit microprocessor having 32-bit instructions, composed of two fields: the first byte contains opcode and the remainder bytes are for single operand address. 10

a) What is the maximum directly addressable memory capacity?
b) How many bits are needed for the program counter (PC)?
c) Define the size of data register (DR), address register (AR), and instruction register (IR)?
d) Show how 16M X 8 SRAM chips can be utilized to build a 16M X 16 memory unit.

2a) The JMP X (unconditional branch) and JMPZ X (branch if accumulator content is zero), the two control instructions, are included in a CPU instruction set. Propose a logic circuit that implements these two. 4

b) Write microprograms for the single-address instructions LOAD X, STORE X, AND X and CLEAR (clear AC). 4

c) Show a logic design with CSAs that performs high speed addition of six 32-bit numbers. 4

3. Describe in brief the opcode extension scheme with example. 8