

Diagram illustrating the bit fields for the **MODE** and **RESET** registers:

- The **MODE** register (bits 7:0) is shown as a row of 8 boxes, with bit 0 on the right and bit 7 on the left. The value **0x00** is indicated to the right.
- The **RESET** register (bits 7:0) is shown as a row of 8 boxes, with bit 0 on the right and bit 7 on the left.
- Connections:
 - Bit 0 of **MODE** is connected to Bit 0 of **RESET**.
 - Bit 1 of **MODE** is connected to Bit 1 of **RESET**.
 - Bit 2 of **MODE** is connected to Bit 2 of **RESET**.
 - Bit 3 of **MODE** is connected to Bit 3 of **RESET**.
 - Bit 4 of **MODE** is connected to Bit 4 of **RESET**.
 - Bit 5 of **MODE** is connected to Bit 5 of **RESET**.
 - Bit 6 of **MODE** is connected to Bit 6 of **RESET**.
 - Bit 7 of **MODE** is connected to Bit 7 of **RESET**.

7 6 5 4 3 2 1 0

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | X | X | X | 0 | 1 | 0 | 0 |
|---|---|---|---|---|---|---|---|

0x10

MODE[3:0]

RESET[7]

7 6 5 4 3 2 1 0

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | x | x | x | 0 | 0 | 1 | 0 |
|---|---|---|---|---|---|---|---|

0x01

MODE[3:0]

RESET[7]

7 6 5 4 3 2 1 0

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| - | - | - | 0 | 0 | 0 | 0 | S |
|---|---|---|---|---|---|---|---|

0x02

SERROR[0]

ERROR[2]

CUR_STATUS[4:3]

Diagram illustrating the bit fields of the `CORE_ERR[0]` register:

| Bit | Field |
|-----|--------------|
| 7 | IORESET [6] |
| 6 | |
| 5 | CORE_ERR [0] |
| 4 | |
| 3 | CORE_ERR [0] |
| 2 | |
| 1 | CORE_ERR [0] |
| 0 | |

The register value is shown as `0x03`.