FSM

1. Lab Description

Part A: Moore State Machine

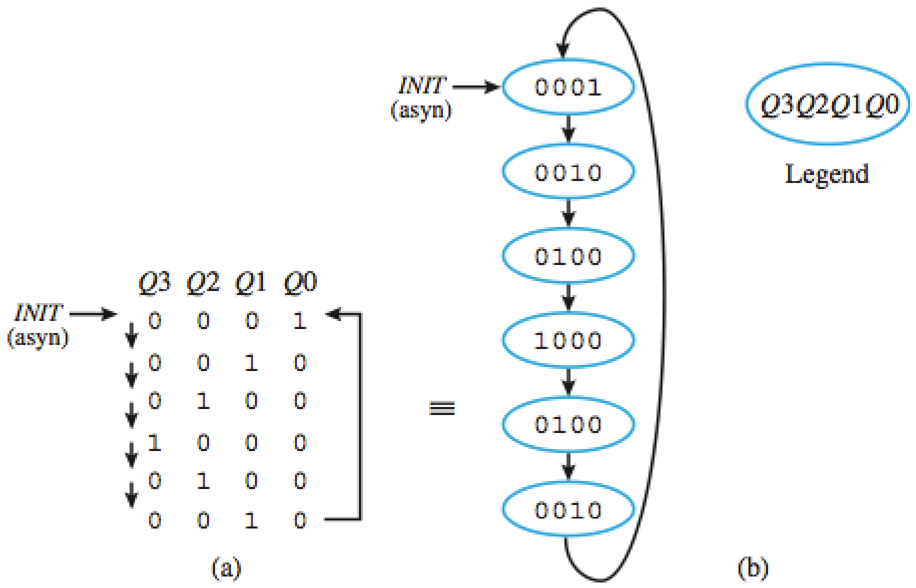


Figure 1 Robot eyes a) state table b) state diagram

Write a Verilog code creating the state machine shown in Figure 1 b). Use clk, reset as input, whereas W [3:0] as output. Write an appropriate testbench code to test your HDL code.

Part B: Mealy State Machine

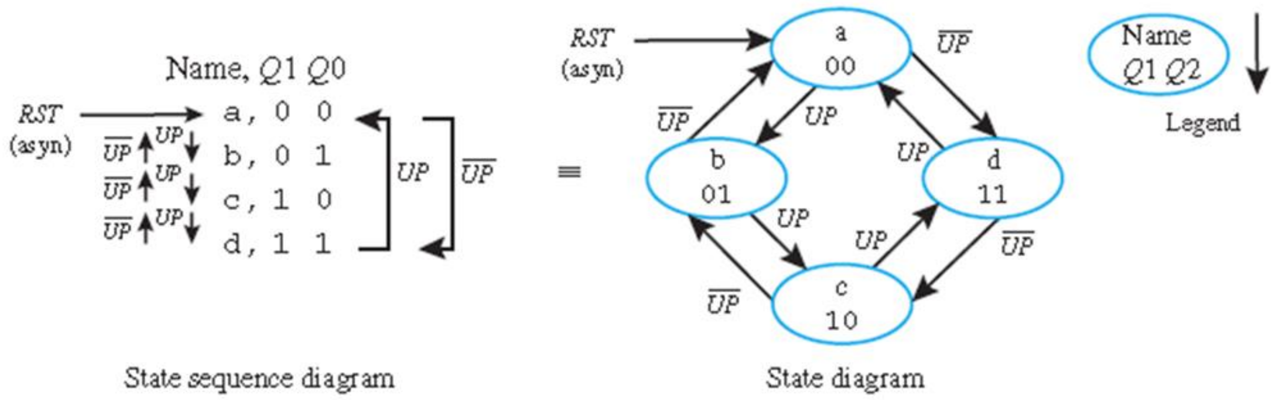


Figure 2. Binary Counter

Write a Verilog code creating the state machine shown in Figure 2. Use clk, reset, up as input, whereas Q [1:0] as output. Write an appropriate testbench code to test your HDL code.

Submit your Verilog and testbench file

Part A: Moore FSM

```
module FSM_Moore(Clk,Reset,W);
   input Clk,Reset;
   output [3:0] W;

   reg [4:0] state_reg, state_next;

   parameter S0 = 5'b00001;
   parameter S1 = 5'b00010;
   parameter S2 = 5'b00100;
   parameter S3 = 5'b01000;
   parameter S4 = 5'b10100;
   parameter S5 = 5'b10010;

   //state register
   always @ (posedge Clk, posedge Reset)
   if (Reset) state_reg <= S0;
```

```
            else
            state_reg <= state_next;

   //Combinational Logic
   always @ (*)
   case (state_reg)
   S0: state_next = S1;
   S1: state_next = S2;
   S2: state_next = S3;
   S3: state_next = S4;
   S4: state_next = S5;
   S5: state_next = S0;
   default: state_next = S0;
   endcase

   //Output Logic
   assign W = state_reg[3:0];

endmodule
```

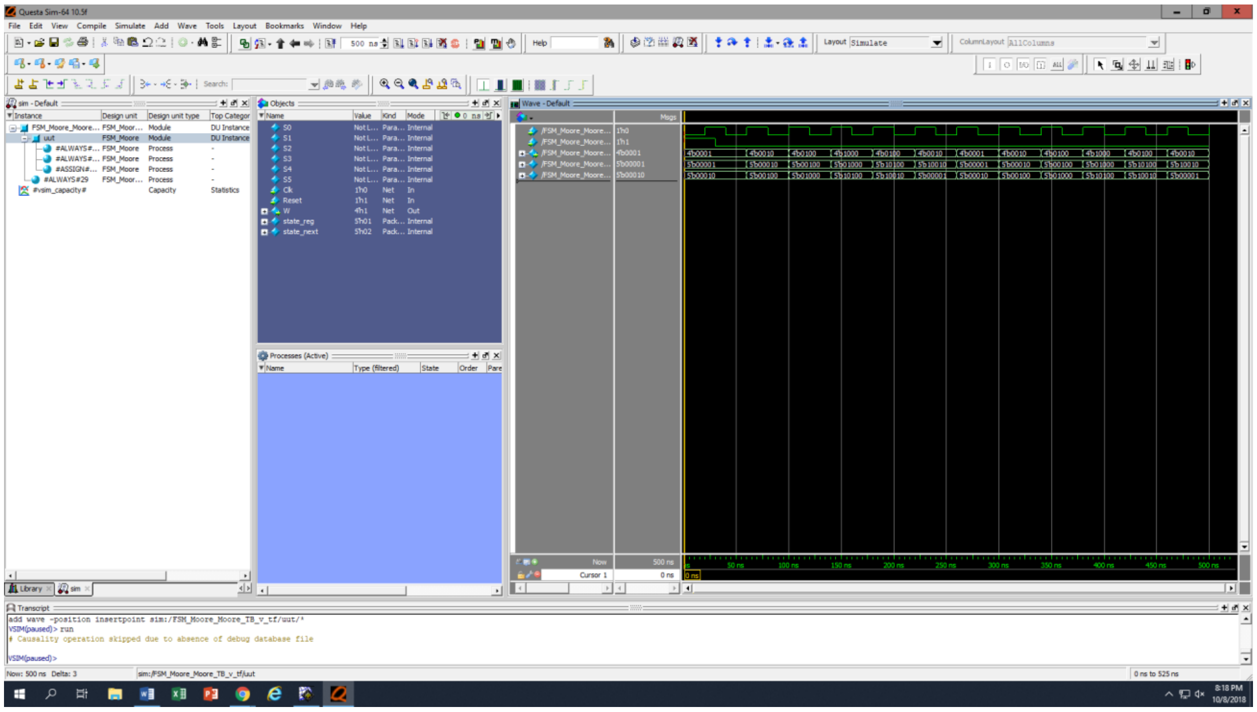
Moore Testbench:

```
module FSM_Moore_Moore_TB_v_tf();

// DATE:     19:59:14 10/08/2018
// MODULE:   FSM_Moore
// DESIGN:   FSM_Moore
// FILENAME: Moore_TB.v
// PROJECT:  Lab4
// VERSION:
```

```
// Inputs
   reg Clk;
   reg Reset;

// Outputs



// Bidirs


// Instantiate the UUT
   FSM_Moore uut (
      .Clk(Clk),
      .Reset(Reset),
      .W(W)
      );

// Clock Signal
          always
          begin
                    Clk = 1'b0;
                    #20;
                    Clk = 1'b1;
                    #20;
          end

// Initialize Inputs
      initial begin
         Clk = 0;
```

```
        Reset = 1;
                    #30;
                    Reset = 0;
    end

endmodule
```

Moore Output Waveform:



```
add wave -position insertpoint sim:/FSM_Moore_Moore_TB_v_tf/uut/*
VSIM(paused)> run
# Causality operation skipped due to absence of debug database file

VSIM(paused)>
```

Part B: Mealy FSM

```
module FSM_Mealy(Clk,Reset,Up,Q);
```

```
input Clk,Reset,Up;

output [1:0] Q;


reg [1:0] state_reg, state_next;


parameter S0 = 2'b00;

parameter S1 = 2'b01;

parameter S2 = 2'b10;

parameter S3 = 2'b11;


//state register

always @ (posedge Clk, posedge Reset)

if (Reset) state_reg <= S0;

      else

      state_reg <= state_next;


//Combinational Logic

always @ (*)

case (state_reg)

S0: if(Up) state_next = S1;

        else   state_next = S3;

S1: if(Up) state_next = S2;

        else   state_next = S0;

S2: if(Up) state_next = S3;

        else   state_next = S1;

S3: if(Up) state_next = S0;

        else   state_next = S2;


default: state_next = S0;
```

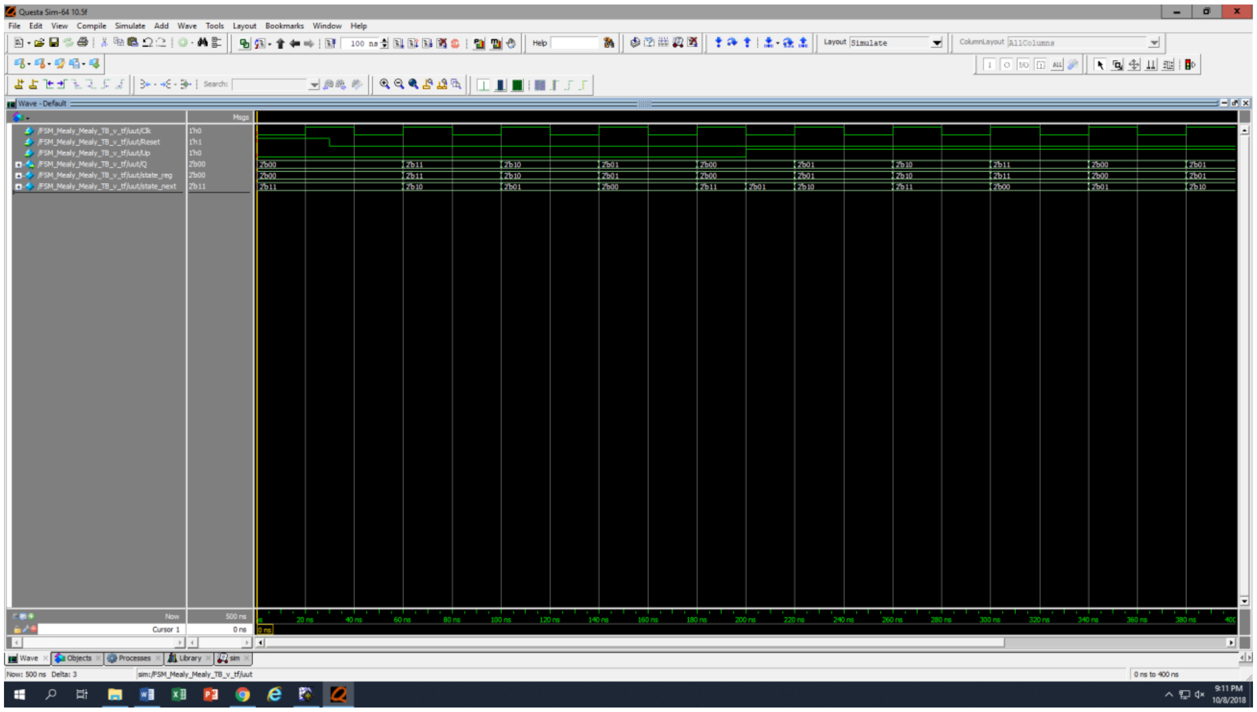
```
    endcase

    //Output Logic
    assign Q = state_reg;

endmodule
```

Mealy Testbench:

```
module FSM_Mealy_Mealy_TB_v_tf();

// DATE:     20:36:25 10/08/2018
// MODULE:   FSM_Mealy
// DESIGN:   FSM_Mealy
// FILENAME: Mealy_TB.v
// PROJECT:  Lab4
// VERSION:



// Inputs
    reg Clk;
    reg Reset;
    reg Up;



// Outputs
    wire [1:0] Q;

// Bidirs
// Instantiate the UUT
   FSM_Mealy uut (
      .Clk(Clk),
      .Reset(Reset),
      .Up(Up),
      .Q(Q)
      );

// Clock Signal
         always
         begin
                  Clk = 1'b0;
                  #20;
                  Clk = 1'b1;
                  #20;
         end

// Initialize Inputs
      initial begin
                   Clk = 1'b0;
         Reset = 1'b1;
                   #30;
                   Reset = 1'b0;
                   Up = 1'b1;
                   #80;
                   Up = 1'b0;
                   #80
      end
```

endmodule

Mealy Output Waveform:



```
/FSM_Mealy_Mealy_TB_v_tf/uut/Clk          1'h0
/FSM_Mealy_Mealy_TB_v_tf/uut/Reset        1'h1
/FSM_Mealy_Mealy_TB_v_tf/uut/Up           1'h0
/FSM_Mealy_Mealy_TB_v_tf/uut/Q            2'b00   2'b00 2'b11 2'b10 2'b01 2'b00 2'b01 2'b10 2'b11 2'b00 2'b01
/FSM_Mealy_Mealy_TB_v_tf/uut/state_reg    2'b00   2'b00 2'b11 2'b10 2'b01 2'b00 2'b01 2'b10 2'b11 2'b00 2'b01
/FSM_Mealy_Mealy_TB_v_tf/uut/state_next   2'b11   2'b11 2'b10 2'b01 2'b00 2'b11 2'b01 2'b10 2'b11 2'b00 2'b01 2'b10
```

Now: 500 ns Delta: 3   sim:/FSM_Mealy_Mealy_TB_v_tf/uut   0 ns to 400 ns