6.15 Write a behavioral architecture declaration for the DFF shown in Figure P6.15. Use an if statement and an elsif statement. The signal *SET* (asyn) is clock independent—that is, it overrides the clock.

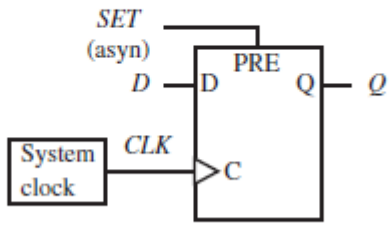

FIGURE P6.15

6.44 Write a dataflow architecture declaration for the counter circuit in Figure P6.44. Use three conditional signal assignments. The signal *INIT* (asyn) is clock independent—that is, it overrides the clock.

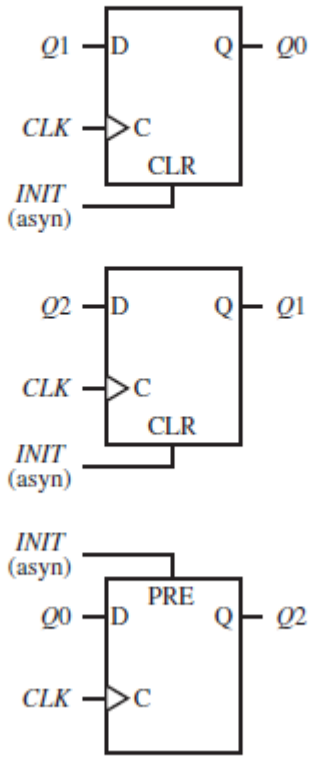

FIGURE P6.44

6.45 Write the required library clause, use clause (for the package IEEE.STD_LOGIC_1164), and entity declaration for the counter circuit in problem 6.44.

6.46 Combine your code for problems 6.44 and 6.45 to form a complete VHDL design. Obtain a waveform diagram that shows correct functionality for the complete VHDL design.

6.59 Use the arithmetic method to write a behavioral architecture declaration with a process for a binary up counter that increment by 2 as shown in Figure P6.59. The signal *RST* (asyn) is clock independent—that is, it overrides the clock.

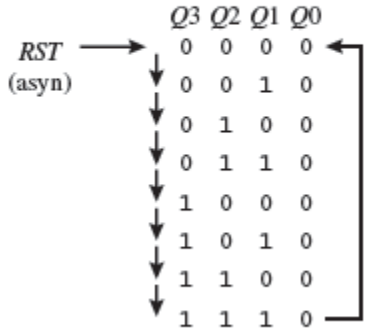

FIGURE P6.59

6.60 Write the required library clause, use clauses, and entity declaration for the counter in problem 6.59.

6.61 Combine your code for problems 6.59 and 6.60 to form a complete VHDL design. Obtain a waveform diagram that shows correct functionality for the complete VHDL design.

6.67 For a crystal clock oscillator frequency of 100 MHz, how many clock cycles must be counted for each half-period to generate an accurate frequency of 10 Hz and also an accurate frequency of 4 Hz?

6.70 Use the PS/NS tabular method to write a behavioral architecture declaration for the counter shown in Figure P6.70. The signal *SET* (syn) is clock dependent—that is, it doesn't take effect until the clock ticks.

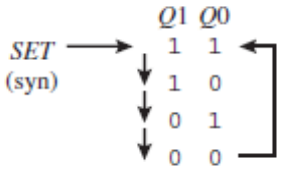

FIGURE P6.70

6.71 Write the required library clause, use clause (for the package IEEE.STD_LOGIC_1164), and entity declaration for the counter in problem 6.70.

6.72 Combine your code for problems 6.70 and 6.71 to form a complete VHDL design. Obtain a waveform diagram that shows correct functionality for the complete VHDL design.