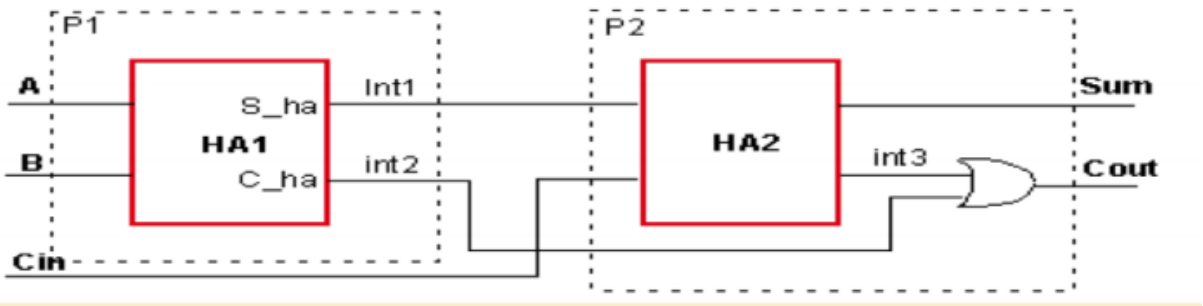
Implementing the Design on FPGA

1. Lab Description

Part A: Full Adder

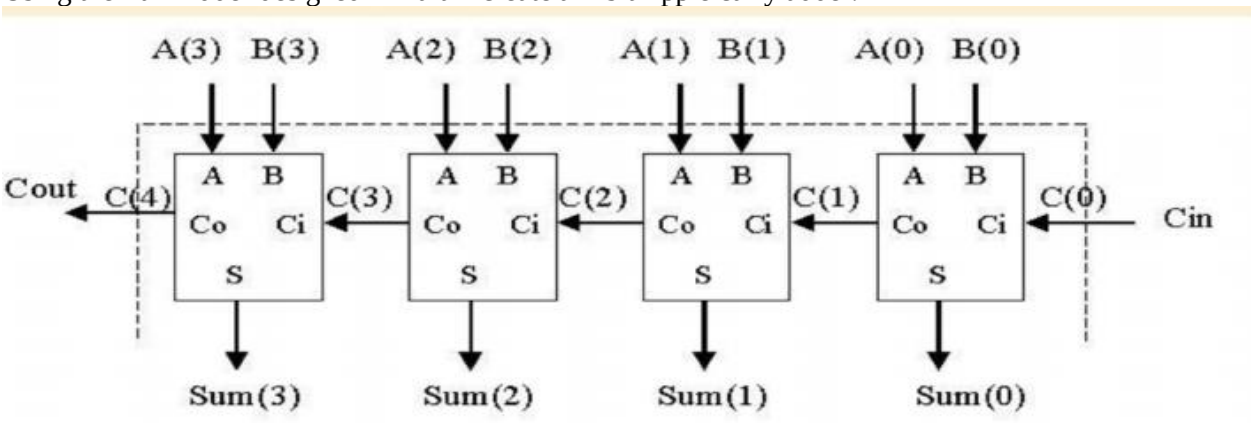


Implement your design on FPGA using the verilog code from Practice Lab No 2.

Connect the inputs, A, B, Cin to switches whereas output Sum and Cout to LED.

Part B: 4-Bit Ripple Carry Adder

Using the Full Adder designed in Part B create a 4-bit ripple carry adder.



Implement your design on FPGA using the verilog code from Practice Lab No 2.

Connect the input bus A [3:0] and B [3:0] to switches whereas output Sum and Cout to LED's.

Submit your .XDC file for Part A and B here.

A. Full Adder Code:

```
set_property IOSTANDARD LVCMOS33 [get_ports Cout]
set_property IOSTANDARD LVCMOS33 [get_ports A]
set_property IOSTANDARD LVCMOS33 [get_ports Sum]
set_property IOSTANDARD LVCMOS33 [get_ports B]
set_property IOSTANDARD LVCMOS33 [get_ports Cin]
```

```
set_property PACKAGE_PIN H17 [get_ports Cout]
set_property PACKAGE_PIN K15 [get_ports Sum]
set_property PACKAGE_PIN J15 [get_ports A]
set_property PACKAGE_PIN L16 [get_ports B]
set_property PACKAGE_PIN M13 [get_ports Cin]
```

B. Ripple Carry Adder Code:

```
set_property IOSTANDARD LVCMOS33 [get_ports {Sum[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports Cout]
set_property IOSTANDARD LVCMOS33 [get_ports Cin]
set_property IOSTANDARD LVCMOS33 [get_ports {A[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {Sum[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {Sum[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {A[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {Sum[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {A[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {A[0]}]
set_property PACKAGE_PIN J15 [get_ports {A[0]}]
set_property PACKAGE_PIN L16 [get_ports {A[1]}]
set_property PACKAGE_PIN M13 [get_ports {A[2]}]
set_property PACKAGE_PIN R15 [get_ports {A[3]}]
set_property PACKAGE_PIN R17 [get_ports {B[0]}]
set_property PACKAGE_PIN T18 [get_ports {B[1]}]
set_property PACKAGE_PIN U18 [get_ports {B[2]}]
set_property PACKAGE_PIN R13 [get_ports {B[3]}]
set_property PACKAGE_PIN T8 [get_ports Cin]
set_property PACKAGE_PIN R18 [get_ports Cout]
set_property PACKAGE_PIN N14 [get_ports {Sum[3]}]
set_property PACKAGE_PIN J13 [get_ports {Sum[2]}]
set_property PACKAGE_PIN K15 [get_ports {Sum[1]}]
set_property PACKAGE_PIN H17 [get_ports {Sum[0]}]
```