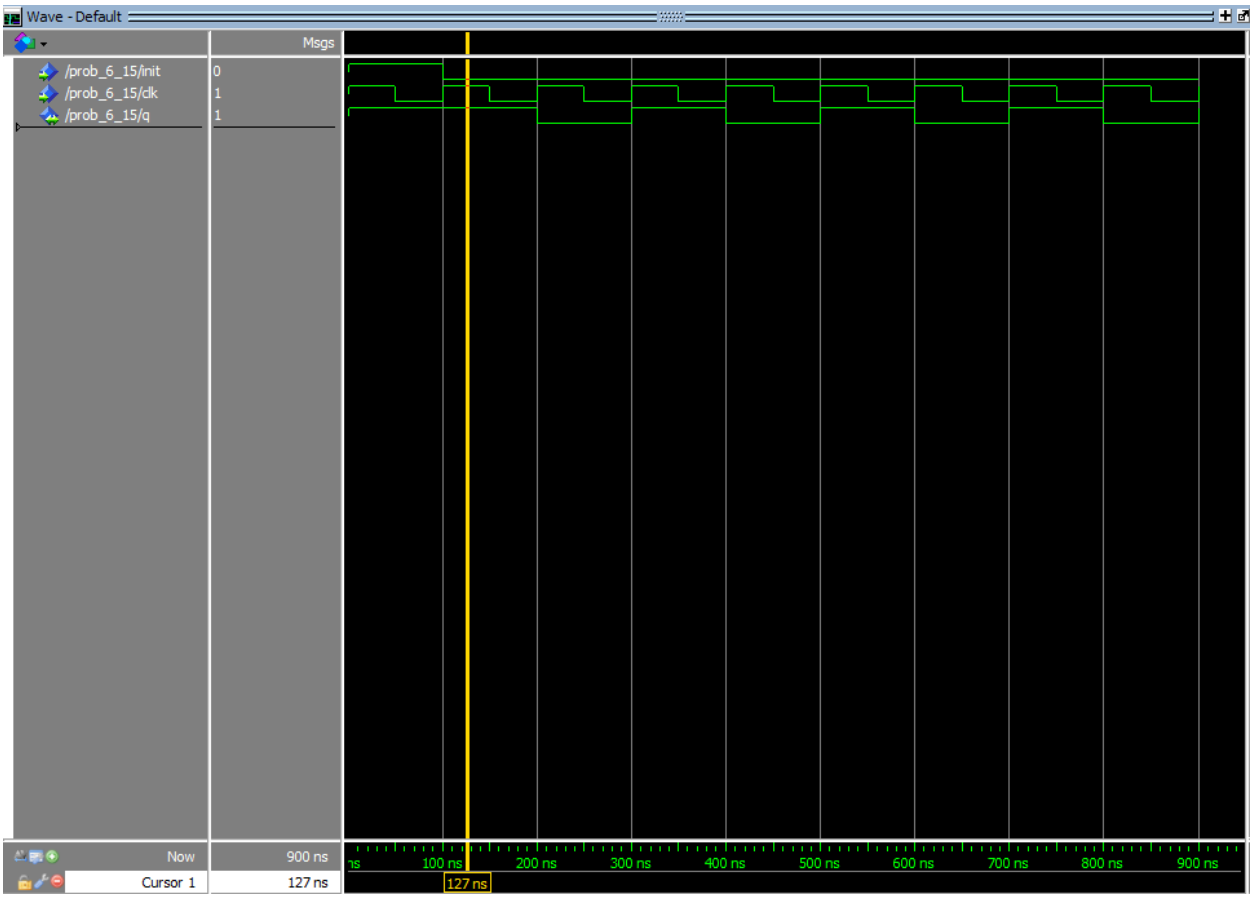
Lab 4

Problem 6.15:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Prob_6_15 is port (
        init, clk : in std_logic;
        q : inout std_logic
        );
end Prob_6_15;

architecture behavioral of Prob_6_15 is
begin
process (init, clk)
begin
        if init = '1' then q <= '1';
        elsif rising_edge(clk) then
                case q is
                        when '0' => q <= '1';
                        when '1' => q <= '0';
                        when others => null;
                end case;
        end if;
end process;
end behavioral;
```



Problem 6.44:

```
architecture dataflow of Prob_6_44 is
        signal q2, q1, q0: std_logic;
begin
        q2 <= (not q(2) and not q(1) and q(0));
        q1 <= (q(2) and not q(1) and not q(0));
        q0 <= (not q(2) and q(1) and not q(0));

        q <= "001" when init = '1' else
                (q2,q1,q0) when rising_edge(clk);
end dataflow;
```

Problem 6.45:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Prob_6_44 is port (
        init, clk : in std_logic;
        q : inout std_logic_vector (2 downto 0)
```

```
        );
end Prob_6_44;
```

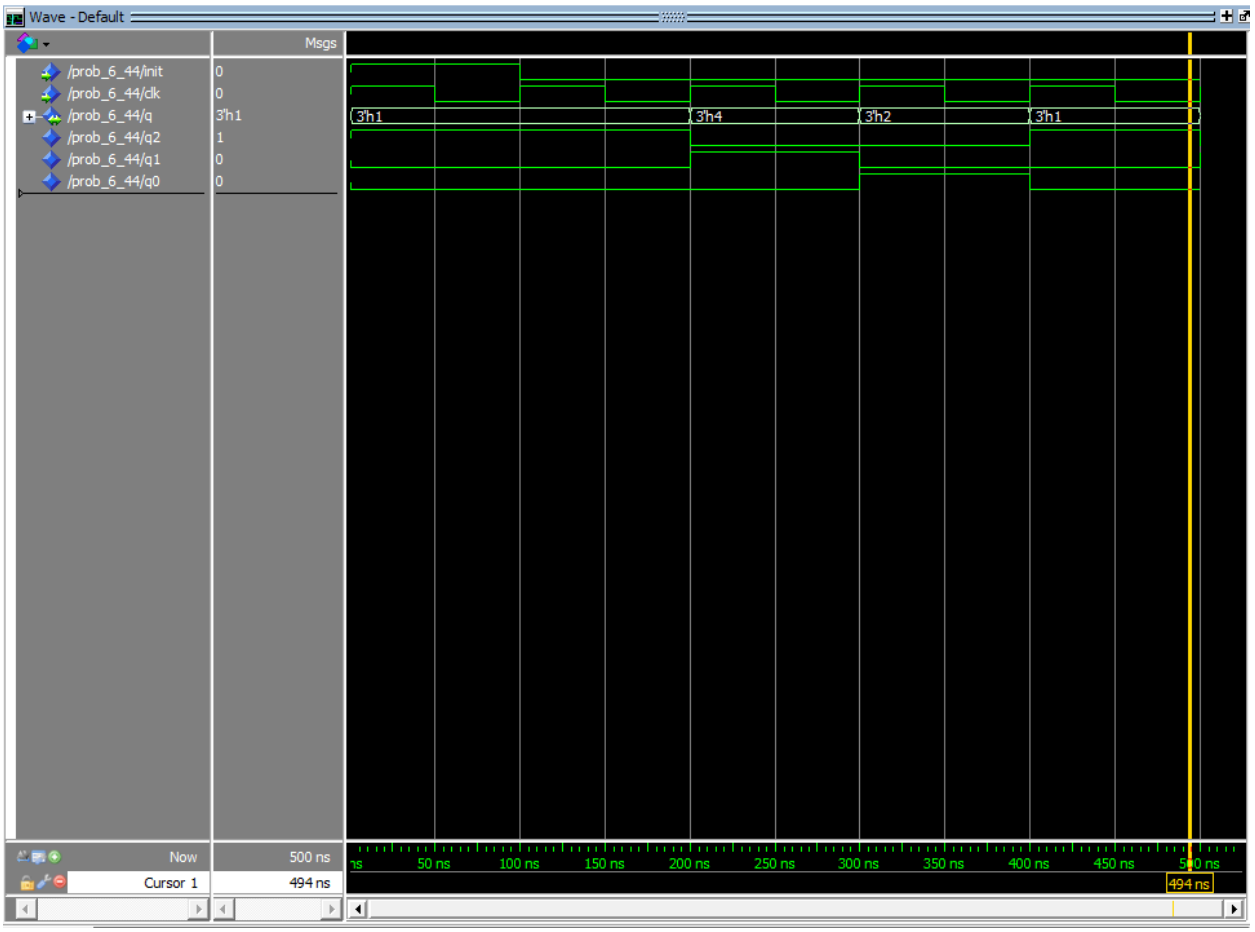
Problem 6.46:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Prob_6_44 is port (
        init, clk : in std_logic;
        q : inout std_logic_vector (2 downto 0)
        );
end Prob_6_44;

architecture dataflow of Prob_6_44 is
        signal q2, q1, q0: std_logic;
begin
        q2 <= (not q(2) and not q(1) and q(0));
        q1 <= (q(2) and not q(1) and not q(0));
        q0 <= (not q(2) and q(1) and not q(0));

        q <= "001" when init = '1' else
                (q2,q1,q0) when rising_edge(clk);
end dataflow;
```



Problem 6.59:

```
architecture behavioral of Prob_6_59 is
begin
process (clk, rst)
begin
        if rst = '1' then q <="0000";
        elsif rising_edge(clk) then q <= q + 2;
        end if;
end process;
end behavioral;
```

Problem 6.60:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity Prob_6_59 is port (
        rst, clk : in std_logic;
```

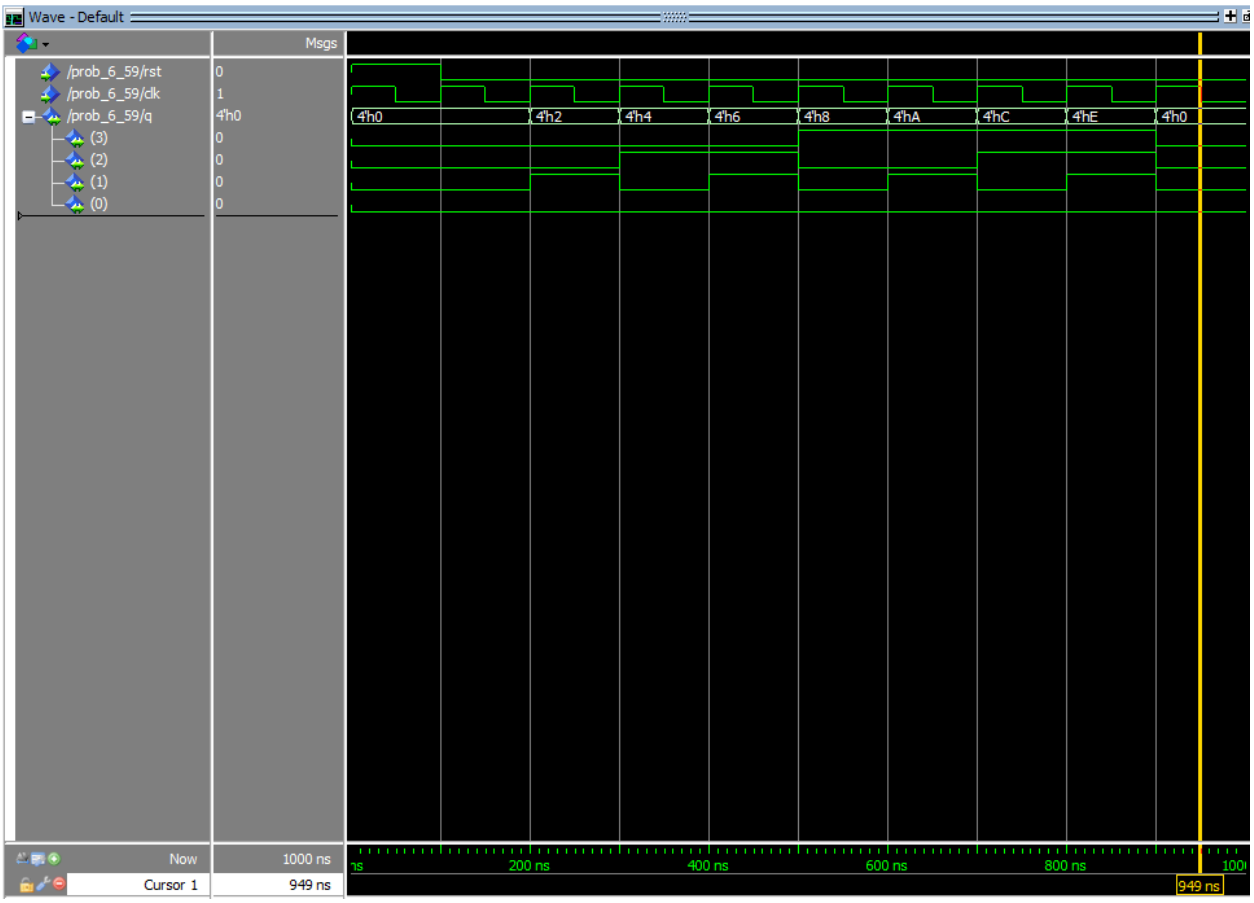
```
        q : inout std_logic_vector (3 downto 0)
        );
end Prob_6_59;
```

Problem 6.61:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity Prob_6_59 is port (
        rst, clk : in std_logic;
        q : inout std_logic_vector (3 downto 0)
        );
end Prob_6_59;

architecture behavioral of Prob_6_59 is
begin
process (clk, rst)
begin
        if rst = '1' then q <="0000";
        elsif rising_edge(clk) then q <= q + 2;
        end if;
end process;
end behavioral;
```



Problem 6.67:

100 MHz/10 Hz = 10 million/2 = 5 million clock cycles for each half period to generate an accurate frequency of 10 Hz.

100 MHz/4 Hz = 25 million/2 = 12.5 million clock cycles for each half period to generate an accurate frequency of 4 Hz.

Problem 6.70:

```
architecture behavioral of Prob_6_70 is
begin
process (set, clk)
begin
        if set = '1' then q <= "11";
        elsif rising_edge(clk) then
                case q is
                        when "11" => q <= "10";
                        when "10" => q <= "01";
                        when "01" => q <= "00";
                        when "00" => q <= "11";
                        when others => null;
```

```
                end case;
        end if;
end process;
end behavioral;
```

Problem 6.71:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Prob_6_70 is port (
set, clk : in std_logic;
q : inout std_logic_vector (1 downto 0)
);
end Prob_6_70;
```

Problem 6.72:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Prob_6_70 is port (
set, clk : in std_logic;
q : inout std_logic_vector (1 downto 0)
);
end Prob_6_70;

architecture behavioral of Prob_6_70 is
begin
process (set, clk)
begin
        if set = '1' then q <= "11";
        elsif rising_edge(clk) then
                case q is
                        when "11" => q <= "10";
                        when "10" => q <= "01";
                        when "01" => q <= "00";
                        when "00" => q <= "11";
                        when others => null;
                end case;
        end if;
end process;
end behavioral;
```


Wave - Default
Msgs
/prob_6_70/set
/prob_6_70/clk
/prob_6_70/q
(1)
(0)
-No Data-
-No Data-
-No Data-
-No Data-
-No Data-
2'h3
2'h2
2'h1
2'h0
2'h3
2'h2
2'h1
2'h0
Now
900 ns
Cursor 1
988 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns