unsaved

EDITOR ✓NAV-TLV LOG

```
\m5_TLV_version 1d: tl-x.org
\m5
   // ========================================
   // Welcome, new visitors! Try the "Learn" menu.
   // ========================================

   // use(m5-1.0)   /// uncomment to use M5 macro library.
\SV
   // Macro providing required top-level module definition, random
   // stimulus support, and Verilator config.
  // 'include "sqrt32.sv"
   m5_makerchip_module   // (Expanded in Nav-TLV pane.)
\TLV
   // $reset = *reset;
   // Simple Pipeline (Pythagoras's Theorem TL-Verilog .....

   |calc
      @0
         $aa[31:0] = *cyc_cnt[3:0];
         $bb[31:0] = *cyc_cnt[3:0];
      @1
         $aa_sq[31:0] = $aa * $aa;
         $bb_sq[31:0] = $bb * $bb;
      @2
         $cc_sq[31:0] = $aa_sq + $bb_sq;
      @3
         $cc[31:0] = sqrt($cc_sq);
                 //...
   //
   // Assert these to end simulation (before the cycle limit).
   *passed = *cyc_cnt > 40;
   *failed = 1'b0;
\SV
   endmodule
```