RISCV_MYTH_Workshop (April-2025)

Day-3: Lab Assignment

TL-Verilog File Path in Makerchip IDE Server:

1. Makerchip IDE Platform View (Pythagoras Theorem with Valid condition) - https://www.makerchip.com/sandbox/0qxfOhqWZ/076hA1j#)
2. Comb_Logic_Gates - (https://www.makerchip.com/sandbox/0VOflhWJM/0DRh5Ny#)
3. Mux Logic (2x1) - (https://www.makerchip.com/sandbox/0VOflhWJM/0Nxh0D7#)
4. Arithmetic using Bit Vectors - (https://www.makerchip.com/sandbox/0o2fXhW6R/0Q1hkMP#)
5. Mux Block Level (2x1 with Bit Vectors) - (https://www.makerchip.com/sandbox/0o2fXhW6R/0Wnh5RK#)
6. Combinational Calculator (32-Bit w/o retiming concept) - (https://www.makerchip.com/sandbox/0BBfVhvj2/01jhM2Y#)
7. Sequential circuit (Fibonacci Series with Reset Control) - (https://www.makerchip.com/sandbox/0BBfVhvj2/03lhp6n#)
8. Sequential circuit (4-Bit Free Runing Counter) - (https://www.makerchip.com/sandbox/0BBfVhvj2/0vgh7xB#)
9. Sequential Calculator (32-Bit with reset 4x1 mux operation) - (https://www.makerchip.com/sandbox/0PNf4hBRp/0X6hXoM#)
10. Pipeline and Retiming with Valid check (Example: Pythagoras Therorem) - (https://www.makerchip.com/sandbox/0qxfOhqWZ/0g5hAZ0#)
11. Single Cycle Pipeline (Calculator and free Runing Counter with reset control) - (https://www.makerchip.com/sandbox/0qxfOhqWZ/0nZh7NW#)
11. Two Cycle Pipeline (Calculator and free Runing Counter with retiming reset control) - (https://www.makerchip.com/sandbox/0qxfOhqWZ/0qjh8jy#)
12. Hierarchy TL-Veliog Abstraction (Example: Pythagoras Theorem) - (https://www.makerchip.com/sandbox/0qxfOhqWZ/0r0h8ly# and https://www.makerchip.com/sandbox/0qxfOhqWZ/0xGh1oN#)

Day-4 and Day-5: Lab Assignment

RISC-V CPU Micro-architecture:
1. TL-Verilog RISC-V CPU (RV32I) - (https://www.makerchip.com/sandbox/0qxfOhqWZ/0DRh5Aj#))

RISC-V CPU Micro-architecture with Pipiline Concept:

1. TL-verilog code for 3-Cycle Pipeline RISC-V RV32I CPU Architecture - (https://www.makerchip.com/sandbox/0G6fJh1LR/0KOh2WB#)

RISC-V CPU Micro-architecture with Pipiline Concept(@1, @2, @3 and @4):
Topics Covered:
1. Pipilining RISC-V CPU, 2. Load & Store Instructions and Colplete RISC-V CPU.

1. TL-Verilog Code for Complete RISC-V RV32I CPU Instruction Set with Load and Store (Jump & Loops) - (https://www.makerchip.com/sandbox/0rkfAhG55/03lhpK4#)