saved 7 minutes ago û

```
\equiv
 EDITOR
        ✓ NAV-TLV
                   LOG
   \m5_TLV_version 1d: tl-x.org
 2 √ \m5
 3
 4
       5
       // Welcome, new visitors! Try the "Learn" menu.
 6
       7
 8
       //use(m5-1.0)
                      /// uncomment to use M5 macro library.
 9 ▼ \SV
       // Macro providing required top-level module definition, random
10
       // stimulus support, and Verilator config.
11
                           // (Expanded in Nav-TLV pane.)
12
      m5_makerchip_module
13 ▼ \TLV
14
       // Combinational Calculators for Addition, Subtraction, Multiplication
15
       // $reset = *reset;
       // Stimulus .....
16
       |calc
17 ▼
18 ▼
19
            // Stimulus for Calculator .....
20
            $reset = *reset;
            p[1:0] = *cyc_cnt[1:0];
21
22
            $reset_zero[31:0] = 32'b0;
23
            val2[31:0] = rand2[3:0];
24
25 ▼
            // Stimulus for Free Runing Counter.....
26
            \sin[0:0] = 1;
27
            \sin 2[0:0] = 0;
28
            // Summation of next state (feedback) and trigger input "1"....
29
            sum_sq[3:0] = sinp1 + >>1scnt[3:0];
       // Arithmetic Functions (Add, Subt, Mult and Div).....
30
31 ▼
32 ▼
         @1
            Add_out[31:0] = val1_sq + val2;
33
34
            Sub_out[31:0] = val1_sq - val2;
35
            Mul_out[31:0] = val1_sq * val2;
36
            $Div_out[31:0] = $val1_sq / $val2;
37
            // Mux (4x1) Operation....
38 ▼
            calc_out[31:0] = (sop == 00 & reset == 0) ? \\Add_out:
39
                             ($op == 01 & $reset == 0) ? $Sub_out:
                             ($op == 10 & $reset == 0) ? $Mul_out:
40
41
                             ($op == 10 & $reset == 0) ? $Div_out:
42
                             $reset_zero;
43 ▼
            val1_sq[31:0] = & calc_out;
44
45
            // Free Runing Counter Mux (2x1) Operation .....
            cnt[3:0] = (seset == 1) ? sinp2:
46 ▼
47
                                        $sum_sq;
            //
48
49
       //...
50
       // Assert these to end simulation (before the cycle limit).
51
       *passed = *cyc_cnt > 40;
       *failed = 1'b0;
52
53 ▼ \SV
54
       endmodule
55
```

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