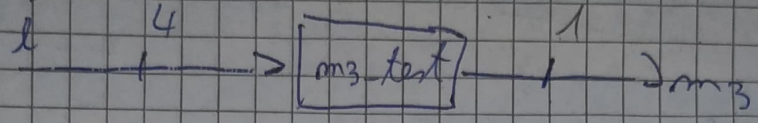
Homework - T2

Regulas Alexandru

1.

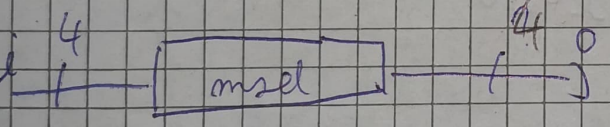
```
module BCD-3421 (
    input [3:0] i,
    output reg [3:0] o
);
    always @(*) begin
        case (i)
        4'b0000 : o = 4'b0000;
        4'b0001 : o = 4'b0111;
        4'b0010 : o = 4'b0110;
        4'b0011 : o = 4'b0101;
        4'b0100 : o = 4'b0100;
        4'b0101 : o = 4'b1011;
        4'b0110 : o = 4'b1010;
        4'b0111 : o = 4'b1001;
        4'b1000 : o = 4'b1000;
        4'b1001 : o = 4'b1111;
        endcase
    end
endmodule
```

2.



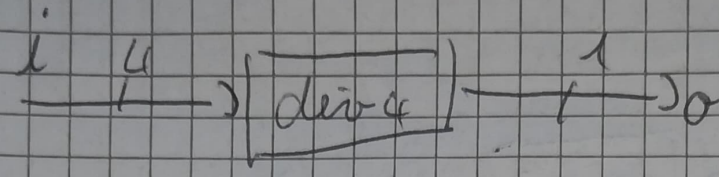

```
module m3_test (
    input [3:0] i,
    output reg o
);
always @(*) begin
    if (i==0 || i==3 || i==6 || i==9 ||
        i==12 || i==15)
        o=1
    else
        o=0
end
end module
```

3)



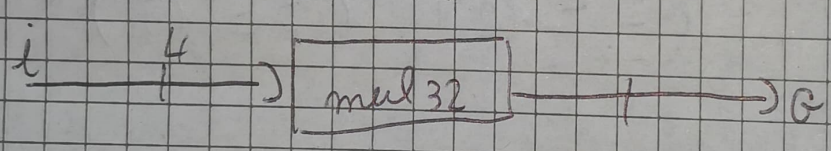

```
module msel (
    input [3:0] i,
    output [3:0] o
);
assign o = (i<=9 && i>=0) ? i:
                              4'b0001;
end module
```

4.




```
module div_4 (
    input [3:0] i,
    output [1:0] o
);
    assign o = i >>2;
endmodule
```

5.




```
module mul_32 (
    input [3:0] i,
    output [9:0] o
);
    assign o = i<<5;
endmodule
```