Lecture-9

Intel 8085 Microprocessor

It is a 40-pin DIP(Dual in package) chip, base on NMOS technology, on a single chip of silicon. It requires a single +5v supply between Vcc at pin no 40 and GND at pin no 20. It can address directly 2^{16} memory locations or 6536 memory locations or 64k memory locations using 16 address line (A_{15}-A_0).

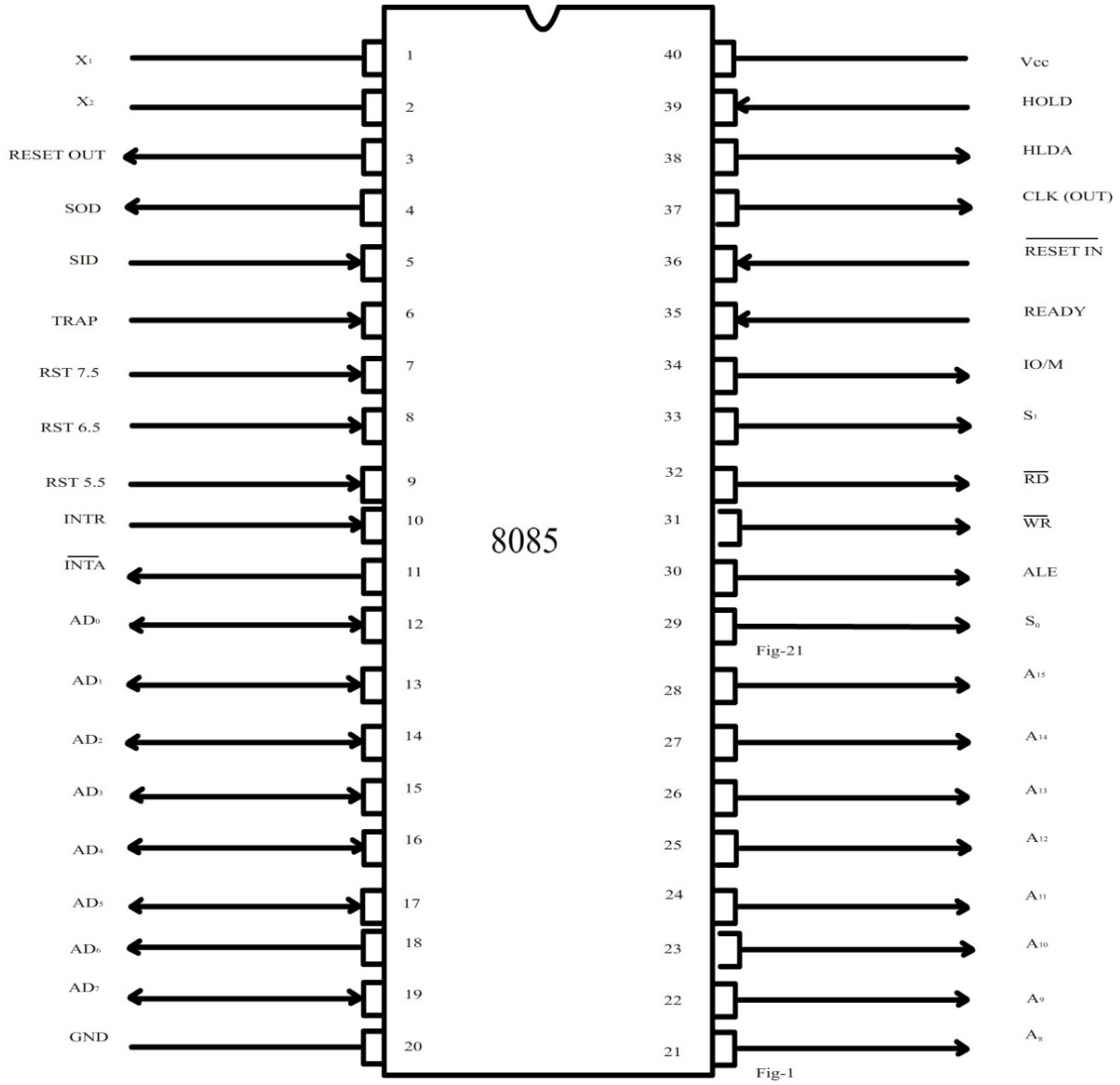


Fig-21

Fig-1

Pin no 28 to 21 gives as the higher order 8 bits of the address (A_{15}-A_8).these 8- address lines are uni-directional tri-state address lines these address lines becomes tri-state under three conditions namely.

(a) During DMA (direct memory access)operation

(b) When a HALT instruction is executed

(c) When μp is being RESET.

A_{15}-A_8 at pin no 19 to pin no 12 → pin no 19 to pin no 12, marked A_7-A_0 is used for dual purpose. The μp during it operation shall move from one state to the other. There are ten (10) different states for the μp namely.

(1) RESET STATE → (T_{RESET}) → μp can be in T_{RESET} state for an integral multiple clock cycle.

(2) WAIT STATE → (T_{WAIT}) → it can be in this state for an integral no of clock cycle. The duration being determined by an external control signal input marked READY.

(3) HOLD STATE → (T_{HOLD}) → H depends upon the external control signal input HOLD.

(4) HALT STATE → (T_{HALT}) → μp enter there state when an ILT instruction is executed by μp it remains in this state till such time when an external signal dictated by the use asked the μp to perform further duties.

(5) The other states, the μp can be IN are marked T_1,T_2,T_3,T_4,T_5 & T_6 states each of them states are of one clock period duration each of there states clearly identifies the predetermined timing

slots T_1,T_2,T_3,T_4,T_5 & T_6 μp perform specific very well defined activities during these states.

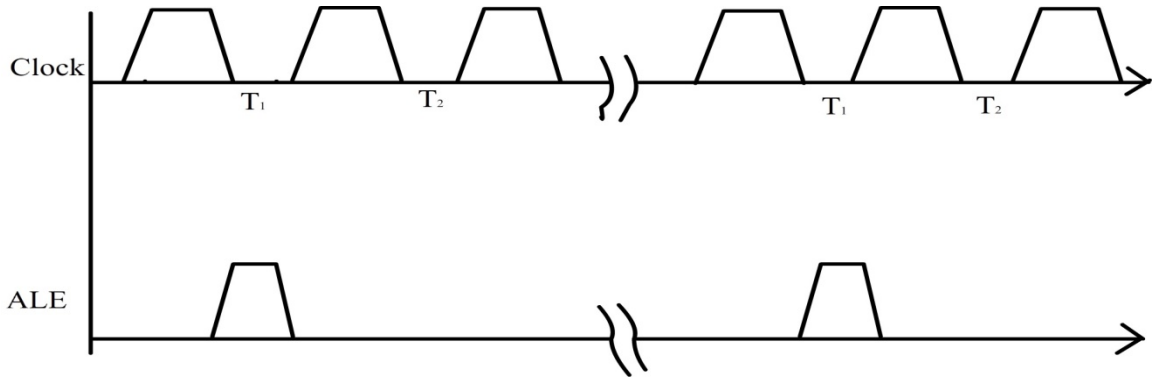
Pin Configuration of Intel 8085A Microprocessor:

Pin no 19 to pin no 12 shall be utilize by the μp to sent lower order bits of the 8^{16} –bit of information during T_1 timing slots and therefore, the same 8-points shall be utilized as bi-directional data bus (BDB) for data transfer operation in the subsequent timing slots T_2 & T_3 Hence these pins are designated AD_7 to AD_6

These 8- lines are also tri-state line they will be tri-stated during T_4, T5 & T_6 states. They will also be tri-stated during DMA operation and when a HALT instruction is executed. These lines will also be tri-stated for a very-short duration of time (few neon sec) between T_1 & T_2 states.

ADDRESS LATCH ENABLE (ALE) AT PIN NO 30

it is a single pulse issued every T_1 state of the μp as shown on fig-2.since the lower order 8-bits of the address information A_7 to A_0 is available at pin no 19 to 12, when ALE pulse exists at pin no 30. We can use these information to latch the lower order bits of the address externally using (say) an 8212 register latch once save on an external latch the lower order address A_7 to A_0 shall be available at the output of the register latch for the subsequent states T_2, T3, T4, T5 & T_6, while pin no 19 to 12 can then be utilized by the μp for bi-directional operation.



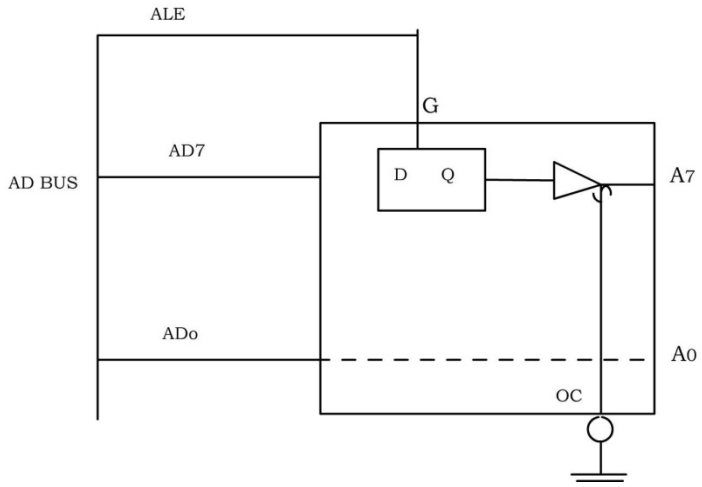
The manner of utilization of pins 19 to 12 is known as time multiplexed mode of operation.

De multiplexing the Address bus AD_1 –AD_0:

The 8085 A uses a multiplexed address-data bus. This is due to limited number of pins on the 8085A-IC. Low-order 8-bits of the memory address (or I/O address) appear on the AD bus during the first clock cycle. (T_1 state of an m/c cycle) It then becomes the data bus during the second and third clock cycles (T_2 and T_3 states). ALE, address latch enable signal occurring during the T_1 state of a m/c cycle is used to latch the address into the on-chip latch of certain peripherals such as 8155/8156/8355/8755A. These chips ALE input pin is connected to the ALE output pin of the 8085 A, thus allowing a direct interface with the 8085 A. Thus IC chips internally de multiplex the AD bus using the ALE signal. Since a majority of peripheral devices do not have the internal multiplexing facility, there is external hardware necessity for it.

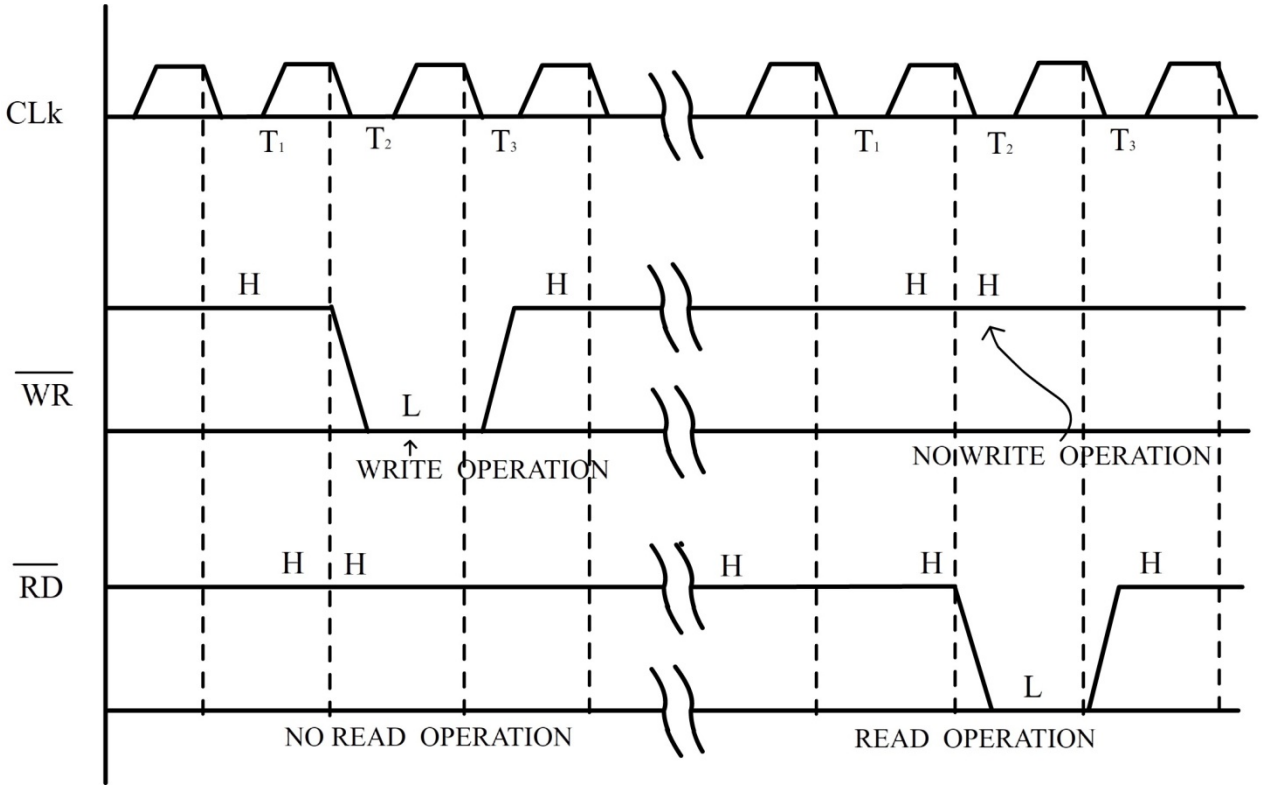
Fig. shows a schematic that uses a latch and the ALE signal to de multiplex the bus. The bus AD_1-AD_0 is connected as the input to the latch 74LS373. The ALE signal is connected to the enable (G) pin of the latch, and the output control (OC) signal of the latch is grounded. When ALE goes high during the T_1 state of a m/c cycle, the

latch is transparent in the output of the latch changes according to the input. The CPU is putting lower-order bits of address during this time. When the ALE goes LOW, the address bits get latched on the output and remain so until the next ALE signal.



Read & Write Control signals at pin no 32 & pin no 31 $\overline{RD}$ & $\overline{WR}$ →

The BDB at pin no 19 to 12 are used for bi-directional data transfer operation T_2 & T_3 states when the BDB is inputting the information from the external world into the μp, we say that μp is in READ MODE and operation is READ operation. When the μp is outputting 8-bit of information to the external world through BDB we have a WRITE operation μp is in OUTPUT MODE or WRITE MODE. To tell the external world that μp is in WRITE MODE. μp Issues a control signal output $\overline{WR}$ at pin no 31 it is normally HIGH & becomes active & LOW. It goes LOW during T_2 state and goes HIGH again during T_3 state of the. This is shown is fig.3



When the BDB is in the input mode for READ operation, the $\overline{RD}$ control signal. Output goes Low during T_2 state and goes HIGH during T_3 state. Note that the normal state of $\overline{RD}$ is HIGH. Also note that for obvious reasons $\overline{RD}$ & $\overline{WR}$ are not made active LOW simultaneously. Note further whenever, the BDB is made to be in the INPUT MODE by the μp, it issues the $\overline{RD}$ control signal output by making it active LOW as described and it is for the user to beep the appropriate 8-bit data either from the memory or from a peripheral device at this appropriate time similarly during a WRITE operation μp first send the desired address in the address lines during T_1 states. Thereafter, if places the desired 8-bit data on the BDB which is na in the output mode and then issues the $\overline{WR}$ control signal output as

described. It is for the user to take appropriate action externally by it interfacing circuitry so that the data so placed goes to the appropriate device.

IO/$\bar{M}$ at pin no 34 →

O/$\bar{M}$ is an output tri-state control signal. It is active both way whenever the address issued by the μp on the address lines refers to the memory then the μp makes IO/$\bar{M}$ LOW throughout T_1,T_2,T_3,T_4,T_5 & T_6 states to indicate the external world that the address so sent belongs to the memory and data on the BDB refers to the memory.

Whenever the address in the address lines. Refers to an I/O device the μp makes IO/$\bar{M}$ control signal output HIGH to tell the external world that the address in the address lines refer to I/O device and the data in the BDB refers to an I/O device.

Note that IO/$\bar{M}$ signal is LOW or HIGH as the case may be throughout six timing slots T_1,T_2,T_3,T_4,T_5 & T_6 states. It is for the user to make use of the facilities give to develop proper interfacing circuitry.