Lecture-17

MICROPROCESSOR INSTRUCTIONN SET:

A microprocessor system – there memory microprocessor and the input and output devices- can be thought if in terms of the register it contains random access semiconductor memory is a collection of register .A microprocessor itself consist of general purpose and dedicated registers input and output devices contain register that hold their data.

The function of a microprocessor system is implemented by a sequence of data transfer between register in the memory, the Mp and I/O devices and data transformation that accrue primarily in register within the microprocessor. Each register that can be manipulated under program control is addressable in same manner allowing it to be singled out for use in a data transfer or transformation.

The kinds of individual transfer & transformation possible are specified by the microprocessor instruction sets .each instruction in the set causes one or more data transfer and or transformation. A sequence of instruction consists a program. The content section decode, the program instruction in turn, and using timing signal derived from the system code, content what register transfer or transformation table places and when. Each μP is designed to execute particular function set .instruction set one fixed by design cannot be changed Intel 8080 .which came in to market in 1973 has 72 bases instruction and 244 variation 8085 μP which came in to the market in Jan 1977 is a commercial with lintel 8086 μP has 74 basic

instruction and 246 variation it includes all the 72 instruction of 8080. The two other instructions in 8085 are RIM & SIM.

8085 is faster than 8080 the program written for 8080 can be run without any modification in 8085 but the user has to be careful where the DELAY ROUTINES are involved because of difference in speed of operation.

INSTRUCTION FORMAT:

All instruction of 8085are 1 to 3 bytes in length .the bit pattern of the first cycle is the op code. The bit pattern is decoded in the instruction register and p[provides information used by the timing and content section to generate sequence of elementary operation micro operation that implemented the instruction.

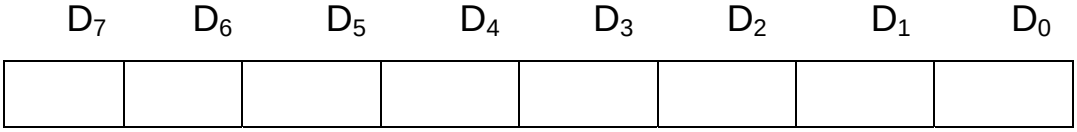

Figure shows a single –byte instruction is the opcode of the instruction. The 8-bit of the op-code available at the memory location N is divided into three potion first group D_7, D_6 recent group $D_5D_4D_3$ and third group $D_2D_1D_0$, $D_2D_1D_0$ when necessary contains the same code SSS. $D_2D_1D_0$ group contain the combination of register DDD. If a register pair is involved the bits. RP is placed in D_5D_4. Whenever D_5D_4 represents the register pair D_3 normal tells whether it is loading operation or storing operation .the first group D_7, D_6 gives the idea of the mnemonic of the operation code.

Whenever 8-byte instruction is used the first byte at memory N is the op-code of the instruction followed by either an 8-bit data or an 8-bit address at memory location N+1.

Whenever a 8-byte instruction is in solved .the first byte at memory location N is the opcode followed by either a-16 bit address or a 16-bit data. The second memory location U (N+1).contain the lower order addresses or data and (n+2) contain the higher order address or data.

ADDRESSING MODES:

Most of the instruction executes requires two operands e.g. transfer of data between two register of a microprocessor system. How the Mp knows the position of these operands. The method of identifying the operands position by the instruction format is known as the addressing mode. Whenever two operands are involved in an instruction the first operand is assumed to be in a register Mp itself. It is for the user to put that operand may be located in one of the following.

i. In any general purpose register in the μP .
ii. In a particular memory location.
iii. It can be immediately available in an instruction format.
iv. I/O device.

In 8085 the following addressing modes are used.

Register addressing:

When the operands for any instruction are available in the internal general purpose register. Only the register need be specified as the address of the operands. Such instruction are said to be use the register addressing mode. These instruction are one byte instruction within that byte i.e. OP code, the register are specified.

E.g., MCV r_1, r2, ADD r, XCHG, DAD rp etc.

MOVr_1, r2 this is an ALP statement and memory of the instruction is more the content of reg (2) to register r_1 .the opcode for the instruction is 01DDD SSS .DDD specifies. The code for the operation register (r_1) and specifies the code for transfer the first two bits 01 specify the MOV operates MOV B, A the opcode 01 000 111=47_H.

ADD r:

This is an ALP statement ADD is the mnemonic for addition and meaning of the instruction is add the content of the register to the content of the accumulator and store the result back in accumulator .the one of the operand is assumed to be in accumulator. By implied addressing mode the second operand is available in any general purpose register specified in the instruction .the op code is 10 000 SSS.

E.g. ADD H. The opcode is 10 000 100=84, the macro ITL is implemented.

(A)←(A) +(r)

Direct addressing mode:

In the addressing mode, the instruction contains the address of the operand contains the address of the operand (external register) involved in the transfer. The 8085A provides.16-bit memory addresses requiring that the address contained in the instruction 1b 16-bit long as a second their byte of the instruction thus it is invariably eg.3-byte instruction.

E.g. LDA addr. This is an ALP statement ADDR in operand field is a symbolic name given to 16-bit address .the systematic name given to

16-bit address symbolic name can be chosen by the user either reference to context LDA is the mnemonic for LOAD accumulator direct. The instruction format for this is as shown.

Opcode	N
$<B_2>$	N+1
$<B_3>$	N+2

Where the memory location 'N' contains the opcode namely 00 110 010=$(3A)_4$ followed by a lower order 8-bits of address $<B_2>$and higher order 8-bit of address $<B_3>$ at memory location NH&N+2 respectively. The meaning of instruction is load the accumulator from the memory location whose address is available directly, in the instruction itself. The macro RTL implemented is,

$$(A) \leftarrow M(B_3,B_2)$$

This is symbolic representation. Only one operand is involved in the instruction e execution.

Register indirect addressing:

The instruction specifies a register pair which contains the address of the memory. Where the data is located or into which the data in to be placed these, the address of the operand is given indirectly through a register pair. In other words, the operand is in memory location or external register share address is available in an internal general purpose register pair.

The H8L register pair is used as a pointer in memory 8885 A, register indirect instruction .the reg H holds the high and reg L holds the large bytes of the effective address e.g. MOV r, M transfer single

bytes from an external reg. M to any of the several integral varying register. External reg M means the external reg pointed by HL the macro RTL implemented is,

$$(r) \leftarrow M (H, L)$$

Before reg indirect instruction are used in a program, a previous instruction most load register pair HL with the appropriate address.

The register pair BC & DE is also used as pointer register in two 8085A instructor i.e. LDAX & STAX rp .the internal register involved for data transfer is always accumulator.

The meaning of LDAX rp is load the accumulator from the memory location. Whose address is available in rp (reg pair either BC or DE). The macro RTL implemented is, the opcode for LDAX B is 00 001 010 = (0A).

Immediate Addressing Mode:

In the type of addressing mode, the operand is available directly in the instruction itself. If the operand data involved is of 8-bits then the instruction is of two bytes. The first byte is the opcode followed by 8-bit data. If 16-bit data is involved in the instruction then the first byte is opcode at memory location N followed by the lower data at memory location NH and higher order data at memory location N+2.

e.g. MVI r, data there is two byte instruction .the instruction format is

00 DDD 110	N
$<B_2>$	N+1

The meaning of the instruction is more the 8-bit data immediately available in the instruction as the 2nd byte to the destination reg r. DDD identifies the internal register the macro RTL implanted

i.e., (r) ← <B_2>

e.g. LXI rp data,

00 RR0 001	N
<B_2>	N+1
<B_3>	N+2

(RpL) ←—<B_2 >

(RpH) ←— <B_3>

<u>Implied addressing mode</u>:

There are certain instructions that operate on one operand in the ACC and therefore need not specify any address. Many instructions in the logics group like RLC, RRC, RAR, RAL, CMA fall in to the category. All these are one byte instruction .these instruction that specify the address the operand is implied addressing for the other operand.