Lecture-14

W-Z:

When a 3-byte instruction containing 2 byte address is to be executed by the µp, the first byte is the (op-code) which is fetched and then decoded by the decoder. Then two memories read m/c cycles are executed to read the two byte address one in each m/c cycle and placed in W-Z register. During instruction execution, (in next m/c cycle), the add^{r} in W-Z register pair is transferred to the address latch to address memory or I/O for data transfer.

Interrupt Control Section:

Sometimes it is necessary to interrupt the execution of the main program to answer a request from an I/O device. For instance, an I/O device may send an interrupt signal to interrupt control unit to indicate that data is ready for input. The µp temporarily stops what it is doing, inputs the data and then returns to what it was doing.

Serial I/O Control:

Sometimes, I/O devices work with serial data rather than parallel. In this case, the serial data stream from an input device must be converted to 8-bit parallel data before the computer can use it. Likewise the 8-bit data out of a computer must be converted to serial form before a serial output device can use it.

The SID input is where serial data enters the 8085. The SOD output is where the serial data leaves the 8085. Two instructions known as SIM & RIM allow the user to perform the serial parallel conversion needed for serial I/O device.

Timing and control section:

The timing and control section supervise the complete operation of the μP . The on chip clock oscillator which produces the internal clock is a part of this section. The timing and control section also has a state generator to generate 10 different states namely $T_1, T_2, T_3, T_4, T_5, T_6, T_{RESET}, T_{HALI}, T_{wait}, T_{HOLD}$ state generator is a multi mode counter. The next state of the state generator from the present state is decided by the many control signals like READ, HALI, INTR, HOLD etc in each states then section of generator many control signals for executing the instruction fetched.

The operation of the μP is cyclic in natural. During the normal operation from the ward Go, μP sequentially and executes one instruction after another until a HALT instruction is executed. The fetching and execution of a single instruction constitutes an instruction cycle. The instruction cycle consists of one or more read or write operation to memory or an I/O device each memory I/O reference requires a mechanic cycle. In other words every time a byte of data is more from CPU to I/O or memory or from memory I/O to cpu , a machine cycle is required.

There are seven different kinds of m/c cycles in the 8085 A:

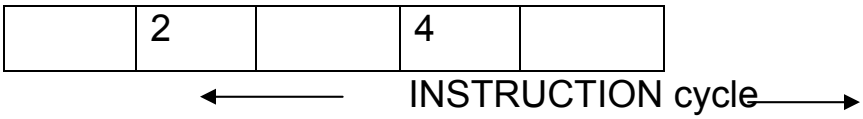
1. OPCODE FETCH
2. MEMORY READ
3. MEMORY WRITE
4. I/O READ
5. I/O WRITE
6. INTEROPT ACKNOLEDGE
7. BUS IDLE

Three status signals IO/$\overline{M}, S_1, S_0$ generated at the beginning of each m/c cycle (and $\overline{RD}, \overline{WR}, and\ \overline{INTA}$ generated during T_2 state of the M/C cycle) identify each type of the m/c cycle the station signals remain valid for the duration of the cycle. The instruction fetch portion of an instruction cycle requires a machine cycle for each byte of the instruction to be fetched since instruction consist of 1 to 8 bytes (1,2 or 3), the instruction fetch Is one to three machine cycles in duration.

The first m/c cycle in an instruction cycle is always an OPCODE fetch m/c cycle which is always single by long and the 8 bits obtained during an OPCODE FETCH are always interpreted as an OPCODE of an instruction. Note that to fetch an instruction is to transfer an entire instruction from memory to the μP necessitates an OPCODE FETCH m/c cycle. However, one or two memory read m/c cycles are also needed to complete the fetch for 2&3 byte instruction respectively.

The number of m/c cycles required to execute the instruction depends on the particular instruction. Some instruction require no addition m/c cycles after the instruction fetch is complete, other requires additional m/c cycles to write or read data to or from memory or I/O devices from one to five. Around 50% of the instruction requires only one m/c cycle for fetching and executing the instruction, no instruction requires more than five m/c cycles M/C cycles like the memory read or memory write may occur more than once a single instruction cycle.

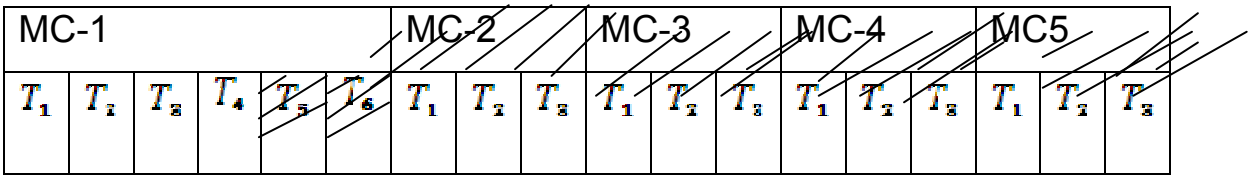
MC-1	MC-	MC-3	MC-	MC-5



The shaded area may be required for executing the instruction. The timing and control unit of μP automatically generates the proper m/c cycles required for an instruction cycle from information provided by the op-code.

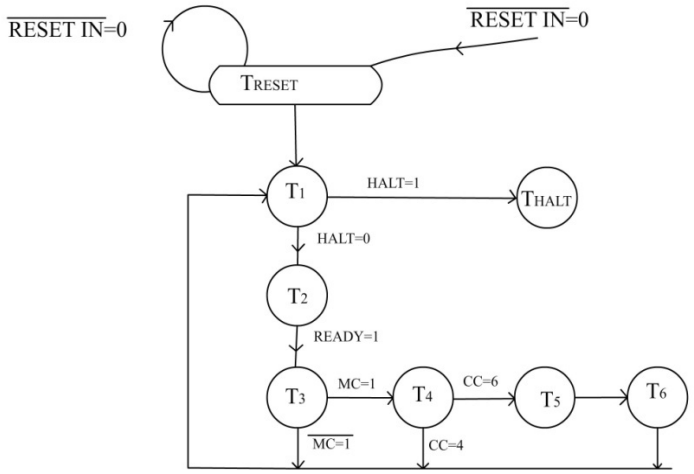
Each m/c cycle contains a number of 320ns clock periods when cryptal used is 6.25MHz. One clock period, i.e. the period between two negative going transitions of that clock is called T state. The various T-states are $T_1, T_2, T_3, T_4, T_5, \& T_6$. Most of the m/c cycles have 3 T states each (T_1, T_2, T_3) only OPCODE FETCH MC has either 4 or 6 states depending on the instruction. The first 3rd states of the mc are identical to a MRMC, the additional T states in OFMC are the T states required by the 8085 A to decode the op code and decide what actions are needed in succeeding MCS.

The combined MCS along with T-states are shown in fig.



MC-i (i=2,3,4,5)

Thus one complete transition from state T_1 through the state diagram and back to T_1 constitutes a complete m/c cycle the partial state transition diagram is shown below assuming READY=1 is no wait.



The shaded portion above that these state may be neede in same instructions. Instruction cycles for various 8085A instruction required to execute an instruction will depend on the READY & HOLD signal inputs.

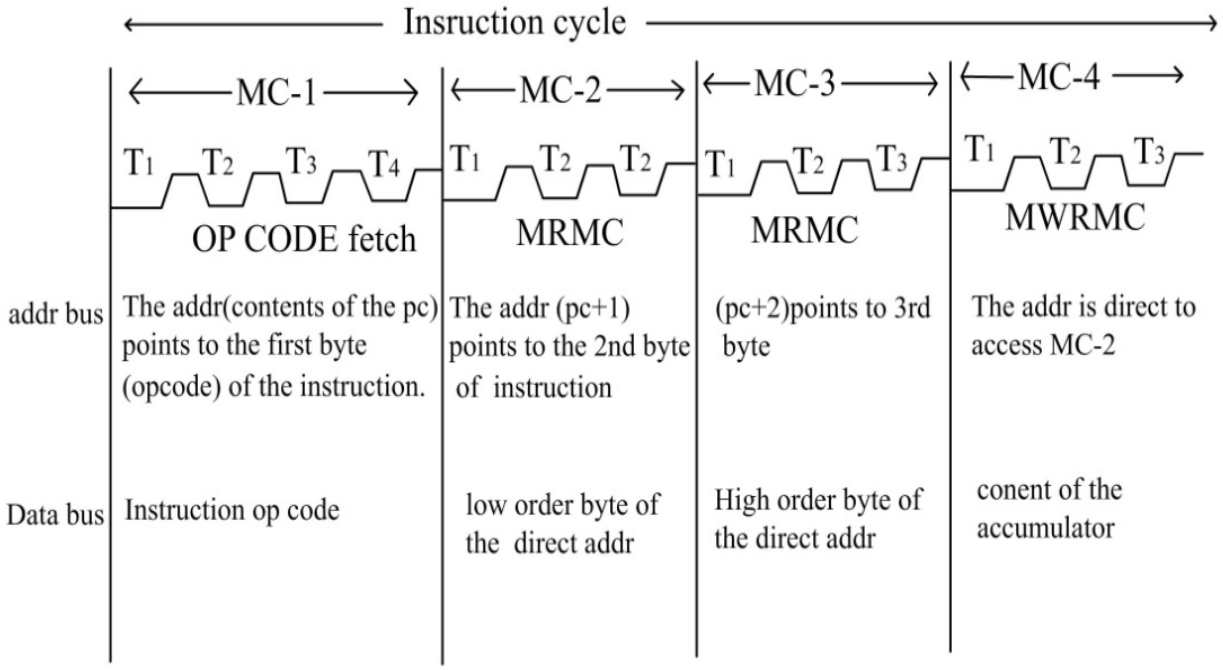
For example consider the 3 byte instruction STA ADDR, STA stands for store accumulator direct the meaning of the instruction is transfer the content of the accumulator to an external memory location whose address is specified in the instruction is ADDR since. The location can be anywhere in the 64k memory space that the 8085A can directly address, 16k are required for the address thus the STA instruction contain 8bytes; a 1 byte op-code and 2-byte address. The instruction is stored in the memory as follows.

OP CODE	BYTE 1
LOWER ADDR	2
HIGHER ADDR	3

Three m/c cycles are required o fetch this

instruction. In MC-1 is op code fetch M/C ,the opcode is transferred from memory to the instruction register during T_1-T_3 states and then during T_4 state it is interpreted , at this point the cpu knows that it must do more m/c cycles two RMC to fetch the complete instruction in MC-2 the lower addresses transferred from the memory to the temporary register Z. in MC-3 the third byte i.e. the higher address is transferred from the memory to the temporary register W. when the entire instruction is in the μP it is executed. Execution means a data transfer from the μP to memory. The contents of the accumulators are transferred to the memory location, whose address was previously transferred to the μP by the proceeding two memory read m/c cycles the address of the memory location to be written is generated as follows the high order address byte is temp reg. W is transferred to the address latch and the low order address byte in Z reg. is transferred to address/data latch. The content of the A is then placed on the data bus. This data transfer is affected by a MWRMC thus 3 byte STA instruction has four m/c cycles in its instruction cycles.

Mnemonic	Instruction byte	
STA	op code	OP CODE
FETCH		
	LO addr	MRMC
	Hi addr	MRMC
		MWRMC



This STA has a total of 13 states. If the 8085A is operating at 325.5ns time, the STA instruction cycle is executed in 4.23 μs . This time period is the instruction execution time, although it actually includes both the instruction fetch and the execution time.