Lecture-28

UNSPECIFIED OP CODES OF THE 8085A

Examine the instruction set of 8085a, one finds that out of the 256 possible opcode with 2 bits, Intel announces only 246, there are no announced instruction corresponding to the 10 missing opcode. User have since reported that these missing opcode. The flags specified by Intel are S, Z, AC, P, CY located in the flag register as

S	Z	X	AC	X	P	X	CY

Users have reported that there are two more flag bits having same useful meaning.

S	Z	X_5	AC	X	P	V	CY

V = overflow bit. This bit is set to 1 of overflow occurs in 2's complement addition / subtraction/ DCX/INX for8 and 16- arithmetic operation.

X_5 their bit has been named for its position in the condition code byte 2t does not resemble any normal flag bat this bit is affected as per the following expression.

$X_5 = S_1.S_2 + SI.R + SL.R$

Where, S_1= sign of operand 1

S_2= sign of operand 2

R= sign of result.

For subtraction & compression replace S_1 by $\overline{S2}$ where operand 2 the subtraction ie result, operand 1- operand 2. The only use for the bit termed are as an unsigned overflow indication resulting from a data change of FFFF to 0000 on executing the instruction INX and as an

unsigned underflow indicator from a data change of 0000 to FFFF an executing DCX.

The ten new instructions, include seven opcode that involve the processing of register pairs, the involve jump operation with X_5 flag bit are that perform a conditional flag bit V.

The various instructions are

1) DSUB: (double subtraction): the macro RTL implements is

(H, L) ← (H, L) — (B, C)

This is a single byte instruction. The opcode is $(OB)_H$. the meaning of the instruction is the content of reg. pain BC are subtracted foam the content of reg. pain (HL) and result placed back in reg pain (H,L). all seven condition flag are affected.

It requires 3 m/c cycles and 10 states like DAD instruction. The addressing mode is register addressing mode.

2) ARHL: (arithmetic right shift HL reg) the macro RTL implemented is

$H_7 \leftarrow (H_7)$, $H_{n-1} \leftarrow H_n$,

$L_7 \leftarrow H_0$, $L_{n-1} \leftarrow L_n$, $CY \leftarrow L_0$

This is a single byte construction the opcode is $(10)_H$. the meaning of the instruction is the contents of register pair (HL) are shifted right by one bit. The upper most bit is duplicated and the lower bit is shifted into the carry bit. The result is placed back into the (H, L) reg. pair only ax flag is affected It requires 2 m/c cycles and 7 statues the addressing mode is register address mode.

3) RDEL: (Rotate D.E reg. pair left through carry) the macro RTL implements

$CY \leftarrow D_{7,} D_{n+1} \leftarrow D_E ,$

$D_0 \leftarrow E_7 , E_{n+1} \leftarrow E_n , E_0 \leftarrow CY.$

This is a single byte instruction. The operation code is 18_4. The meaning of the instruction is the content of repair DE is rotated left by one b through the carry flag. The low order but is set equal to the CY flag and the CY flag is set to the value shifted out of the V flag bits are affected. The result is placed book into the DE register pair. It requires 3m/c cycle and 10 states. The addressing mode is register addressing mode.

4) LDHI: (Lead D, E reg pair with (H, L) flow immediate data). The macro RTL implements is (D,E) $\leftarrow$ (H,L)+<B_2>

This is a 2 byte instruction the operation code format is

28	N
<B_2>	N+1

The meaning of the instruction in the contain of register pair (H, L) are added to the immediate byte. The result is placed in register pair (D, E) no condition flags are affected.

It requires three m/c cycles and 10 states. The addressing mode is immediate & register addressing mode the second byte is called offset.

5) LDSI: (Load (D, E) reg pain with SP flow immediately byte). The macro RTL implements is

(D.E) $\leftarrow$ (BP) + <B_2>

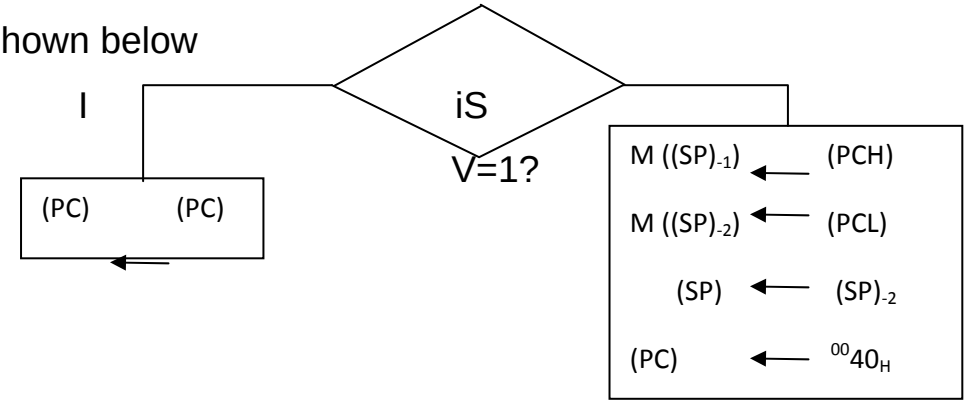
This is a byte instruction the opcode format is

3S	N
<B_2>	N+1

The meaning of the instruction is the content of register pair SP are added to the immediate byte & the results is placed in register pair (D,E). No condition flag are affected.

It requires 3m/c cycle and 10 states. The addressing mode is immediate register addressing mode.

6) RSTV (Restart in overflow). The macro RTL implements is shown below



This is a single byte instruction. The opcode is $(CS)_H$. the meaning is the overflow flag V is set, the actions specified above are performed, otherwise control continues sequentially.

It requires 1 or 3 m/c cycles and 6 or 12 states. The addressing mode is register indirect addressing mode none flags are affected.

7) SHLX: (Store H,L indirect through D,E) the macro RTL implemented is

M ((D,E)) ⟵ (L)

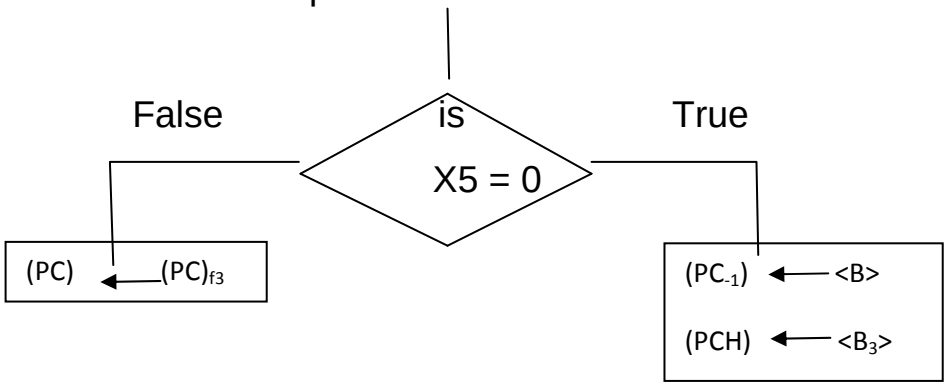
M ((DE)+1) ⟵ (H)

This is a single byte instruction. The opcode is $(D9)_H$. the meaning is the content of register L are moved to the memory location whose addressing register DE. The contents of register are moved to the succeeding memory location.

It requires 3m/c cycles and 10 states. The addressing mode is reg indirect addressing mode is reg indirect addressing mode. None flags are affected.

8) JNX5: (Jump on not X5)

The macro RTL implemented is shown below:



Where (PC) is the address for opcode.

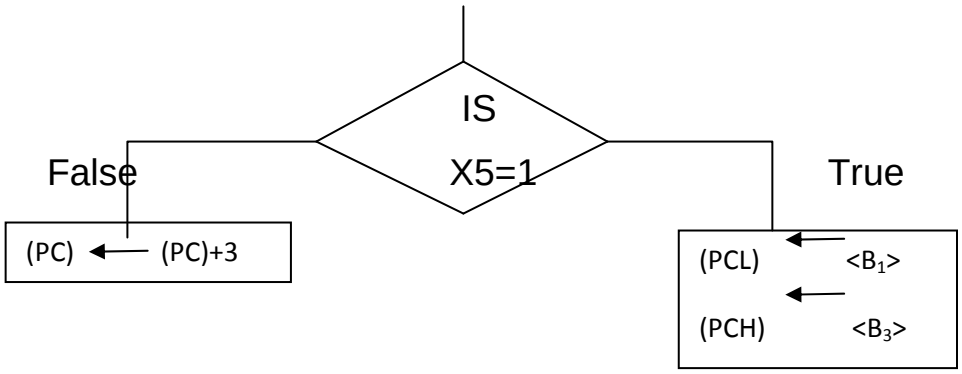
This is an S byte instruction. The operation code format is

DD	N
$<B_2>$	N+1
$<B_3>$	N=2

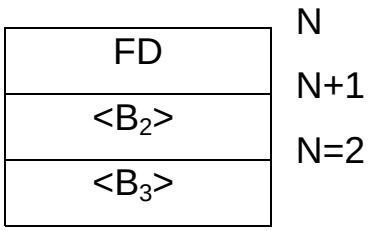
This instruction tests the X_5 bit, if the X_5 bit is '0', the control is transferred to the instruction whose address is specified in byte 2 &

byte 3 of the current instruction, otherwise control continues sequentially. It requires 2 or 3 machine cycle of 7 to 10 states. The addressing mode is immediate mode. None flag are affected.

9) JX5: (Jump on X_5): the macro RTL implemented is shown below.



This is an 8 byte instruction. The operation code formats.



This instruction test X_5 bit if X_5 bit is set, the control is transferred to the instruction whose address is specified in byte 3&2 of the current instruction otherwise the control continues sequentially. It requires 2or 3 m/c cycles and 7 or 10 states. The addressing mode is immediate none flags are affected.

10) LLX: (Load H,L indirect through DE)

The macro RTL implemented is (DE)

(L) ← M (D, E)

(H) ← M ((D, E) +1)

This is a single byte instruction. The operation code is ED_H. The meaning is the content of the memory location whose address is in (DE) reg. pair are moved to register L, & the content of the succeeding memory location are moved to register H. it requires 3m/c cycles and 10 states. The addressing mode is register indirect none flags are affected.