Lecture-10

READY at PIN NO 35→

this is a control signal input. There are many peripheral devices which are slow in operation can be to the μp speed eg. The occurs time of a memory interfaced with a μp may be much larger than the clock period of the μp. Thus is a need for telling the μp that the device so addressed by the μp is not ready for data transfer operation. The device, selected should have the ability to generate a control signal output READY which shall be LOW of the device is not ready for data transfer operation and goes HIGH when the device is READY for data transfer operation.

This idea is summarized in fig-4 considering memory as the external device.

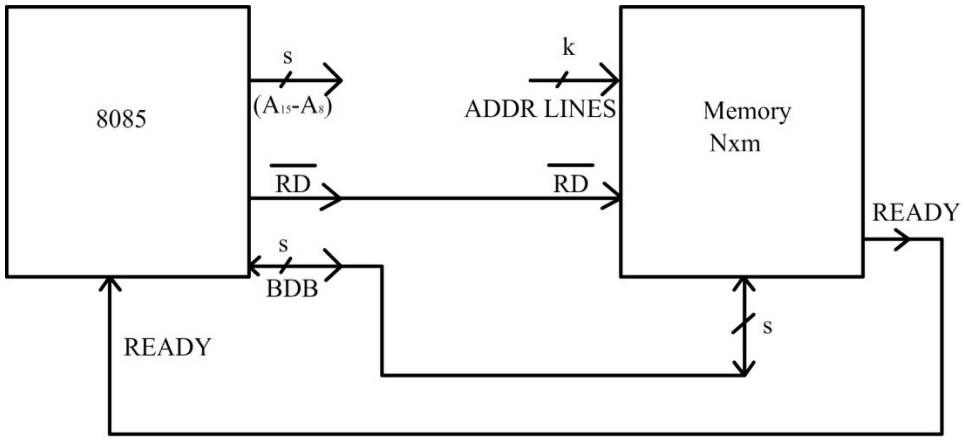

Fig - 4

The μp sent the address during T_1 state of the μp to address the memory and then issues appropriate RD or WR signal during T_2

state either to read the memory or write into the memory Having issued the appropriate $\overline{RD}$ or $\overline{WR}$ signal during T_2 states the μp monitors. READY control signal input if the READY control signal input LOW the μp knows that the device addressed is not ready for data transfer operation and therefore goes to WAIT state (TW). Once in WAIT state, the μp does not do any other work except monitoring control signal as long as READY signal is LOW, μp remains in WAIT state when the READY signal goes HIGH μp realized that the device addressed is ready for data transfer operation and comes out of the WAIT state and goes into T_3 state. The partial state dig describing the above process is shown in fig.5.

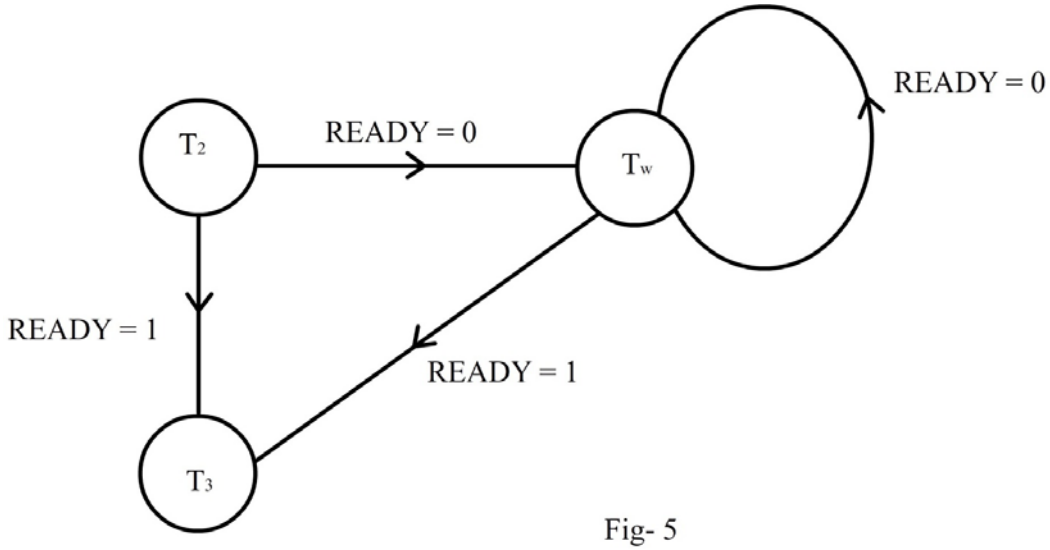

Fig- 5

The appropriate control signal output $\overline{WR}$ or $\overline{RD}$ shall remain LOW throughout the TW state and goes HIGH when the μp comes out of the WAIT state and goes to T_3 state the corresponding timing signals are shown below. In fig-6.

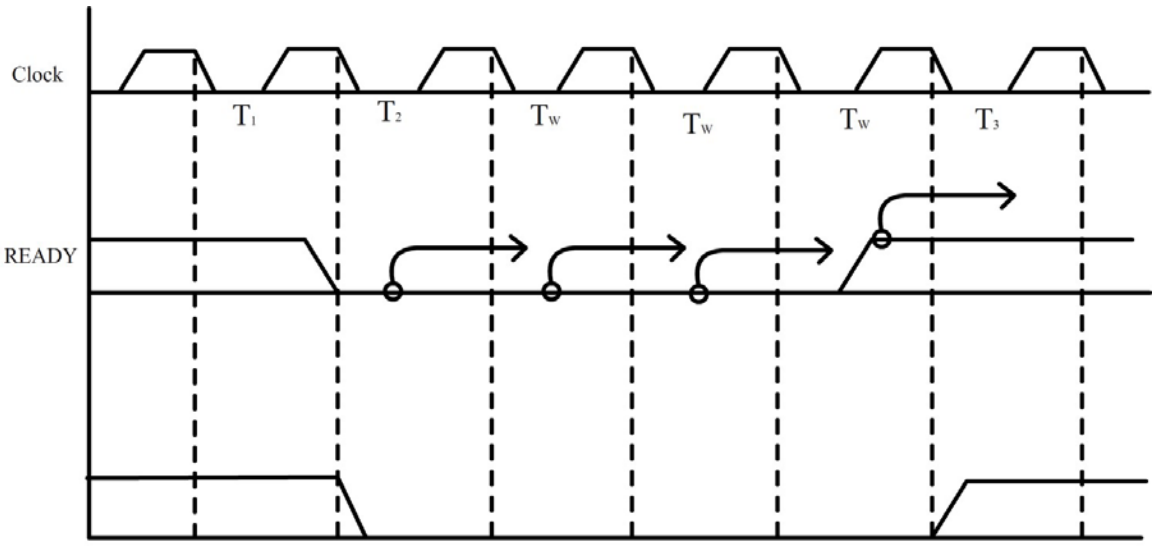

Fig-6 ($\overline{RD}$ shown READ operation assume)

RESET IN at pin no.36 →

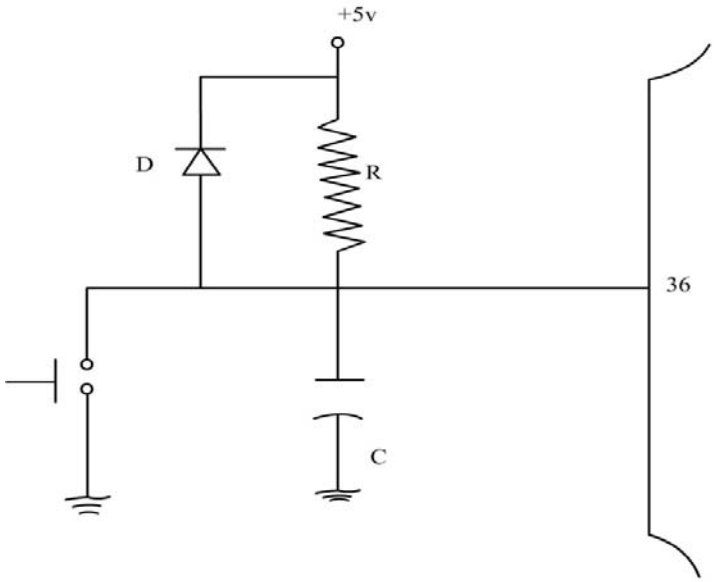

Fig- 7

It is an input control signal normally HIGH and active LOW. It is used to RESET the μp to its initial state. The initial state of the μp shall be described later. During power ON the μp must be RESET. The necessary circutary for resetting the μp is shown in fig-7. Initially the

capacitor is discharged therefore to start with when the power is first ON, $\overline{RESET\ IN}$ control signal is LOW. Therefore the μp will be RESET to its initial state. Depending upon the time constant RC the voltage across the capacitor experientially increases to 5 volts. When the voltage across the capacitor reaches to 2.4 volts,$\overline{RESET\ IN}$ control signal goes to logical '1'. μp Comes out of the RESET state and straight away goes to T_1 state. The time duration to reach around 2.4 volts from the instant of switching the supply is around 4 to 5 CLK cycles. If this duration is not maintain the resetting action of the μp is not guaranteed and therefore, RC combination should be selected accordingly.

The diode D in fig-7 is to provide for the discharge path for the capacitor charge voltage. Whenever the power supply is finally put OFF the push bottom switch provided in fig-7 can be used to RESET the μp to its initial state as and when necessary during the functioning of the μp. The partial state diagram when $\overline{RESET\ 1}$ Control signal is active is shown-in fig -8

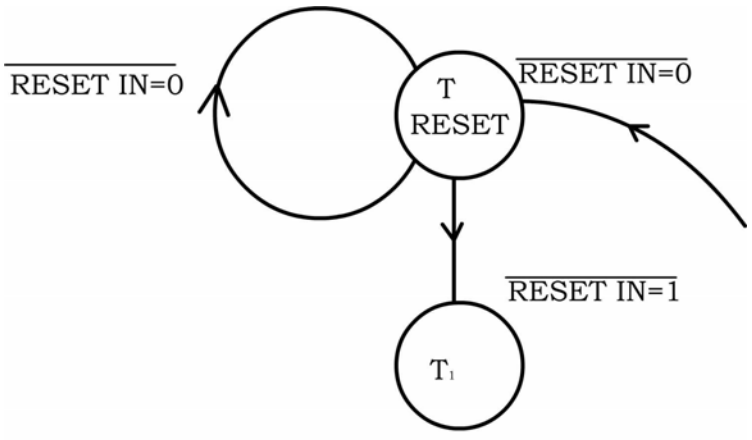

Fig-8

RESET OUT at PIN NO 3 → It is normally LOW, when RESET IN control signal is HIGH. Reset out goes active HIGH as long as RESET IN is active LOW. This RESET OUT control signal is provided for the user to use it RESET all the peripheral devices to their initial states.

It is normally low signal output. It indicates 8085 A is being RESET. When RESET IN control signal is low, RESET OUT goes HIGH. It remains HIGH as long as RESET IN is active and LOW. This output is used to reset other devices used in the microprocessor system. The signal is synchronized with the system CLK and it remains high for an integral no. of clock periods. After the RESET IN goes HIGH, RESET OUT goes LOW, the microprocessor enters in the T_1 state and normal operation begins.

X_1 X_2, terminal at pin no.1& 2 and CLK (OUT) at pin no.37 :

Intel 8085A provi9des on chip crystal oscillator circuit which is shown in fig-9.

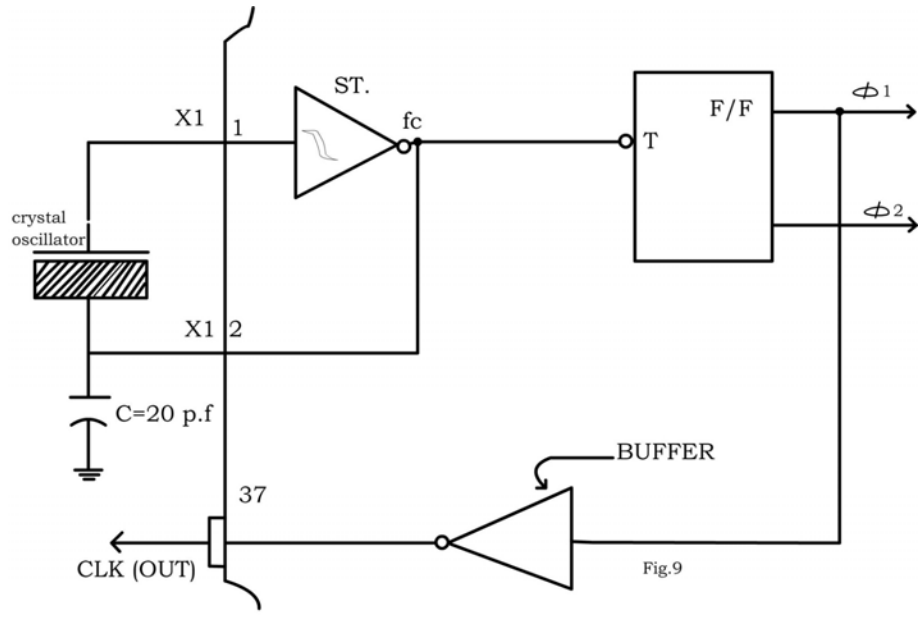

Fig.9

A crystal has to be connected across X_1& X_2 to provide a crystal fq of fc MH_3. Because of the internal T-F/F the operating fq $\emptyset$, clock is fc/2 (half the crystal fq). The $\emptyset$, clock is also buffered and sent out through pin no 37 to the outside world as clock (OUT) signal clock (OUT) signal is used for synchronizing the operation. The data sheet of 8085 puts a lower limit, to the operating fq at 500 kH_3. The max operating fq limit fq for 8085 A-2 is $5MH_3$. Therefore, while using 8085Aμp, a crystal having a +q from $1MH_3$ up to 6.25 MH_3 can be used; 10MH3 crystal has to be used for 8085A-2 μp. The 20pf capacitor on fig-9 is necessary between X_2 and ground if the crystal fq is less than 4 MH_3 to provide for proper oscillation. It is not necessary for higher gq. The data sheet also mentions 15pf. Sheet capacitors across X_1&X_2 internally.

A crystal is to be used across X_1&X_2 to get stable fq of oscillation if stable fq of oscillation is not necessary in our application, then a L-C network or a R-C network can be used as shown in fig 9(b) & 9 (c).

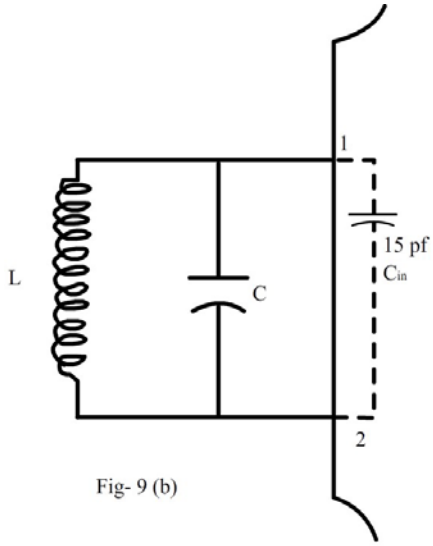

Fig- 9 (b)

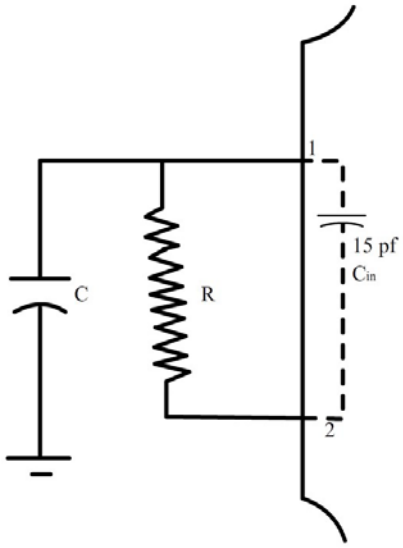

Fig- 9 (c)

The frequency of oscillation of fig 9(b) is given by

$$f=\frac{1}{2\pi\sqrt{L(c_{ext}+c)}}$$

The data sheet recommends as external capacitance of around. If a large variation of fg can be tolerated in our application then fig-9(c) can be used. Fig-9(c) is for $3MH_3$ oscillation. No other fq is recommended using the connection if we have an external clock whose fq is same and can be varied from $1MH_3$ to 6.25 MH_3, then the external clock can be connected as shown in fig-9(d).

If we have an external clock whose frequency is same and can be varied from 1MHz to 6.25 MHz, the external clock may be connected to x_1 and x_2 is left open. If the driving frequency is 8 MHz to 12 MHz, stability of the clock generator will be improved by driving x_1 and x_2 with a push pull force. To prevent self oscillations of the 8085, x_2 should not be coupled back to x_1 through the driving circuit. In last two cases, pull up resistors are required to assure that the high level voltage of the input is at least 4v and maximum low level voltage of 0.8V.

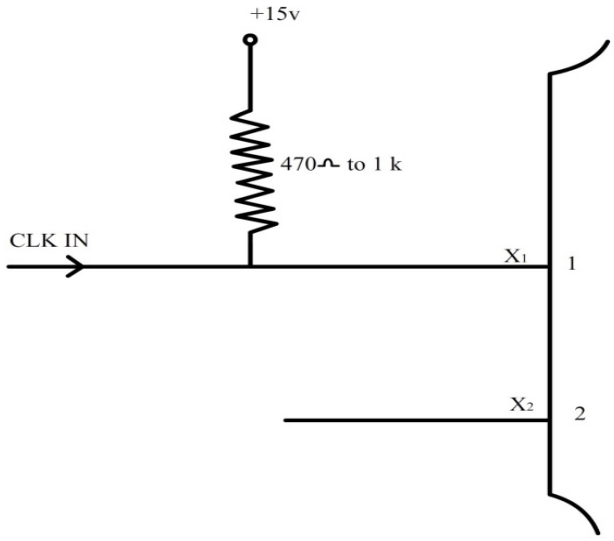

Fig- 9 (d)