EE-309: Microprocessors

SUMMARY

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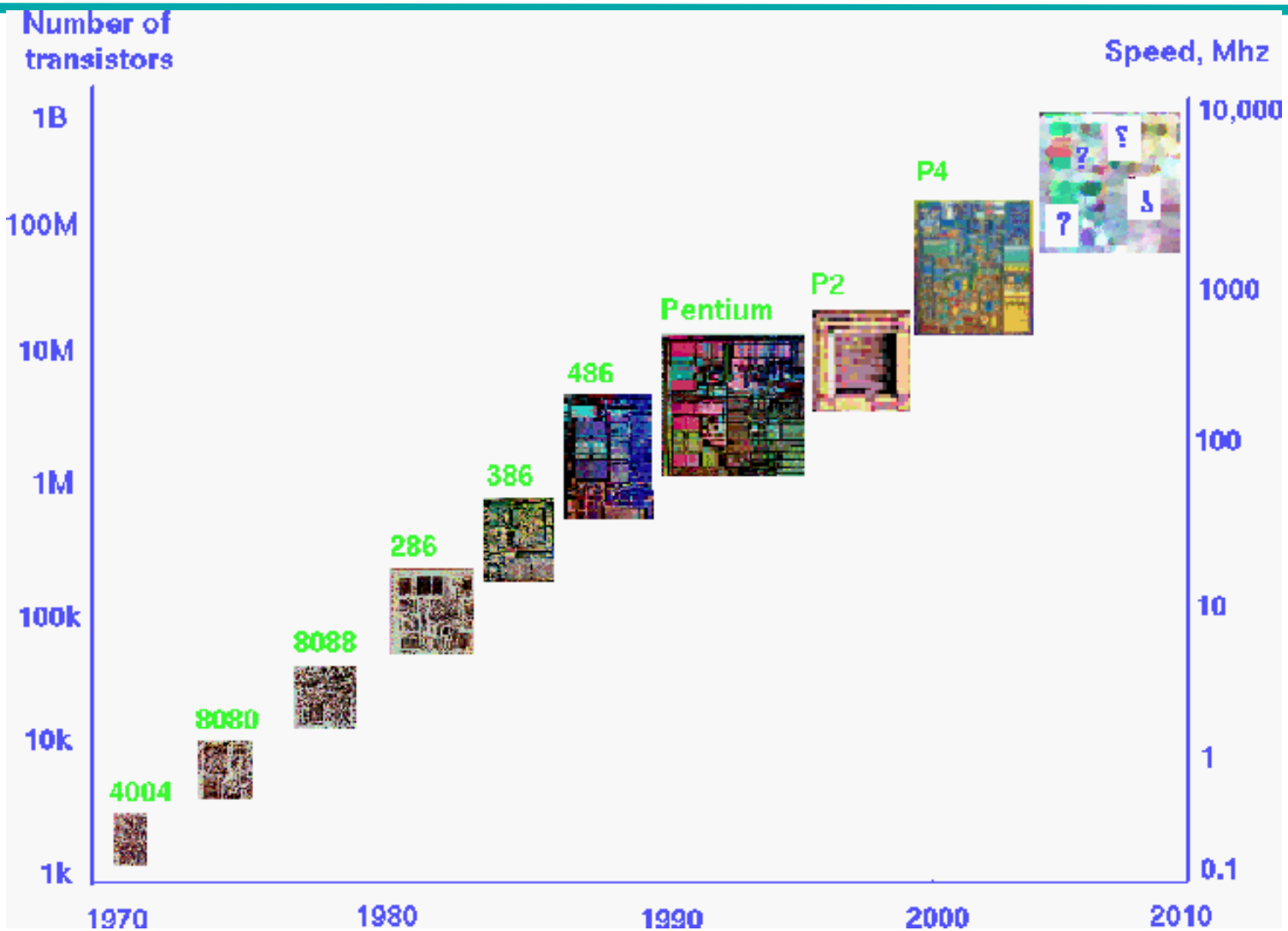
EE-309: Microprocessors

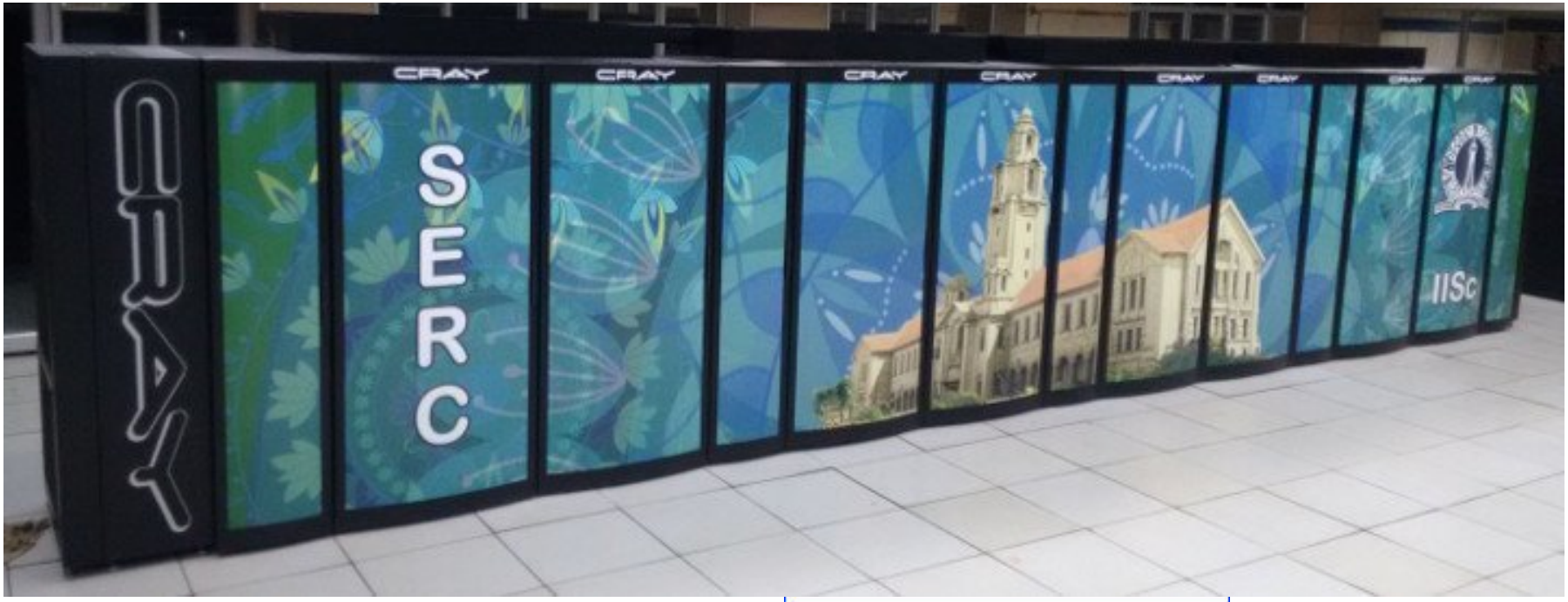
Lecture 43 (05 Nov 2015)

CADSL

Microprocessor Designs



Why Study Microprocessor Design?

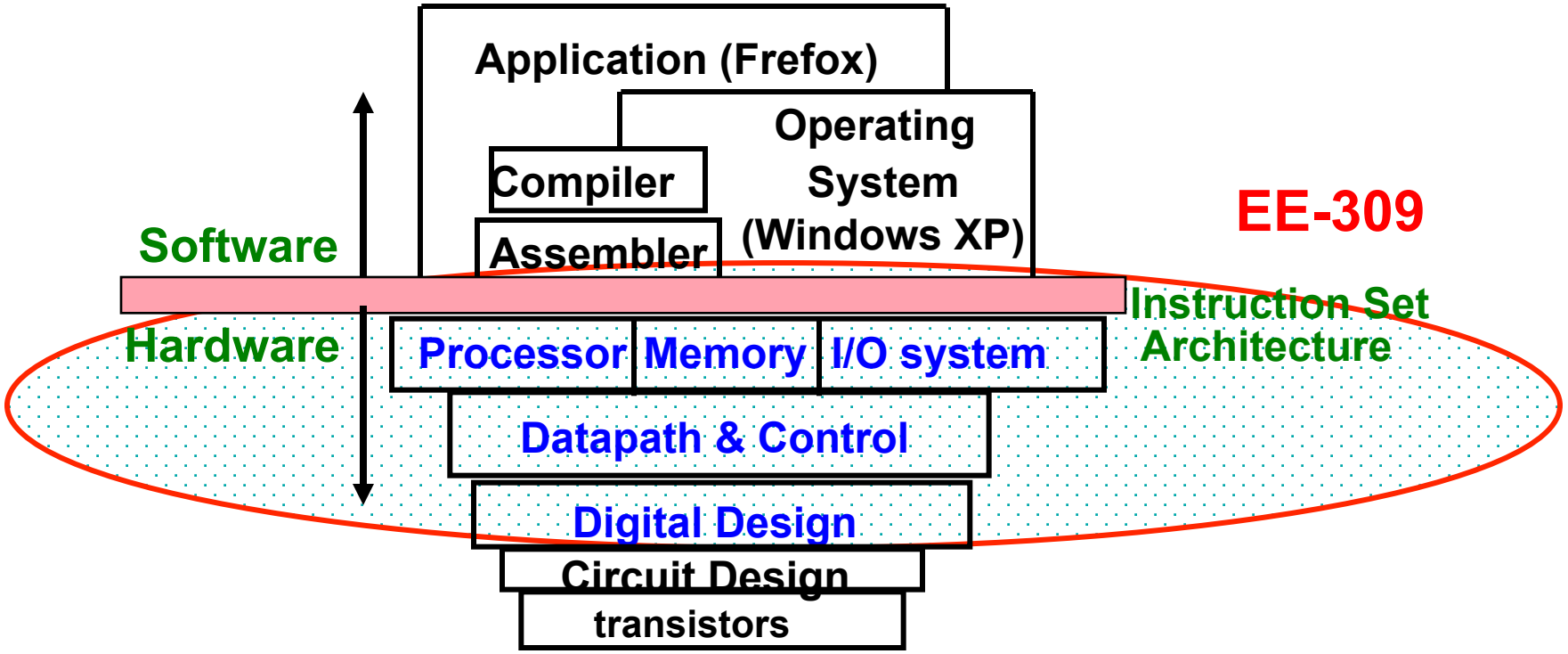


Where are the Embedded Devices?

Computer Technology → Dramatic Change

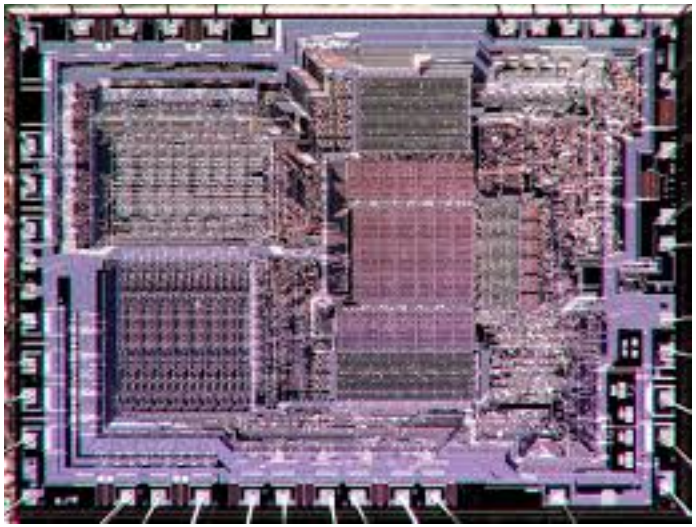
- Processor
  - 2X in speed every 1.5 years;
    100X performance in last decade
- Memory
  - DRAM capacity: 2X / 2 years; 64X size in last decade
  - Cost per bit: improves about 25% per year
- Disk
  - capacity: > 2X in size every 1.0 years
  - Cost per bit: improves about 100% per year
  - 250X size in last decade

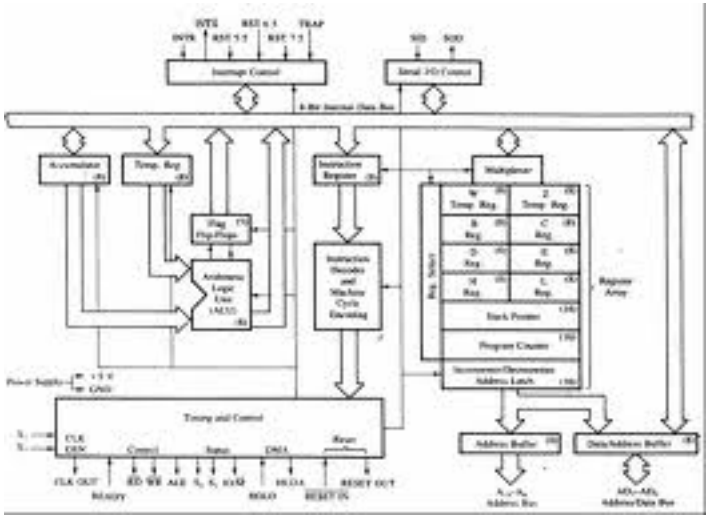
What was this course about?



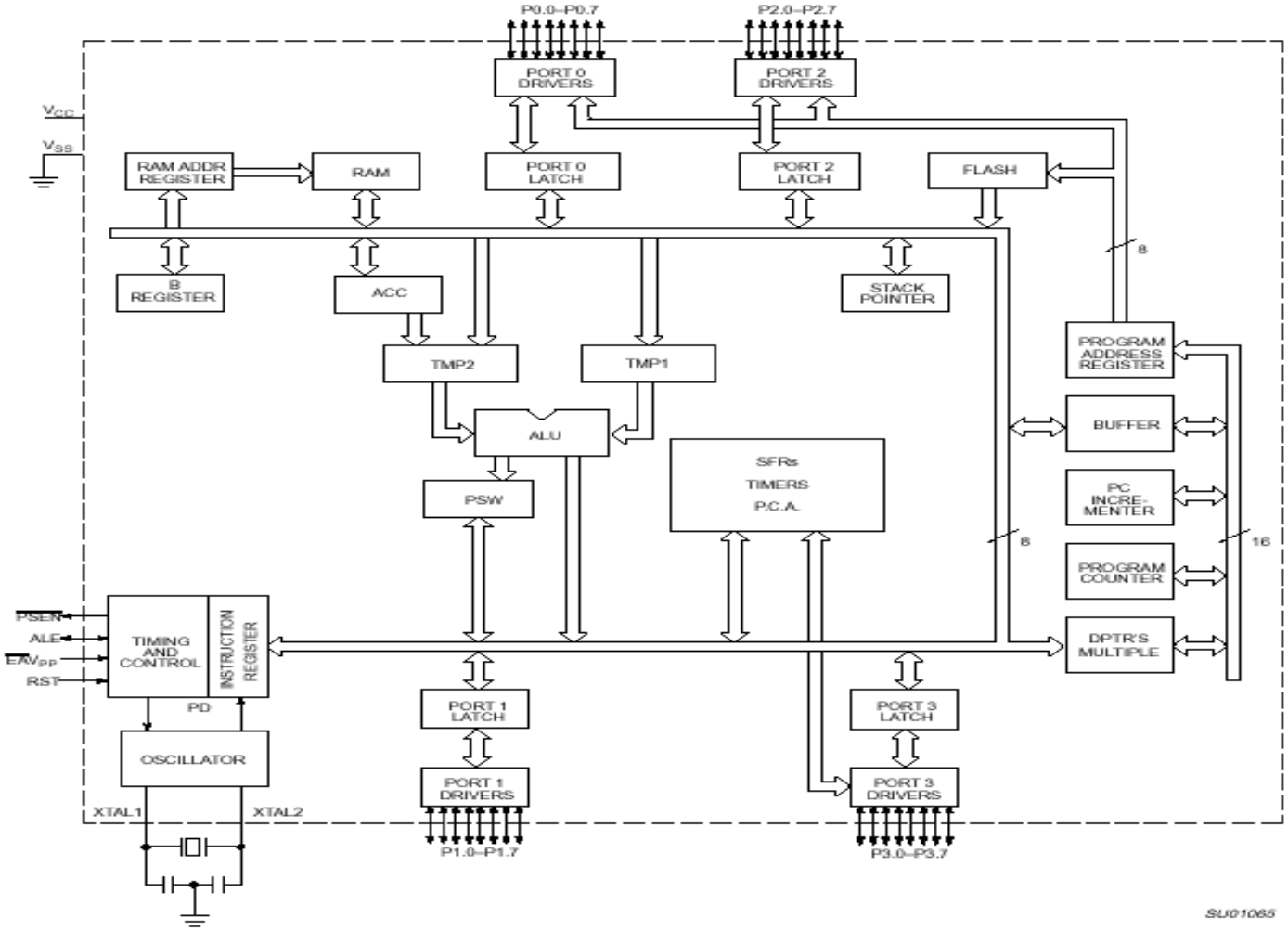
- Coordination of many *levels of abstraction*

Microprocessor: 8085





8051 Internal Block Diagram



Running Program on Processor

$$\text{Processor Performance} = \frac{\text{Time}}{\text{Program}}$$

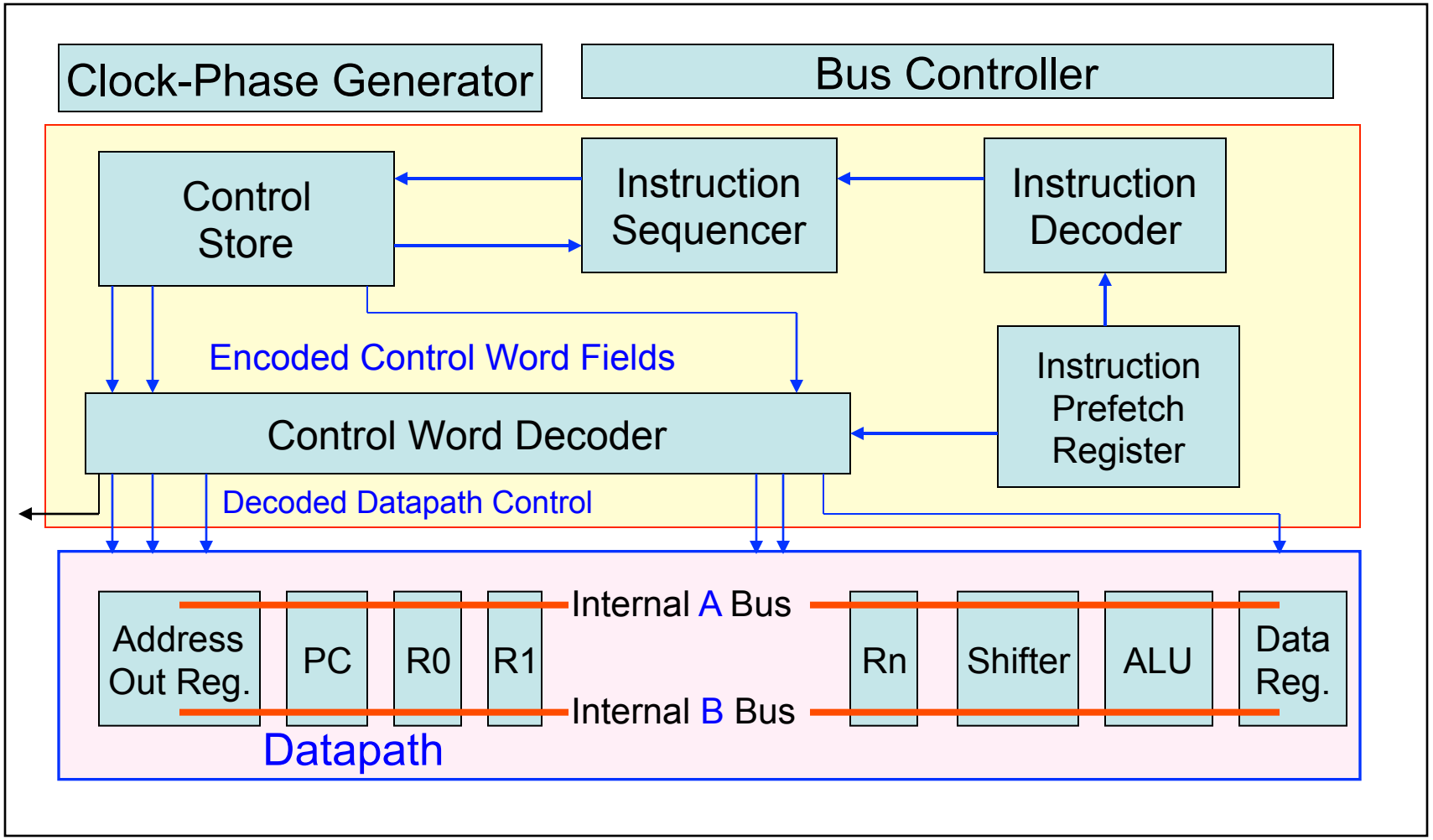
$$= \frac{\text{Instructions}}{\text{Program}} \times \frac{\text{Cycles}}{\text{Instruction}} \times \frac{\text{Time}}{\text{Cycle}}$$

(code size) (CPI) (cycle time)

Architecture --> Implementation --> Realization

Compiler Designer **Processor Designer** **Chip Designer**

Micro-coded Implementation

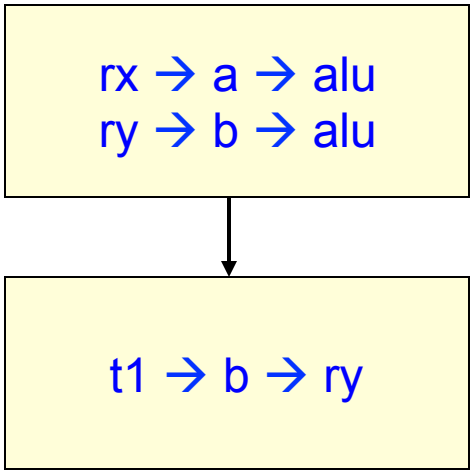


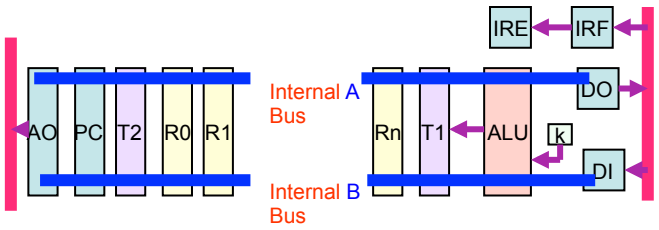
Hardware Flowcharts

ADD RX AR RY

Register-to-Register

R → R ADD

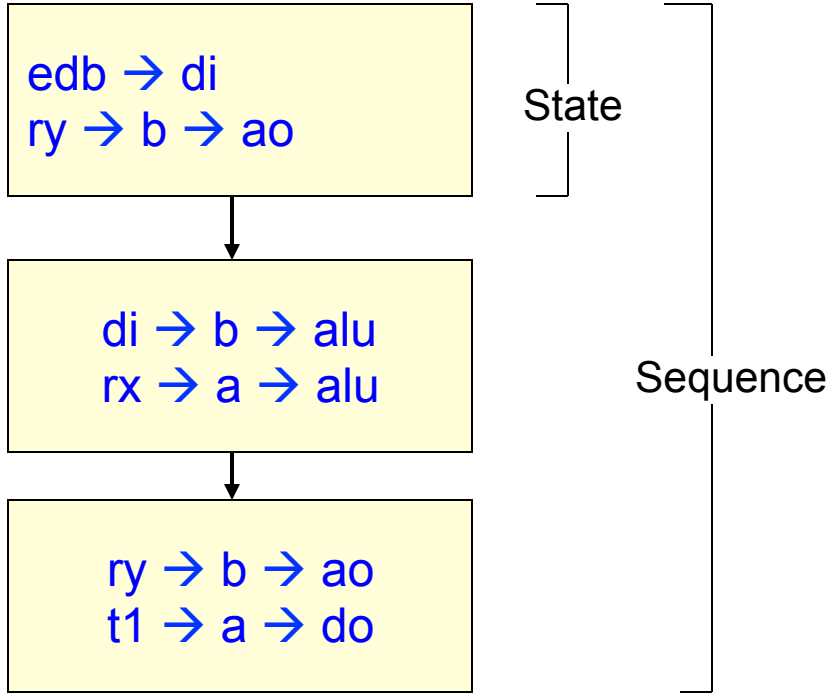


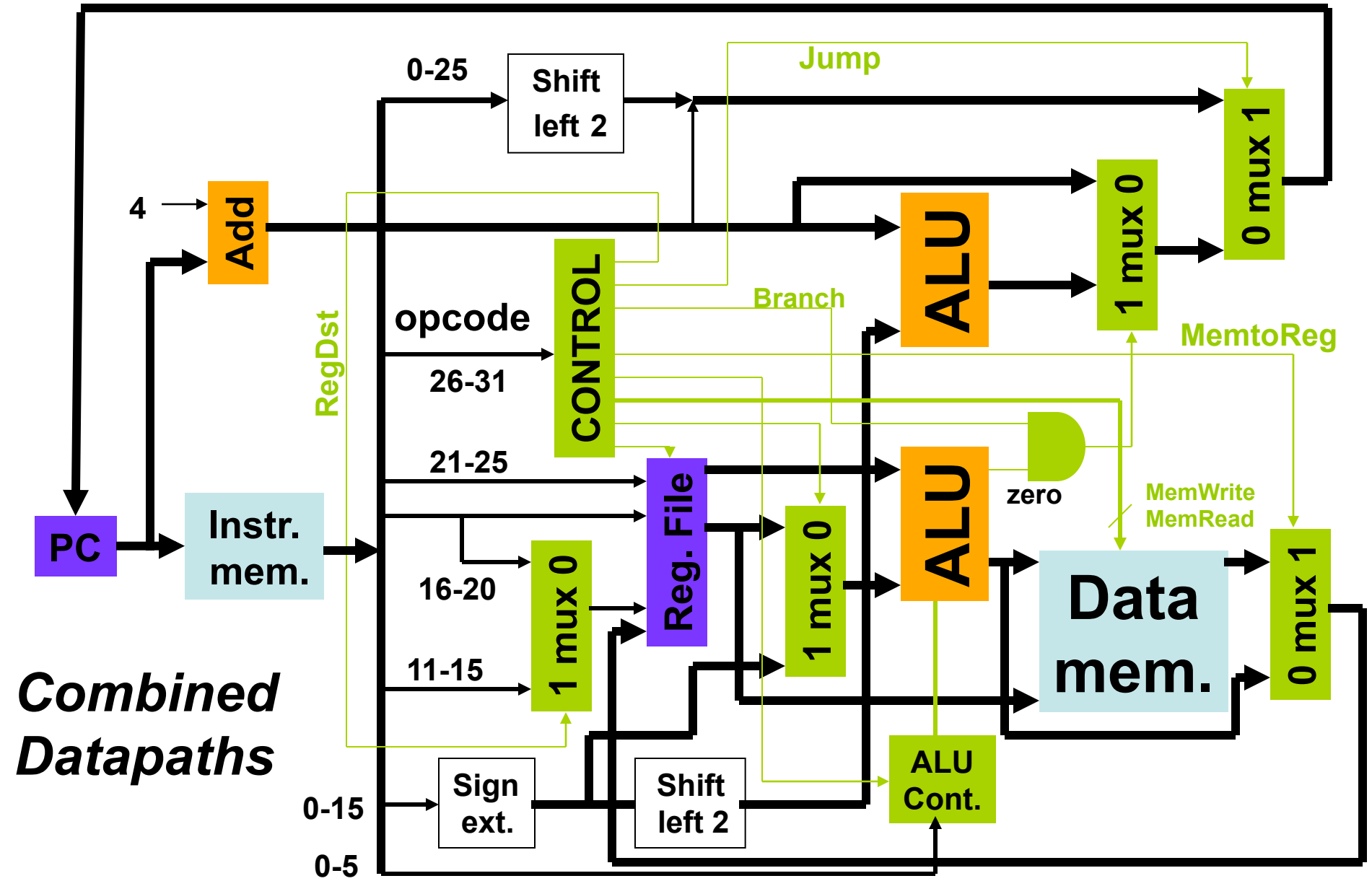


ADD RX AI (RY)

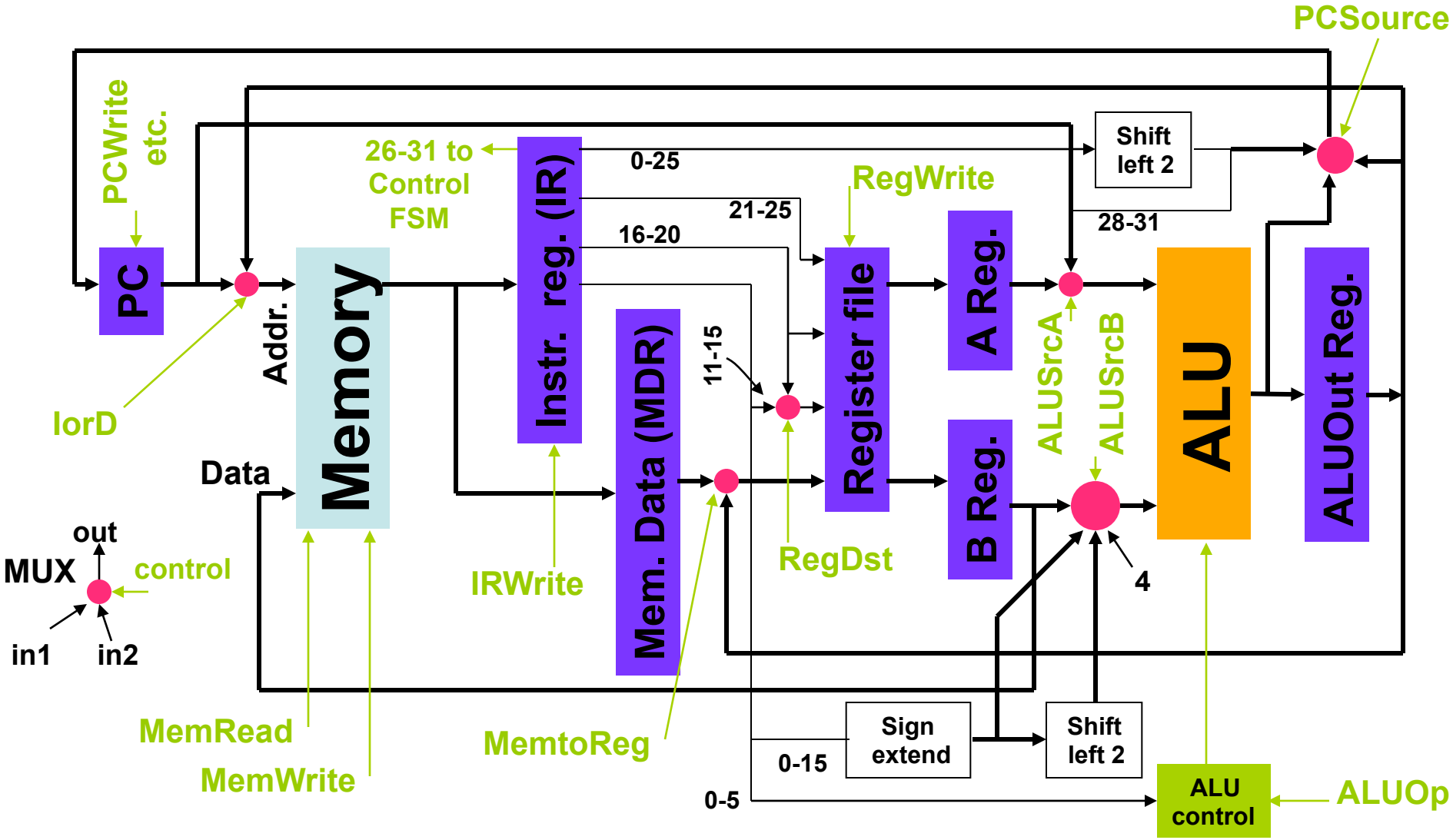
Register-to-Memory

R → M ADD

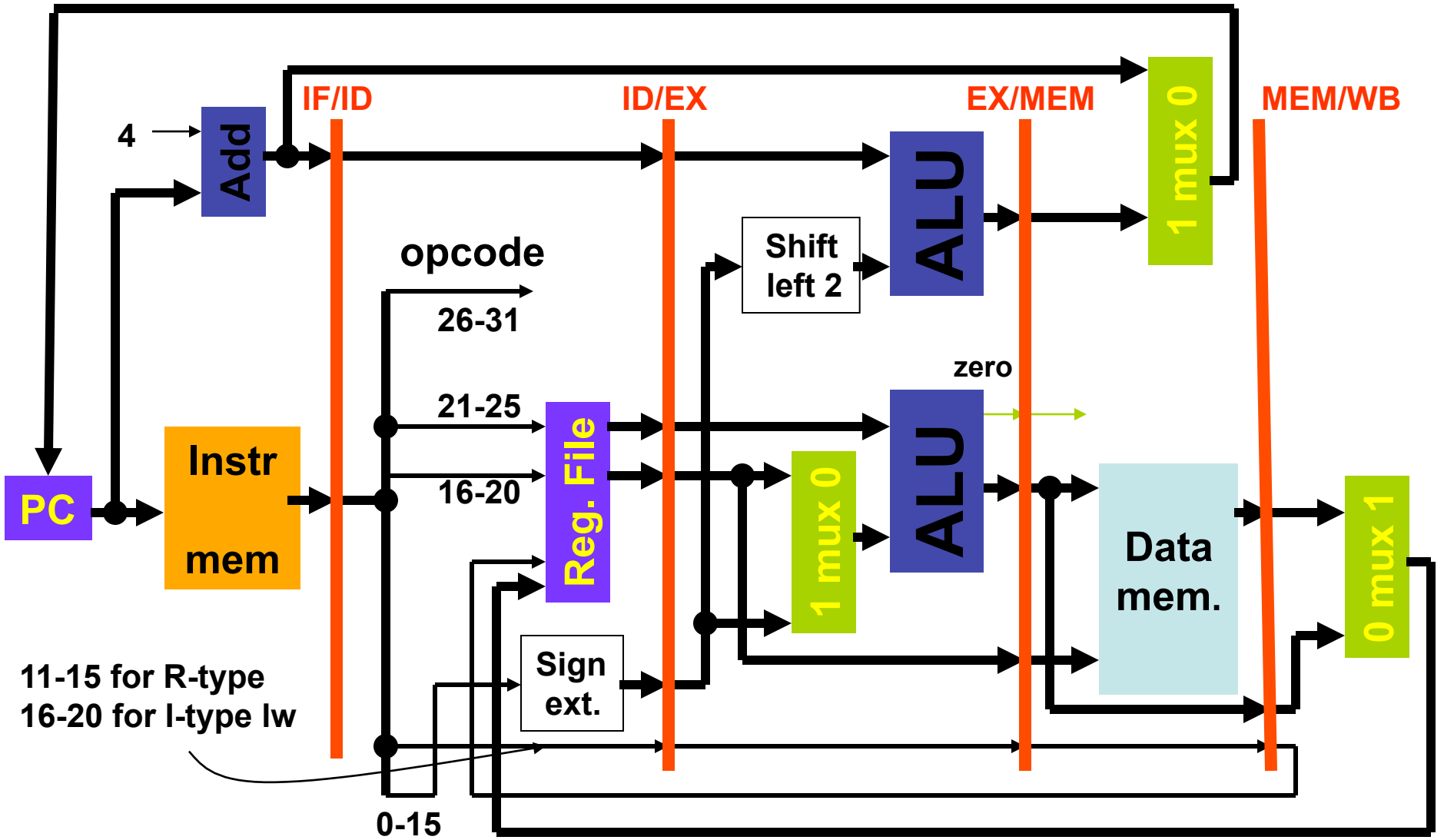



Combined Datapaths
0-25
Shift left 2
Jump
4
Add
ALU
1 mux 0
0 mux 1
RegDst
opcode
26-31
CONTROL
Branch
MemtoReg
21-25
Reg. File
zero
MemWrite
MemRead
PC
Instr. mem.
16-20
1 mux 0
ALU
Data mem.
0 mux 1
11-15
1 mux 0
ALU Cont.
Sign ext.
Shift left 2
0-15
0-5

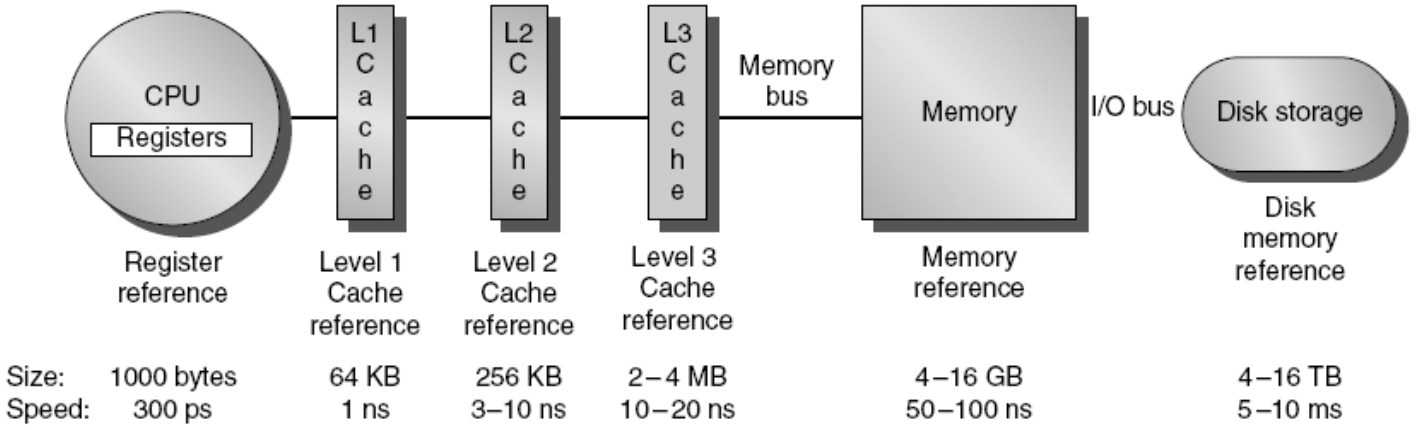
Multicycle Datapath



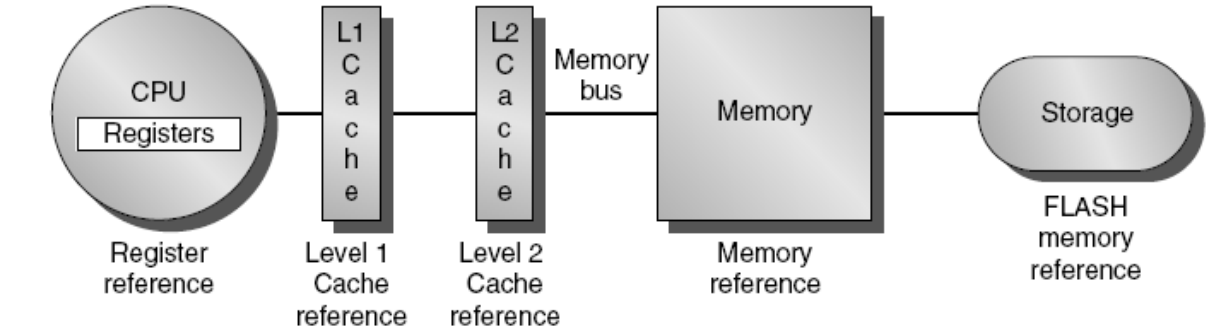
Pipelined Datapath



Memory Hierarchy

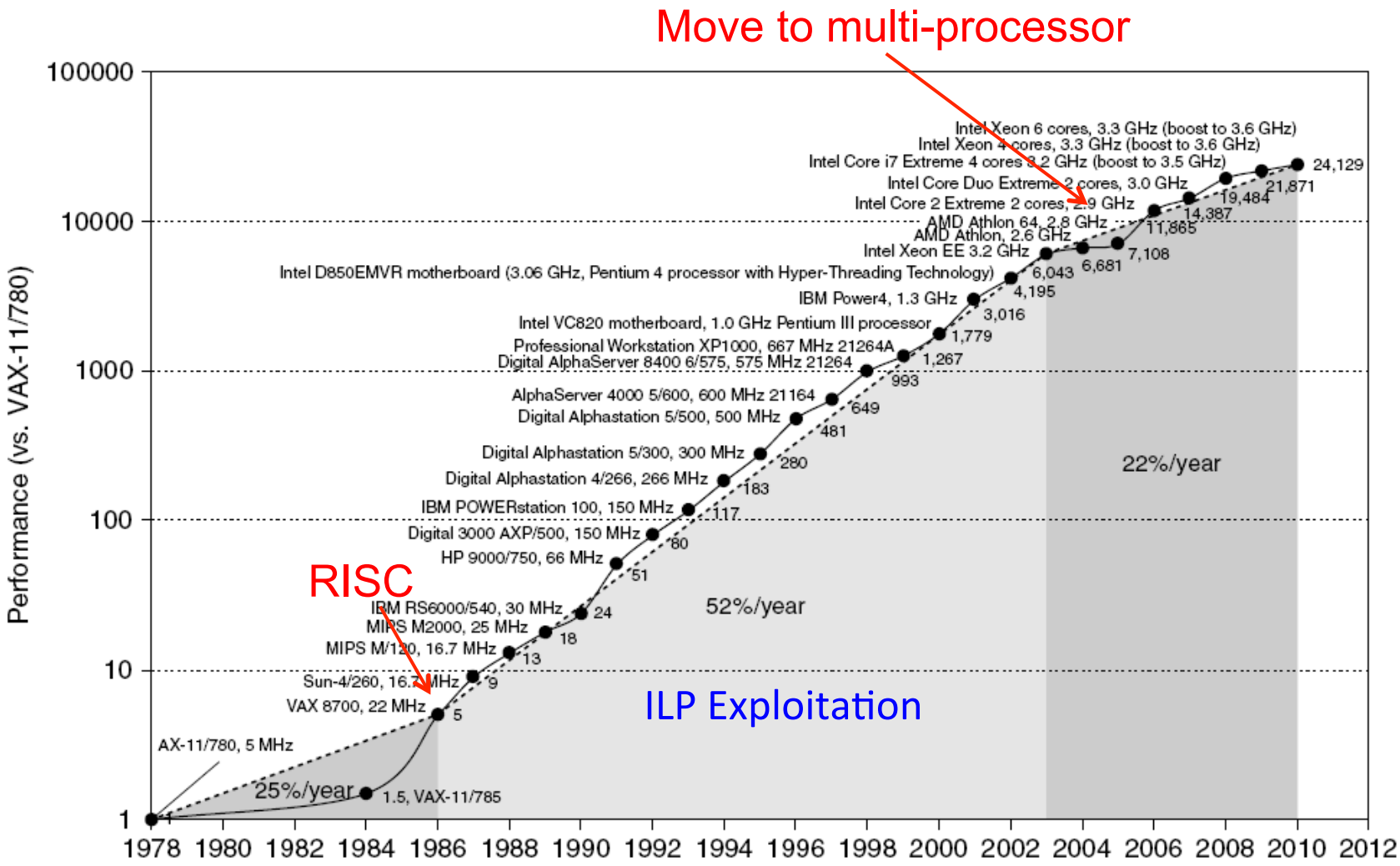


(a) Memory hierarchy for server

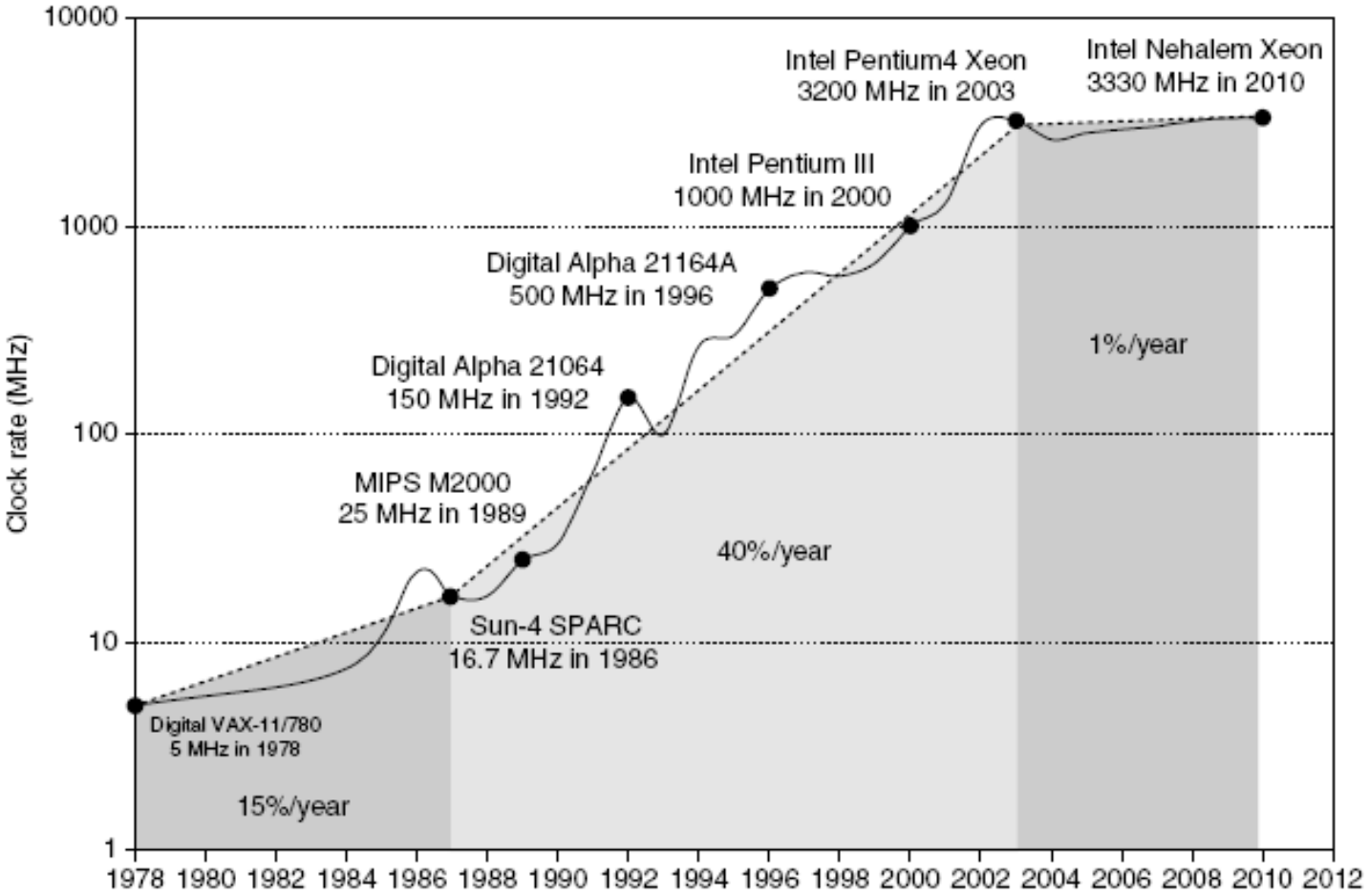


(b) Memory hierarchy for a personal mobile device

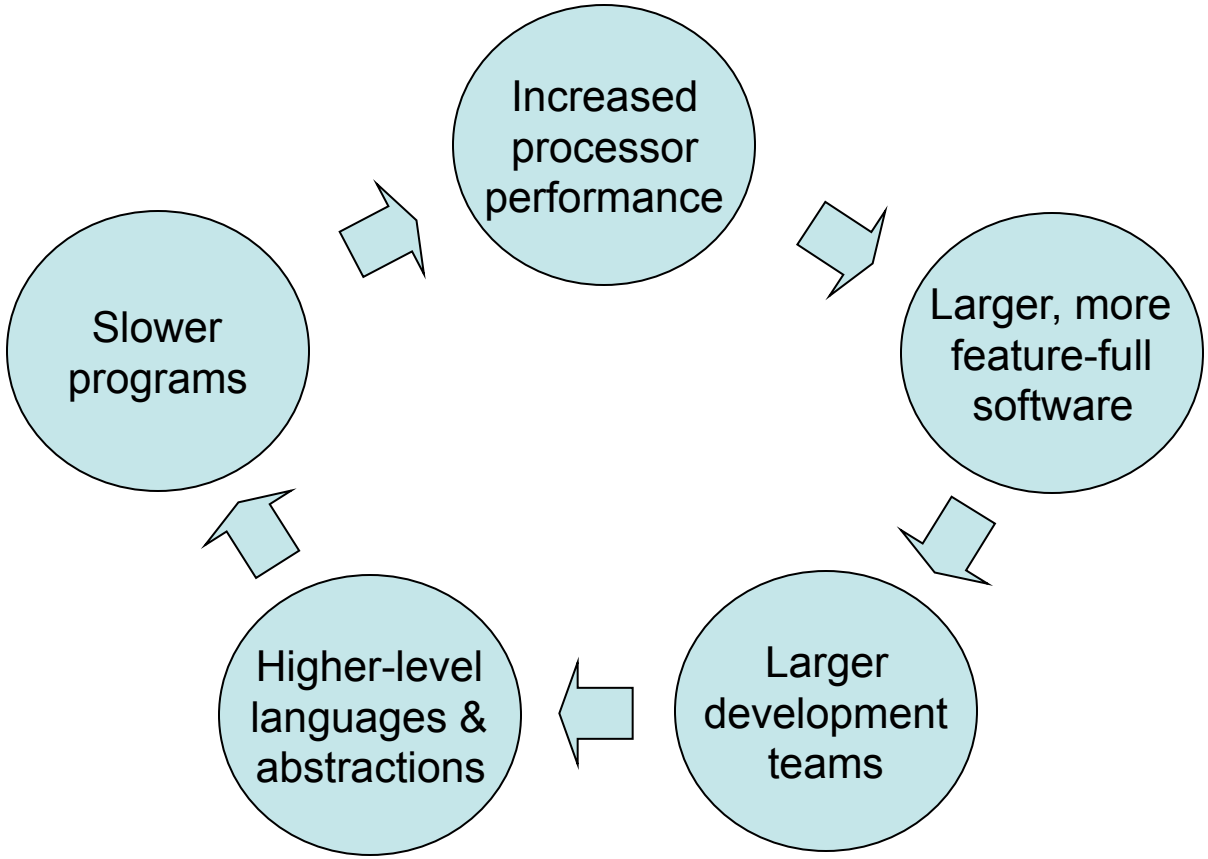
Single Processor Performance



Frequency Scaling



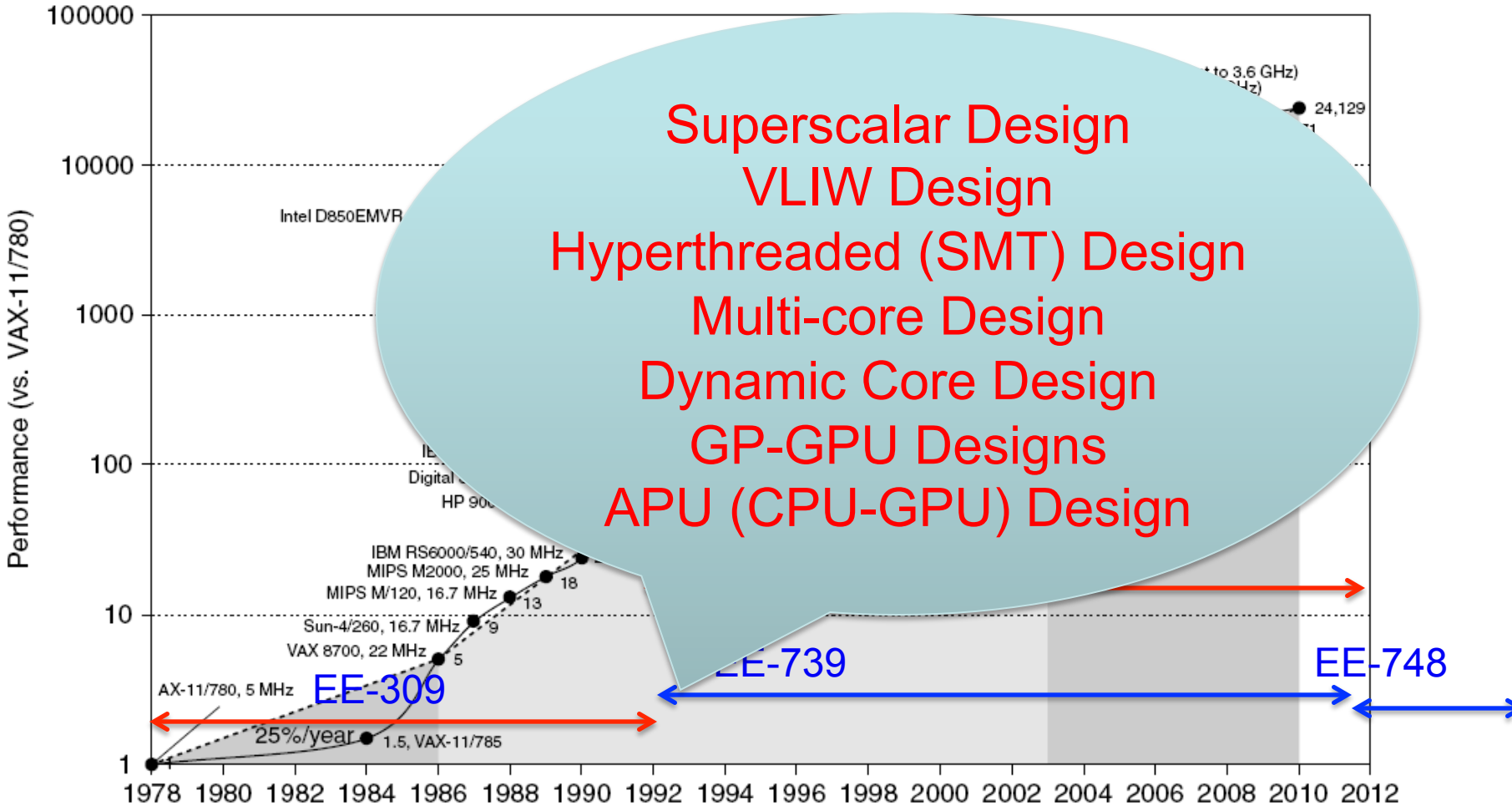
Virtuous Cycle, (1950 – 2005)



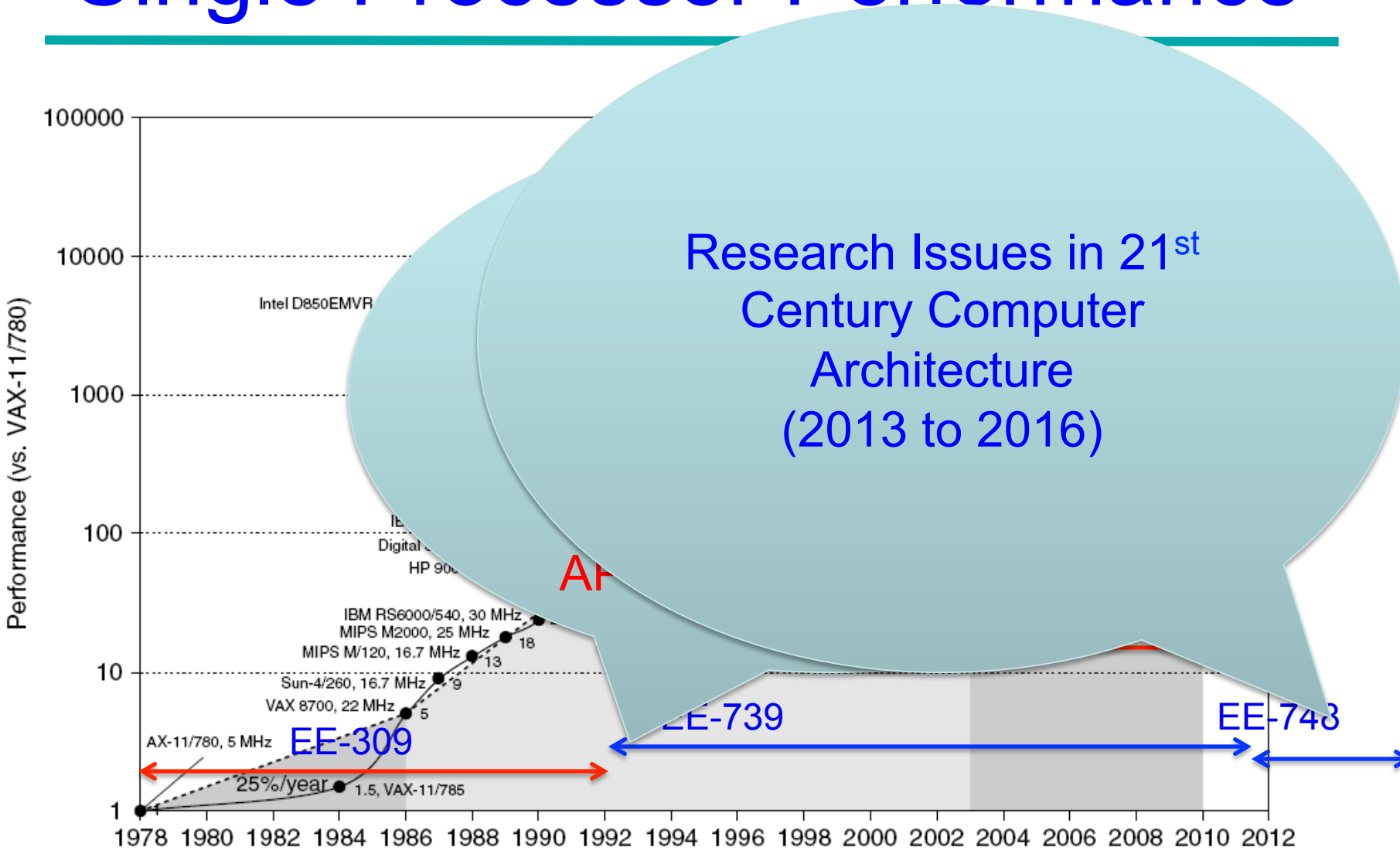
World-Wide Software Market (per IDC):

$212b (2005)

Single Processor Performance

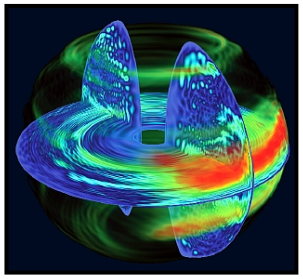


Single Processor Performance



Future of Processor Architecture

Data centers and extreme scale computing



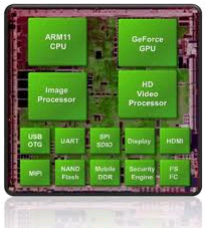
Energy and power consumption are the key limiters

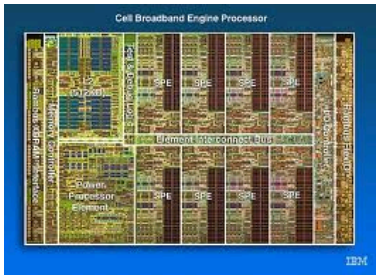
Architectures for programmability

Performance scaling:

- Past: no SW changes
- Now: extensive SW +HW changes

Specialized architectures and heterogeneity





Ultimate goal: fully automated generation of app-specific HW for programs

Future of Processor Architecture

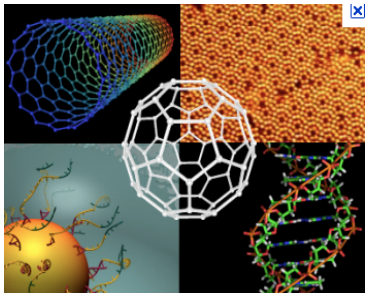
End of road for conventional ISA

Modern systems are skyscrapers built on the ISA of a bungalow

Secure, reliable and predictable from the HW up

Foundation of computing is breaking apart; malicious parties are exploiting it

Exploiting emerging technologies



Architecture research enables new technologies to enter the market quickly

Thank You