Lecture-19

Instruction Set

MVI M, DATA:

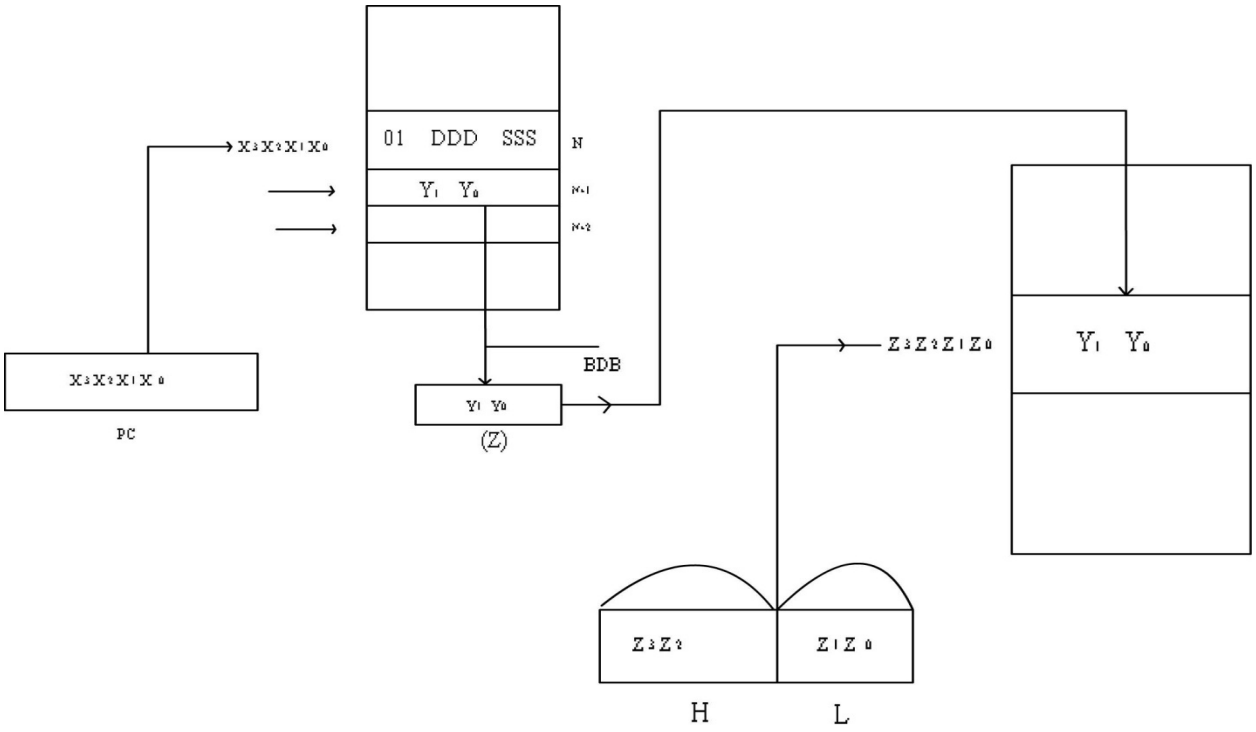
This is an ALP statement DATA is symbolic name given to the 2nd byte of the instruction MVI is the mnemonic for move immediate. M in the operand field stands for memory pointer. The meaning of the instruction is 8 bit data available as a 2nd byte of the instruction should be moved to the memory location whose address is available in m pointer namely (H, L) register pair. The macro RTL implement should be.

$$M\,(H,L) \leftarrow < B_2 >$$

The instruction format

00 110 110	N
<B_2>	N+1

There is no variation in this instruction. It is a 2 byte instruction. First byte is opcode & 2nd byte is 8 bit data. Figure 10.



The operation is illustrated in fig 10. The micro RTL flow is

$MC-1$
$OFMC$
$IO/\overline{M}=0$
$S1=1$
$S0=1$

$T1: AD_7-AD_0 \leftarrow (PCL),\ A_{15}-A_8 \leftarrow (PCH),\ ALE=$
$T2: \overline{RD}=0, (PC) \leftarrow (PC)+1,\quad AD_7-AD_0 \leftarrow M(AB)$
$T3: \overline{RD}=1, \uparrow, (IR) \leftarrow (AD_7-AD_0)$
$T4: MVIM=1$

$MC-2$
$MRMC$
$IO/\overline{M}=0$
$S1=1$
$S0=0$

$T1: AD_7-AD_0 \leftarrow (PCL),\ A_{15}-A_8 \leftarrow (PCH),\ ALE=$
$T2: \overline{RD}=0, (PC) \leftarrow (PC)+1,\quad AD_7-AD_0 \leftarrow M(AB)$
$T3: \overline{RD}=1, \uparrow, (Z) \leftarrow (AD_7-AD_0)$

$MC-3$
$MWRMC$
$IO/\overline{M}=0$
$S1=0$
$S0=1$

$T1: AD_7-AD_0 \leftarrow (L),\ A_{15}-A_8 \leftarrow (H),\ ALE=$
$T2: \overline{WR}=0,\quad AD_7-AD_0 \leftarrow (Z)$
$T3: \overline{WR}=1, \uparrow,\ M(AB) \leftarrow (AD_7-AD_0)$

It requires three m/c cycle OFMC, MRMC, MWRMC and total 10 states. It needs 5μ sec time to execute this instruction using 2 MHz internal clock. Its immediate addressing mode.

LXI rp, DDATA:

This is an ALP statement DDATA stands for double data a symbolic name given to 16 bit data available immediately as the 2nd & 3rd byte of the instruction. Rp stands for LOAD IMMEDIATE register pair. The alphabet X in the mnemonic till that register pair is involved. The meaning of the instruction is the 16 bit data immediate available as the 2nd & 3rd byte of the instruction be loaded into register pair. The macro RTL implemented is,

$$(rpL) \leftarrow < B_2 >$$
$$(rpH) \leftarrow < B_3 >$$

The instruction format is

00 RPO 001	N
<B_2>	N+1
<B_3>	N+2

Notes: Only in the instruction D_3 is zero for loading otherwise D_3 is '1' for loading. 4 variations exists in the this instruction. The bit code RP in the opcode at memory location N identifies the register pair.

RP = 00 LXI B, DDATA
RP = 01 LXI D, DDATA
RP = 10 LXI H, DDATA
RP = 11 LXI SP, DDATA

The micro RTL flow is

$MC-1$
OFMC
$IO/\overline{M}=0$
$S1=1$
$S0=1$

$T1: AD_7-AD_0 \leftarrow (PCL),\ A_{15}-A_8 \leftarrow (PCH),\ ALE=$
$T2: \overline{RD}=0,\ (PC) \leftarrow (PC)+1\quad AD_7-AD_0 \leftarrow M(AB)$
$T3: \overline{RD}=1, \uparrow,\ (IR) \leftarrow (AD_7-AD_0)$
$T4: LXI\,rp=1$

$MC-2$
MRMC
$IO/\overline{M}=0$
$S1=1$
$S0=0$

$T1: AD_7-AD_0 \leftarrow (PCL),\ A_{15}-A_8 \leftarrow (PCH),\ ALE=$
$T2: \overline{RD}=0,\ (PC) \leftarrow (PC)+1\quad AD_7-AD_0 \leftarrow M(AB)$
$T3: \overline{RD}=1, \uparrow,\ (rp) \leftarrow (AD_7-AD_0)$

$MC-3$
MRMC
$IO/\overline{M}=0$
$S1=1$
$S0=0$

$T1: AD_7-AD_0 \leftarrow (PCL),\ A_{15}-A_8 \leftarrow (PCH),\ ALE=$
$T2: \overline{RD}=0,\ (PC) \leftarrow (PC)+1\quad AD_7-AD_0 \leftarrow M(AB)$
$T3: \overline{RD}=1, \uparrow,\ (rpH) \leftarrow (AD_7-AD_0)$

It requires three m/c cycle OFMC & two MRMC. And total no of 10 states. It needs 5µsec using 2 MHz internal clock. It is immediate addressing mode.

LDA ADDR:

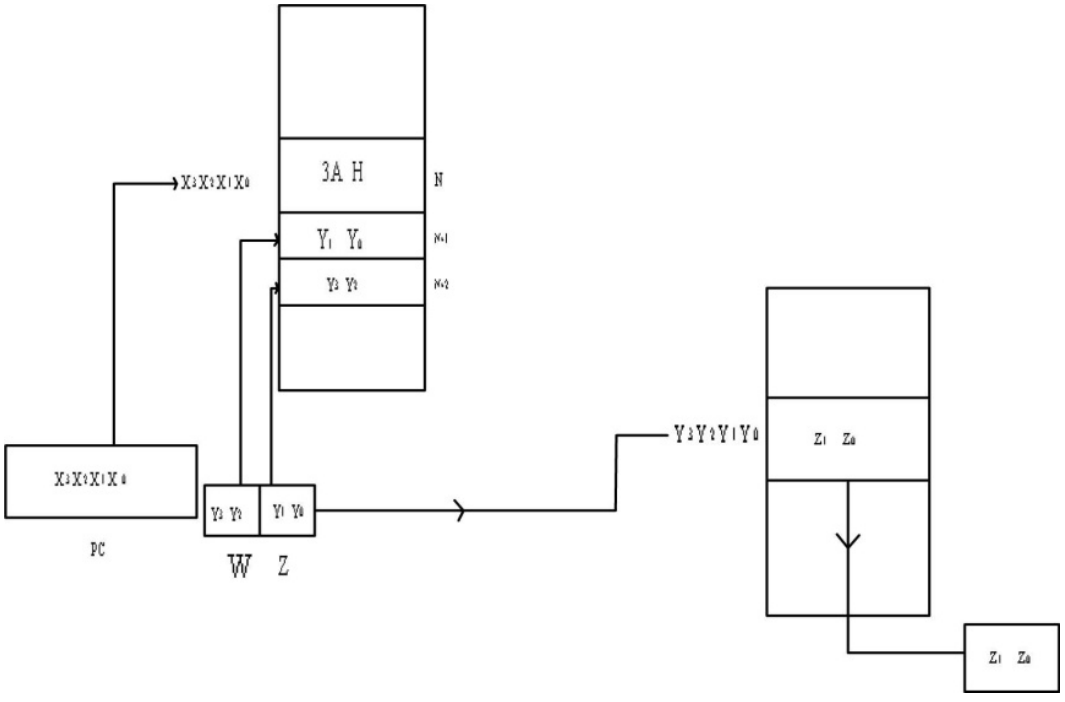
This is an ALP statement. ADDR is the symbolic name given to the 16 bit address directly available in the instruction. LDA is the mnemonic for LOAD ACCUMULATOR DIRECT. The meaning of the instruction is the content of the memory location whose address is directly available in the instruction be loaded into the accumulator this is a 3 byte instruction format is

00 111 010	N
<B_2>	N+1
<B_3>	N+2

The macro RTL implemented is

(A) $\leftarrow M(B_3, B_2)$

This is directed addressing mode



The micro RTL flow is:

MC – 1 OFMC $IO/\overline{M}=0$ S1 =1 S0 =1	T1: $AD_7 - AD_0 \leftarrow (PCL)$, $A_{15} - A_8 \leftarrow (PCH)$, ALE= T2: $\overline{RD}=0$, $(PC) \leftarrow (PC)+1$ $AD_7 - AD_0 \leftarrow M(AB)$ T3: $\overline{RD}=1, \uparrow$, $(IR) \leftarrow (AD_7 - AD_0)$ T4: LDA = 1
MC – 2 MRMC $IO/\overline{M}=0$ S1 =1 S0 =0	T1: $AD_7 - AD_0 \leftarrow (PCL)$, $A_{15} - A_8 \leftarrow (PCH)$, ALE= T2: $\overline{RD}=0$, $(PC) \leftarrow (PC)+1$ $AD_7 - AD_0 \leftarrow M(AB)$ T3: $\overline{RD}=1, \uparrow$, $(Z) \leftarrow (AD_7 - AD_0)$
MC – 3 MRMC $IO/\overline{M}=0$ S1 =1 S0 =0	T1: $AD_7 - AD_0 \leftarrow (PCL)$, $A_{15} - A_8 \leftarrow (PCH)$, ALE= T2: $\overline{RD}=0$, $(PC) \leftarrow (PC)+1$ $AD_7 - AD_0 \leftarrow M(AB)$ T3: $\overline{RD}=1, \uparrow$, $(W) \leftarrow (AD_7 - AD_0)$
MC – 4 MRMC $IO/\overline{M}=0$ S1 =1 S0 =0	T1: $AD_7 - AD_0 \leftarrow (Z)$, $A_{15} - A_8 \leftarrow (W)$, ALE= T2: $\overline{RD}=0$, $AD_7 - AD_0 \leftarrow M(AB)$ T3: $\overline{RD}=1, \uparrow$, $(A) \leftarrow M(AD_7 - AD_0)$

STA ADDR:

This is an ALP statement STA is the mnemonic for the STORE ACCUMULATOR DIRECT. The meaning of the instruction is the content of the accumulator should be moved to the memory location whose address is directly available in the instruction itself as a 2nd & 3rd byte of instruction. This is a 3 byte instruction. The instruction format is

00 110 010
<B_2>

<B_3>	N

N+1

N+2

The macro RTL should be

$M(B_2, B_3) \leftarrow (A)$

This has no variations this is. This is direct addressing mode. The micro RTL flow is:

MC – 1	
OFMC	T1: $AD_7 - AD_0 \leftarrow (PCL)$, $A_{15} - A_8 \leftarrow (PCH)$, ALE=
$IO/\overline{M} = 0$	T2: $\overline{RD}$=0, (PC)←(PC)+1 $AD_7 - AD_0 \leftarrow M(AB)$
S1 =1	T3: $\overline{RD}$=1,↑, (IR)←$(AD_7 - AD_0)$
S0 =1	T4: STA=1
MC – 2	
MRMC	T1: $AD_7 - AD_0 \leftarrow (PCL)$, $A_{15} - A_8 \leftarrow (PCH)$, ALE=
$IO/\overline{M} = 0$	T2: $\overline{RD}$=0, (PC)←(PC)+1 $AD_7 - AD_0 \leftarrow M(AB)$
S1 =1	T3: $\overline{RD}$=1,↑, (Z)←$(AD_7 - AD_0)$
S0 =0	
MC – 3	
MRMC	T1: $AD_7 - AD_0 \leftarrow (PCL)$, $A_{15} - A_8 \leftarrow (PCH)$, ALE=
$IO/\overline{M} = 0$	T2: $\overline{RD}$=0, (PC)←(PC)+1 $AD_7 - AD_0 \leftarrow M(AB)$
S1 =1	T3: $\overline{RD}$=1,↑, (W)←$(AD_7 - AD_0)$
S0 =0	
MC – 4	
MWRMC	T1: $AD_7 - AD_0 \leftarrow (PCL)$, $A_{15} - A_8 \leftarrow (PCH)$, ALE=
$IO/\overline{M} = 0$	T2: $\overline{WR}$=0, $AD_7 - AD_0 \leftarrow (A)$
S1 =0	T3: $\overline{WR}$=1,↑, M(AB)←$(AD_7 - AD_0)$
S0 =1	

It requires 4 machine cycle OFMC & 2 MRMC & one MWRMC and 13 states. It need 6.5μsec using 2 MHz internal clock.

(9) LHLD ADDR: This is an ALP statement LHLD is the mnemonic for LOAD (H, L) REGISTER PAIR DIRECT. The meaning the instruction is the content of the memory location whose address is directly available as 2nd & 3rd byte of the instruction register L and the content of the memory location at next higher address to the register H. this a 3 byte instruction. The instruction format is

00 101 010	N
$<B_2>$	N+1
$<B_3>$	N+2

The macro RTL implemented is

$(L) \leftarrow M(B_3, B_2)$

$(H) \leftarrow M((B_3, B_2)+1)$

The micro RTL flow is

$MC-1$
$OFMC$
$IO/\overline{M}=0$
$S1=1$
$S0=1$

$T1: AD_7-AD_0 \leftarrow (PCL),\ A_{15}-A_8 \leftarrow (PCH),\ ALE=$
$T2: \overline{RD}=0, (PC) \leftarrow (PC)+1,\ AD_7-AD_0 \leftarrow M(AB)$
$T3: \overline{RD}=1, \uparrow,\ M(AB) \leftarrow (AD_7-AD_0)$
$T4: LHLD=1$

$MC-2$
$MRMC$
$IO/\overline{M}=0$
$S1=1$
$S0=0$

$T1: AD_7-AD_0 \leftarrow (PCL),\ A_{15}-A_8 \leftarrow (PCH),\ ALE=$
$T2: \overline{RD}=0, (PC) \leftarrow (PC)+1,\ AD_7-AD_0 \leftarrow M(AB)$
$T3: \overline{RD}=1, \uparrow,\ (Z) \leftarrow (AD_7-AD_0)$

MC – 3

MRMC T1: $AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (PCH),\ ALE =$

$IO/\overline{M} = 0$ T2: $\overline{RD} = 0, (PC) \leftarrow (PC) + 1,\ AD_7 - AD_0 \leftarrow M(AB)$

S1 = 1 T3: $\overline{RD} = 1, \uparrow, (W) \leftarrow (AD_7 - AD_0)$

S0 = 0

MC – 4

MRMC T1: $AD_7 - AD_0 \leftarrow (Z),\ A_{15} - A_8 \leftarrow (W),\ ALE =$

$IO/\overline{M} = 0$ T2: $\overline{RD} = 0,\ AD_7 - AD_0 \leftarrow M(AB)$

S1 = 1 T3: $\overline{RD} = 1, \uparrow, (L) \leftarrow (AD_7 - AD_0)$

S0 = 0

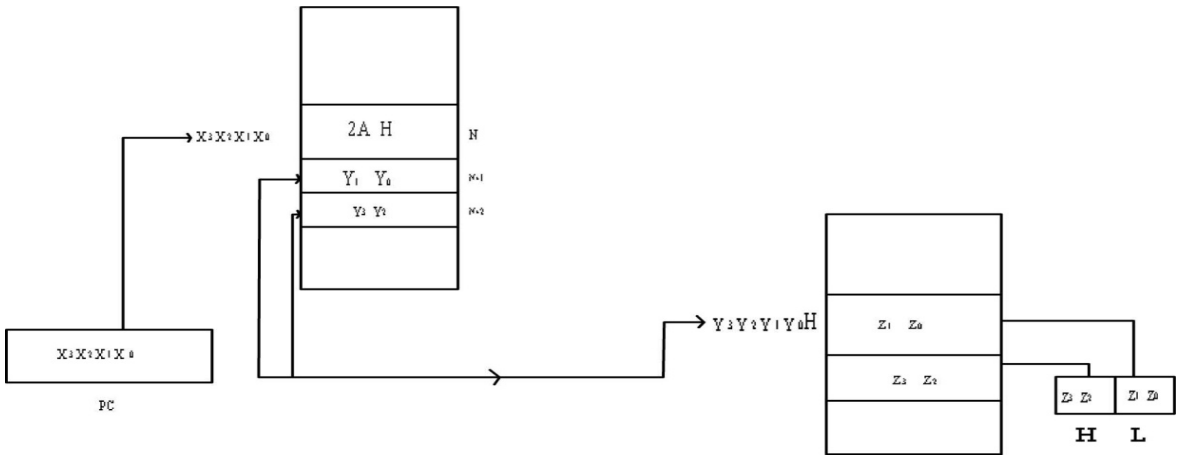
MC – 5

MRMC T1: $AD_7 - AD_0 \leftarrow (Z+1),\ A_{15} - A_8 \leftarrow (W),\ ALE =$

$IO/\overline{M} = 0$ T2: $\overline{RD} = 0,\ AD_7 - AD_0 \leftarrow M(AB)$

S1 = 1 T3: $\overline{RD} = 1, \uparrow, (H) \leftarrow (AD_7 - AD_0)$

S0 = 0



This instruction requires 5m/c cycles OFMC & 4 MRMC and total 16 states. It needs 8μs using 2 MHz clock. This instruction has no variations. It is direct addressing mode.

(10) <u>SHLD ADDR:</u> This is an ALP statement SHLD is the mnemonic for STORE (H, L) REGISTER PAIR DIRECT. The meaning for the instruction is the content of (L) register should be

moved into the memory location whose address is available as 2nd & 3rd byte of the instruction itself and the content of (H) register should be moved into the memory location whose address is next higher address. The instruction format is

00 100 010	N
$<B_2>$	N+1
$<B_3>$	N+2

The macro RTL implemented should be,

$M(B_3, B_2) \leftarrow (L)$

$M((B_3, B_2)+1 \leftarrow (H)$

The micro RTL flow is,

$MC-1$

$OFMC$

$IO/\overline{M}=0$

$S1=1$

$S0=1$

$T1: AD_7-AD_0 \leftarrow (PCL),\ A_{15}-A_8 \leftarrow (PCH),\ ALE=$

$T2: \overline{RD}=0, (PC) \leftarrow (PC)+1,\ AD_7-AD_0 \leftarrow M(AB)$

$T3: \overline{RD}=1, \uparrow, (IR) \leftarrow (AD_7-AD_0)$

$T4: SHLD=1$

$MC-2$

$MRMC$

$IO/\overline{M}=0$

$S1=1$

$S0=0$

$T1: AD_7-AD_0 \leftarrow (PCL),\ A_{15}-A_8 \leftarrow (PCH),\ ALE=$

$T2: \overline{RD}=0, (PC) \leftarrow (PC)+1,\ AD_7-AD_0 \leftarrow M(AB)$

$T3: \overline{RD}=1, \uparrow, (Z) \leftarrow (AD_7-AD_0)$

$MC-3$

$MRMC$

$IO/\overline{M}=0$

$S1=1$

$S0=0$

$T1: AD_7-AD_0 \leftarrow (PCL),\ A_{15}-A_8 \leftarrow (PCH),\ ALE=$

$T2: \overline{RD}=0, (PC) \leftarrow (PC)+1,\ AD_7-AD_0 \leftarrow M(AB)$

$T3: \overline{RD}=1, \uparrow, (W) \leftarrow (AD_7-AD_0)$

$MC-4$	
MWRMC	T1: $AD_7-AD_0 \leftarrow (PCL),\ A_{15}-A_8 \leftarrow (PCH),\ ALE=$
$IO/\overline{M}=0$	T2: $\overline{WR}=0,\quad AD_7-AD_0 \leftarrow (A)$
$S1=0$	T3: $\overline{WR}=1,\uparrow,\ M(AB) \leftarrow (AD_7-AD_0)$
$S0=1$	
$MC-5$	
MWRMC	T1: $AD_7-AD_0 \leftarrow (PCL),\ A_{15}-A_8 \leftarrow (PCH),\ ALE=$
$IO/\overline{M}=0$	T2: $\overline{WR}=0,\quad AD_7-AD_0 \leftarrow (A)$
$S1=0$	T3: $\overline{WR}=1,\uparrow,\ M(AB) \leftarrow (AD_7-AD_0)$
$S0=1$	

This instruction requires 5 m/c cycles OFMC, 2MRMC & 2 MWRMC and total 16 states, it needs 8µsec using 2 mhz. this instruction has no variations. It is direct addressing mode