Lecture-23

LOGICAL GROUP:

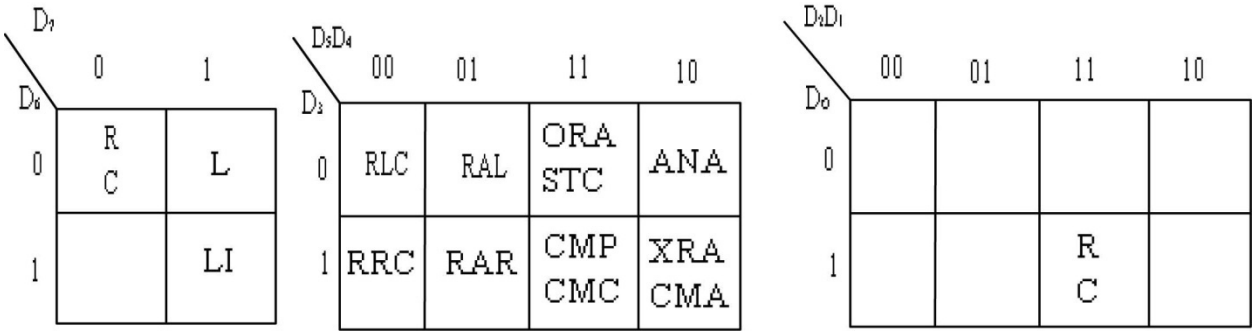


Fig 17

Fig 17 gives the operation code format for logical group. It consists of 19 basic instructions. There are three basic logic operation AND XOR & OR logical operation takes place bit by. The operand is assumed to be in the accumulator. The second operand is seen either in the internal general purpose register, in the memory location pointed to the M- pointer or as the second byte logical operation is stored back in the accumulator.

(21) ANA v: The macro RTL implemented is

$(A_i) \leftarrow (A_i) n (v_i) \qquad i = 0 \text{ to } 7$ Or

$(A) \leftarrow (A)\ n\ (v)$

This is a single byte instruction. The meaning of the instruction is AND bit by bit the content of register (v) to the content of accumulator and store the result back in the accumulator. The operation code is

10 SSS	100

N

It has 7 variations. The micro RTL flow is given below. The cy flag is cleared and AC is set.

	$T1: AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \rightarrow (PCH), ALE =$
OFMC	$T2: \overline{RD} = 0,\ (PC) \rightarrow (PC)H, AD_7 - AD_0 \leftarrow M(AB)$
$IO/\overline{M} = 0$	$T3: \overline{RD} = 1, \uparrow,\ (IR) \leftarrow (AD_7 - AD_0)$
$S1 = 0$	$T4: (A) \leftarrow (A) \cap (r)$
$S0 = 1$	FEO

It requires single M/C cycle OFMC of 4 states. It is register addressing mode.

ANA M:

The macro RTL implemented is,

$(A) \leftarrow (A) \cap M(H, L)$

This is a single byte instruction the meaning of the instruction is AND bit byte the content of the memory location whose address is stored in (H, L) pair to the content of the accumulator and store the reset back in the accumulator. The operation code is,

10	100	110

N

It has no variation. The Micro RIL flow as given below:

	$T1: AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (PCH), ALE =$
OFMC	$T2: \overline{RD} = 0,\ (PC) \leftarrow (PC) + 1, (AD_7 - AD_0) \leftarrow M(AB)$
$IO/\overline{M} = 0$	$T3: \overline{RD} = 1, \uparrow,\ (IR) \leftarrow (AD_7 - AD_0)$
$S1 = 0$	$T4: ANAM = 1$
$S0 = 1$	

MRMC T1: $AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (H),\ ALE =$

$IO/\overline{M} = 0$ T2: $\overline{RD} = 0,\ (PC),\ (AD_7 - AD_0) \leftarrow M(H,L)$

$S1 = 1$ T3: $\overline{RD} = 1, \uparrow,\ (Temp) \leftarrow (AD_7 - AD_0),\ (A) \leftarrow (A) \cap (Temp)$

$S0 = 0$

It requires 2 machine cycle OFMC & MRMC 7 states. It is regular indirec5t addressing mode.

ANI DATA → The macro RTL implemented

$$(A) \leftarrow (A) \cap < B_2 >$$

It is two byte instruction the meaning of the instruction is AND bit by bit the content available as a second byte of instruction to the content of the accumulator and store the result back in the accumulator the operation code is

11 011 110
<B_2>

It has no variation the micro RTL flows given below

OFMC T1: $AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (PCH),\ ALE =$

$IO/\overline{M} = 0$ T2: $\overline{RD} = 0,\ (PC) \leftarrow (PC) + 1,\ (AD_7 - AD_0) \leftarrow M(AB)$

$S1 = 1$ T3: $\overline{RD} = 1, \uparrow,\ (IR) \leftarrow (AD_7 - AD_0)$

$S0 = 0$ T4: $ANI\ DATA = 1$

MRMC T1: $AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (H),\ ALE =$

$IO/\overline{M} = 0$ T2: $\overline{RD} = 0,\ (PC),\ (AD_7 - AD_0) \leftarrow M(H,L)$

$S1 = 1$

$S0 = 0$ T3: $\overline{RD} = 1, \uparrow,\ (Temp) \leftarrow (AD_7 - AD_0),\ (A) \leftarrow (A) \cap (Temp)$

It requires two machine cycle OFMC&MRMC and 7 states. It is immediate addressing mode.

Note: In these AND operation except for CY and AC flags other flags are effect as per standard rules, CY flag is always clear to'0' and AC flag set to'1'.

XRA r Exclusive or register the macro RTL implemented is,
(A) ← (A) + (r)

It is a single byte instruction the meaning of the instruction is exclusively
Ed bit by bit the contents of register r is with the contents of accumulator and
Store the result back into accumulator the operation code is

1 0	1 0	1	S	S	S

N

It has seven variations and the addressing mode is register addressing mode. Only one Machine cycle is required i.e. OFMC of 4 states.
XRA M Exclusive OR memory), the macro RTL implemented is
(A) ← (A) + M (H, L)
It is a single byte instruction the meaning of the instruction is exclusively ORed bit by bit the contents of memory location printed by (H,L) register pair with the contents of accumulator and Store the result back into accumulator the operation code is,

1 0 1 0 1 1 1 0

N

If has no variation the addressing mode is register indirect addressing mode two machine cycles are required OFMC-4, OFMC-3,is total 7 states.

XRI data (Exclusive OR immediate), the macro RTL implemented is
(A) ← (A) + < B_2>

If is a two byte instruction the meaning of the instruction is the contend of the second byte of the construction is exclusive ORed with the contents of accumulator bit by bit and the result is stored back into accumulator the operation code is,

11 101 110

If has no variation the addressing mode is immediate addressing mode two M/C cycles are required OFMC-4, ΔMRMC-3 is total 7 states.

Note 1: In all exclusive – OR ALP is all the flags are affected as per standard rule expect AC & CY flags are cleared.

2. There is no explicit instruction to clear the accumulator to 'zero' however it is implicit is the statement XRAA. This means (A) Δ (A) + (A) ,the result will be 0000 0000 is the accumulator along with dealing AC & CY flags.

7) ORA r (OR Register), this is an ALP statement. The macro RTL implemented is,

(A) ← (A) U (r)

If is a single byte instruction the contend of the register r is inclusive ORed with the contents of accumulator bit by bit and the result is stored back into accumulator the operation code is,

1 0 1 1 0 S S S	N

If has seven variation the addressing mode is register addressing mode if

requires are M/C cycles OFMC of 4 states, All the flags are affected except AC Δ CY flags are cleared.

8). ORA M (OR Register), this is an ALP statements .the macro RTL implemented is

(A) ← (A) U M (H, L)

If is a single byte instruction the content of the memory location whose address is available in the H, L register pair is inclusive ORed with the contents of accumulator and the result is placed in the accumulator. The operation code is,

1 0 1 1 0 110	N

If it has no variation the addressing mode is register indirect addressing mode if requires two M/C cycles OFMC- 4 and MRMC- 3 & total 7 states. All the flags are affected except AC Δ CY flags are cleared.

9). ORI data (OR immediate), this is an ALP statements .the macro RTL implemented is,

(A) ← (A) U < B_2 >

If in a two byte instruction, the content of the second byte of the instruction is inclusive ORed with bit by bit with the contents of accumulator. The operation code is,

11 110 1 1 0
< B_2 >

If has no variation the addressing mode is immediate addressing mode. If

requires two Machine cycles OFMC- 4 and MRMC- 3 & total 7 states. All the flags are affected except AC Δ CY flags are cleared.

Note: ANI data, XRI data & ORI data are used for manipulating any bit of the

Accumulated without affecting the other bits. For example,

(i) Set Bit 5 of ACC without affecting the other bits.

OR operation $\frac{B_7}{A_7}\ \frac{B_6}{A_6}\ \frac{B_5}{1}\ \frac{B_4}{A_4}\ \frac{B_3}{A_3}\ \frac{B_2}{A_2}\ \frac{B_1}{A_1}\ \frac{B_0}{A_0}$ `

ORI 20 set bit 5 of (A) without affecting the other bits. This is known as Masking.

(ii) Force bit 3 & bit 2 to 0,0 without affecting the other bits.

ANI operations $\frac{B_7}{A_7}\ \frac{B_6}{A_6}\ \frac{B_5}{1}\ \frac{B_4}{A_4}\ \frac{B_3}{A_3}\ \frac{B_2}{A_2}\ \frac{B_1}{A_1}\ \frac{B_0}{A_0}$ ANI F3

4

(iii) Complement bit – 7 , bit-5 & bit -3 without affecting the other bits.

EX-OR operation $\frac{B_7}{A_7}\ \frac{B_6}{A_6}\ \frac{B_5}{1}\ \frac{B_4}{A_4}\ \frac{B_3}{A_3}\ \frac{B_2}{A_2}\ \frac{B_1}{A_1}\ \frac{B_0}{A_0}$ XRI AS

4

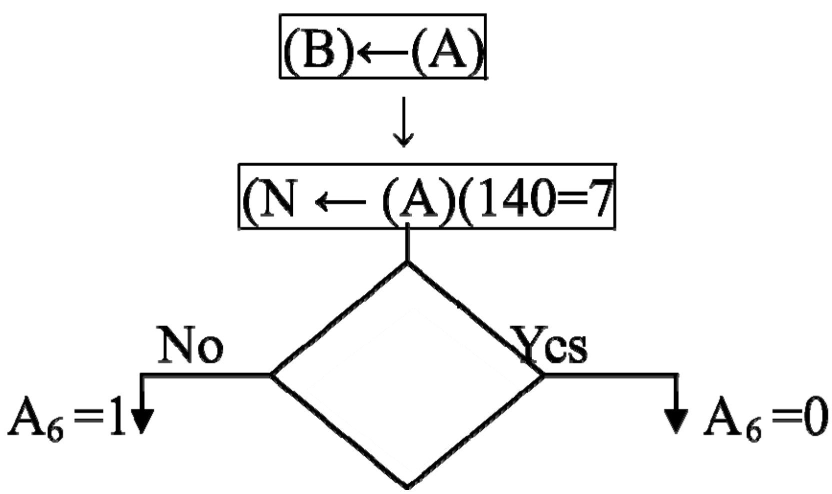
(iv) Test a particular bit (say bit.6) to find whether it is zero or 1

And $\frac{B_7}{A_7}\ \frac{B_6}{A_6}\ \frac{B_5}{1}\ \frac{B_4}{A_4}\ \frac{B_3}{A_3}\ \frac{B_2}{A_2}\ \frac{B_1}{A_1}\ \frac{B_0}{A_0}$ MOV B,A

ANI 40

2f A_6= 0, content of the code will be zero

A_6 = 1, content of the code will be non zero.



13. CMP r: (compare register with ACC) this is also an ALP statement. The content is also an ALP statement the content of register r is subtracted from the accumulator (A) – (r) operation is performed but the result of the subtraction operation is not content of Acc & register (r) is not destroyed but as result of this operation the flags are affected as per standard rule as follows.

If (A) > (V) CY = 0, z = 0

(A) = (V) CY = 0, z = 1

(A) < (V) CY = 1, z = 0

If is a single byte instruction. The operation code is,

10 111 S S S

If has seven variations. The addressing mode is requiring addressing mode. One M/C cycle is required OFMC – 4 of 4 states.

CMP M: (compare memory with ACC); the content of the memory location whose address is contained in the HL register pair is subtracted from the accumulator. The accumulator remains unchanged. The condition flags are
set as a result of the subtraction.

2f (A) >M (H,L) CY = 0, z = 0

(A) = M (H,L) CY = 0, z = 1

(A) < M (H,L) CY = 1, z = 0

2f is a single byte instruction. The operation code is,

1 0 1 1 0 110	N

It has no variations. The addressing mode is requiring indirect addressing mode. It requires two machines cycle of OFMC & NMRC of seven states.

12) CPI data: (compare immediate) this is an ALP statement. The content of the second byte of the instruction is subtracted from the

accumulator, the result of the subtraction flags are set as a result of the subtraction. The Z flag is set if

(A) = < B_2)>,the CY flag is set if (A) = < B_2)>

2f is a two byte instruction the operation code is

11 110 1 1 0
< B_2 >

2f has no variations. The addressing mode is immediate addressing. It requires too M/C cycle OFMC and MRMC of seven states.