Lecture-11

INTERRUPT CONTROL SIGNALS → TRAP at pin no 6, RST 7.5 at pin no 7,at pin no 6.5 at pin no 8, RST 5.5 at pin no 9, and INTR at pin no 10 are interrupt control signal input provided for interrupting the μp while it is executing the main programme. These interrupt control signal input can be broadly divided in to two categories.

(a) Non – maskable interrupts

(b) Maskable interrupts

Non – maskable control signal input are those control signal input which can interrupt the μp programming execution once the power is ON. The maskable interrupts are those control signal inputs which can be individually disabled or enabled as and when necessary, once the power is on. The TRAP signal control input of INTEL 8085 is NMI (non-maskable interrupts) signal.

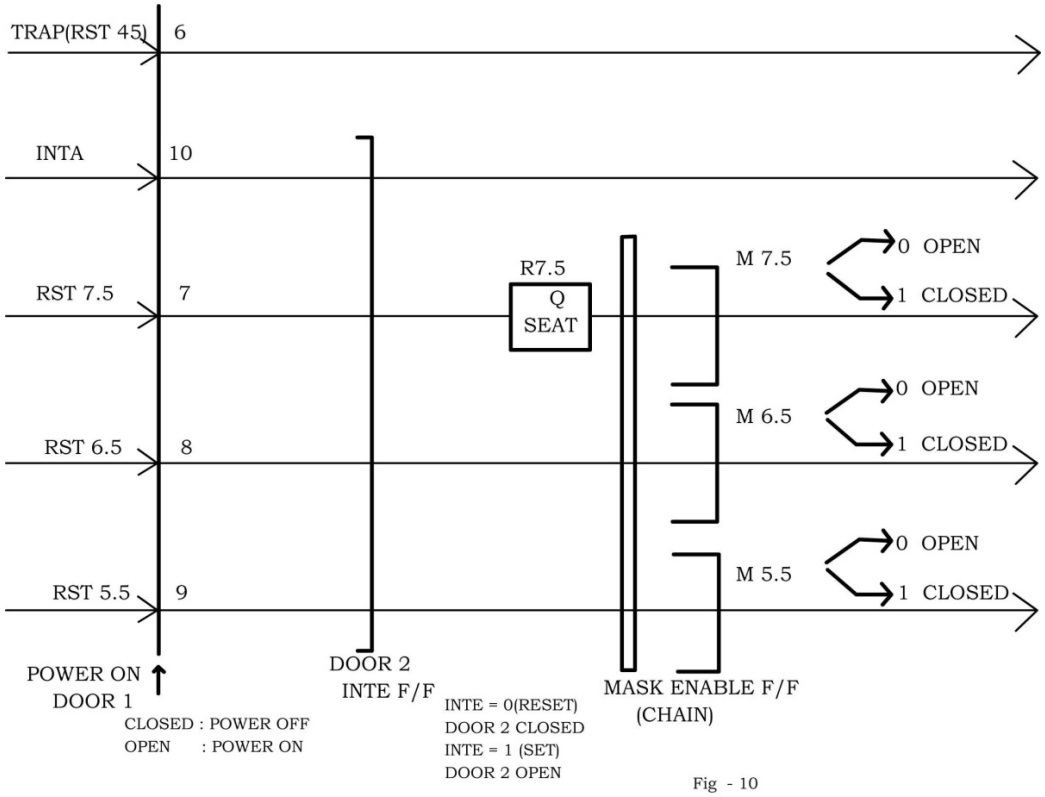

Fig - 10

The way these interrupt control signal input interrupt the μp can be pictorially represented as shown in fig.10.

TRAP at pin no.6:

TRAP is a non maskable RESTART vectored interrupt. When the power is ON, it is enabled and enable interrupt command is required TRAP has the highest priority of any interrupt. It is both raising edge and lends sensitive interrupt i.e. it becomes active at the Lo-Hi edge but must stay high until it is sampled and recognized. Whenever this interrupt is recognized, it forces the 8085 A to perform a CALL (0024) H instruction, means when the current execution is over, the PC is loaded with 0024 H so that the CPU starts executing the program from 0024 H.

INTR at pin no.10:

This is the lowest priority interrupt request in the 8085 A processor and is used as a general purpose interrupt. An input of INTR=1 implies some external device has put up an interrupt and wants the CPU to execute an appropriate service routine. The 8085 A monitors the status of the INTR line by sampling it in the last but one clock cycle of each instruction and during HOLD & HALT states. If the interrupt structure of the 8085 A is enabled when INTR is sampled high, the program counter (PC) will not be incremented and an INTA=0 will be issued by the μp in response to INTR. It is now the responsibility of the interrupting device to issue a RESTART or CALL instruction so that the 8085 A can jump to the proper interrupt service routine.

The INTR is enabled by executing a EI instruction and is disabled by executing a DI instruction. Disabled means INTR will not be acknowledged. It is also disabled by RESET and immediately after an interrupt is acknowledged.

INTA at pin no.11:

(Interrupt acknowledge) This is an active low control signal output. When the μρ acknowledges the interrupt than instead of RD signal it issues INTA signal to tell the external world that it is in interrupt acknowledge m/c cycle. Basically, it replaces RD control signal output during INTA m/c cycle. INTA is normally high and becomes active low during T_2 timing slot of the μρ and goes high again during T_3 state of the μρ just like RD signal. During this period RD signal is HIGH. It can be used to activate an 8259 A interrupt chip or some other interrupt port.

RST 5.5, 6.5 & 7.5:

These are 8085 A's maskable restored interrupts. They operate exactly like INTR except for the following:

1. The RESTART instruction is automatically inserted by internal logic. It does not have to be provided from outside. These instructions are:

RST 5.5	CALL 0020 H
RST 6.5	CALL 0034 H
RST 7.5	CALL 0030 H

The address for any RST can be calculated multiplying the RST number with 8 and converting it into hex.

E.g. For RST 5.5 the address is 5.5x8 = 44D = 002C H

2. RST 7.5 is an edge (LO-Hi) sensitive interrupt unlike RST 6.5, RST 5.5 and INTR which are lend (High) triggered.
3. These three interrupts can be individually masked or unmasked using SIM instructions.
4. They have higher priority than INTR, among them RST 7.5 has the highest priority and RST 5.5 has the lowest priority.

Like the INTR, whenever any of these interrupts is recognized it disables all the interrupts. These interrupts can be enabled/disabled using EI/DI instruction.

M7.5 (Mask 7.5) is a FLIP-FLOP, R7.5 (RESET 7.5) is a flip-flop. It is normally RESET when the power is on. Only LOW to HIGH transition of RST 7.5 will SET the FLIP-FLOP and stores in R7.5. When M7.5 is RESET only then this signal can interrupt the μp. R7.5 provides a seat (MASK is said open when it is RESET). A common chain (MASK ENABLE FLIP-FLOP) is provided for all the MASKS. This MASK ENABLE must be SET for individually enabling or disabling the MASK doors.

The pictorial representation shown in fig-10 is self-explanatory. The following FLIP-FLOPs are internally provided in the interrupt system of the μp.

1). <u>INTE FLIP-FLOP</u>→

When this FLIP-FLOP is RESET, the entire interrupt system is disabled except for TRAP & no other interrupt control signal can interrupt the μp. When the INTE FLIP-FLOP is SET, the interrupt

system is enabled and the other interrupt control signal can be selectively enabled or disabled.

When the power is ON for the first time $\overline{RESET\ IN}$ goes LOW and it RESET, the INTE FLIP-FLOP so that the entire interrupt system is disabled as described above. Then the INTE FLIP-FLOP can be SET or RESET using instructions.

2) <u>INTA FLIP-FLOP (Interrupt acknowledge F/F) →</u>

This is used only for internal operation by the μp.when first the power is ON this FLIP-FLOP will be RESET by the $\overline{RESET\ IN}$ control signal. Thereafter, whenever a valid interrupt is recognized by the μp it always RESETs the INTE FLIP-FLOP and then SET, the INTA FLIP-FLOP. Before further action thus, further interrupts shall not be recognized, unless, user through instructions in the programme desires further recognition of the interrupt. This statement shall be elaborated further in the interrupt chapter.

<u>MASK FLIP-FLOP (M5.5, M6.5, M7.5)</u>→

These Mask FLIP-FLOPs are used individually to MASK the interrupts RST5.5, RST 6.5, RST7.5 (RST stands for RESTART). When these FLIP-FLOPs are individually SET, then the corresponding interrupt is masked and the interrupt control signal in question can not interrupt the μp (see fig-10). These Mask FLIP-FLOPs can be individually and selectively CLEAR to '0' through SIM instruction (SET INTERRUPT MASK) provided a particular FLIP-FLOP known as MASK ENABLE FLIP-FLOP is also SET (set fig-10)

MASK ENABLE FLIP-FLOP can be SET simultaneously using SIM instruction.

R7.5 FLIP-FLOP →

The RST 7.5 control signal input is a LOW to HIGH transition active interrupt control signal input. The LOW to HIGH transition of the signal is registered in R7.5 FLIP-FLOP. Whenever M7.5 FLIP-FLOP is CLEAR, the output of R7.5 is sensed and recognized as an interrupt by the μp R7.5 FLIP-FLOP can be CLEAR through the same SIM instruction. It is for the user to make use of these facilities.

With the above explanation, we can write the logic expression for the logic variable, VALID INT.

VALID INT = 0 when none of the interrupt control signal input are interrupting the microprocessor and VALID INT = 1 when any of the interrupt control signal is active. Thus

VALID INT= TRAP+ INTE [INTR+R7.5$\overline{M7.5}$ + RST 6.5$\overline{M6.5}$+ RST 5.5$\overline{M5.5}$]

$\overline{INTA}$(Interrupt acknowledge bar) signal at pin no.11→

This is an active LOW control signal output replaces $\overline{RD}$ control signal at pin no 32 during INTA machine cycle. when INTR control signal input at pin no 10interrupt μp the μp tells the outside world that it is in INTA machine by issuing IO/$\overline{M}$=1 and also S_1=1, S_0=1throughout the machine cycle $\overline{INTA}$ output is normally HIGH and becomes LOW

during T_2 timing slot of the μp and goes high again during T_3 state of the μp just like $\overline{RD}$ signal (note that $\overline{RD}$=1 during this cycle).

SID & SOD at PIN NO 5 & 4 →

SID stands for SERIAL INPUT DATA and SOD stands for SERIAL OUTPUT DATA. These two pins are specially provided in 8085 μp for communicating with serial devices, like CRT, TTY, PRINTERS etc. μp as and when needed uses SID, SOD lines for transfer of data bit by bit along the same lines more about these lines when we talked about the use of RIM & SIM instructions.

Status Signals S_1 (33) and S_0 (29):

These two outputs along with IO/M signal output identify the type of the machine cycle being executed by the 8085 A. These signals are issued (or become valid) at the beginning of the machine cycle and remain stable throughout the machine cycle. The falling edge of ALE may be used to catch the state of these lines. The seven types of machine cycles are:

1. Opcode Fetch Machine Cycle (OFMC)
2. Memory Read Machine Cycle (MRMC)
3. Memory Write Machine Cycle (MWRMC)
4. I/O Read Machine Cycle (IORMC)
5. I/O Write Machine Cycle (IOWRMC)
6. Interrupt Acknowledge Machine Cycle (INTAMC)
7. Bus Idle Machine Cycle. (BIMC)

The μp tells the external world the type of m/c cycle it is IN by issuing the status signals IO/$\overline{M}_{(34)}$, $S1_{(33)}$ and $S0_{(29)}$ throughout the machine cycle. The truth table is shown below:

Machine Cycle	Status signal			Control Signal		
	IO/M	S1	S0	RD	WR	INTA
OFMC	0	1	1	0	1	1
MRMC	0	1	0	0	1	1
MWRMC	0	0	1	1	0	1
IORMC	1	1	0	0	1	1
IOWRMC	1	0	1	1	0	1
INTAMC	1	1	1	1	1	0
BIMC						
HALT	X	0	0			

These control signal are normally HIGH and becomes active LOW during T_2 state and goes back to HIGH during T_3 state. In between T_2 & T_3 states any no of WAIT states T_w can be inserted.

HOLD at pin no 39 and HLDA at pin no 38:

HOLD is a control signal input and HLDA is a control signal output these two (hold acknowledge) signals are used for hand shaped control during DMA operation (Direct memory access). The use of these control signals are depicted in the function diagram of fig-12

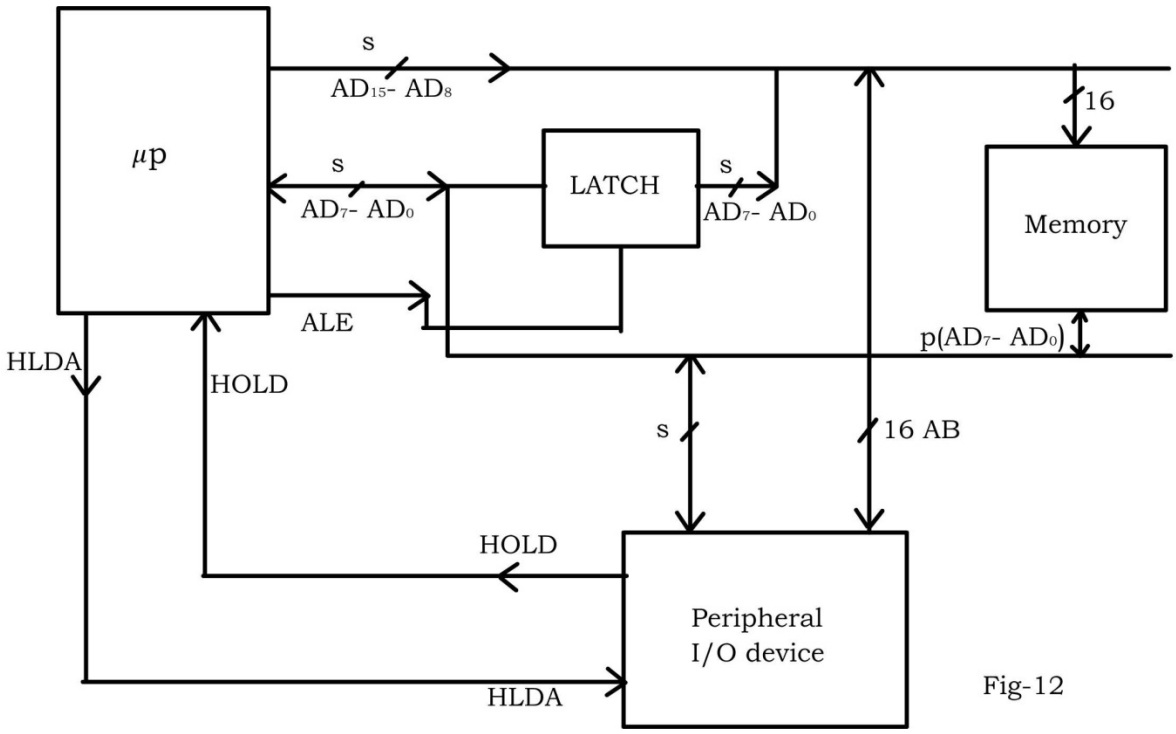

Fig-12

The device asking for DMA makes the HOLD signal HIGH the μp which continually monitor the HOLD signal input during even m/c cycle recognizes that an external device is requesting for a DMA, complete the current m/c cycle in, thereafter, tri -states the address bus & the BDB (Bi-directional data bus), enters in to a HOLD states. T_{HOLD} also while entering the HOLD state it issues the HLDA control signal at pin no 38 HIGH. The external device asking for DMA monitors the HLDA control signal and knows that the μp has gone into the HOLD state when HLDA is HIGH thereafter, the address bus and the data bus which are tri state with respect to the μp are in the exclusive control of external signal asking DMA. The DMA operation between the external device and memory continues

The μp while in HOLD state continues to monitor the HOLD control signal input as long as it is HIGH it remains in HOLD state. The

external device performing the DMA operation, after completing its operation makes HOLD signal LOW to tell the μp that the DMA is over μp which is continuously monitoring HOLD signal in HOLD state recognizes the above fact & comes out of HOLD state and continues the operation from there it has gone into HOLD state.