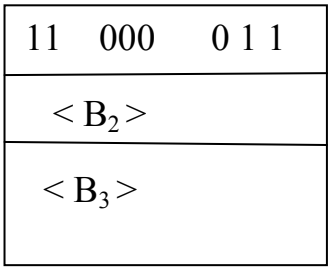
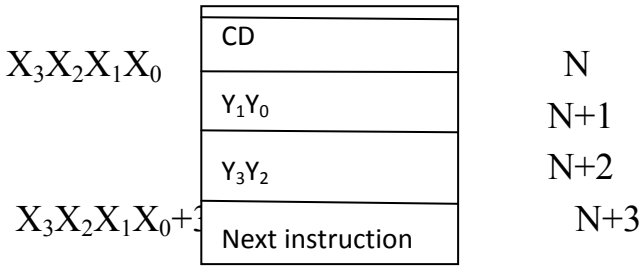
Lecture-25

2. CALL ADDR: This is an ALP statement ADDR the symbolic name given to the 16-bit address available as the 2nd and 3rd byte of the instruction that is a 3byte instruction the operation code format is,



N = CD 4
N + 1
N + 2

If a program it looks as shown in fig.



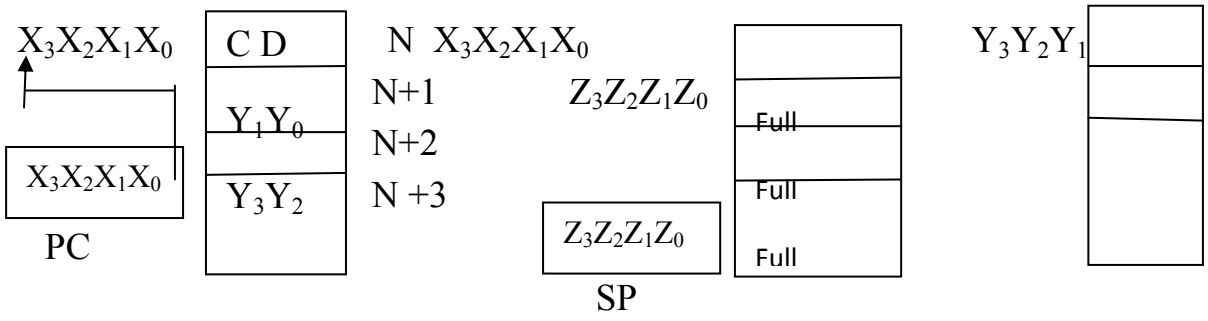
N
N+1
N+2
N+3

The op-code cycle CD being at memory location, the next address being $(X_3X_2X_1X_0)_4$ then N +3 = $(X_3X_2X_1X_0)_4$ is known as the return address this instruction is used for unconditional subroutine CALL. The starting address of the subroutine is $Y_3Y_2Y_1Y_0$ available immediately in the instruction itself. The stack is made use of to store the return address before jumping to the subroutine. The meaning of the instruction is save the return address on the PC with the address immediately available RTL implemented is,

M [(sp)-1]← (PCH)
M [(sp)-2]← (PCL)
(sp) ← (sp)-2
(pc) ← (B_3 , B_2)

Where (PCH,PCL) is the RETURN address the high order 8bits of the return address are moved to the memory location whose address is are less

than the content of sp. The low order 8 bits of the return address are moved to the memory location whose address is two less than the content of SP the content of the register SP is decremented by 2 so that it always point to the top of the stick. Content is transferred to the instruction whose address is specified in byte 2 & 3 of the current mode because the 16- bit address is immediately available in the instruction. Their also includes register indirect address has to be saved in the memory location whose address is available in the register SP. Condition before execution is,



The main RTL flow is

MC - 1

OFMC T_1 : AD_7- $AD_0 \leftarrow$ (PCL) , $A_{15} - A_8 \leftarrow$ (PCH), ALE =

IO/$\overline{M}$ = 0 T_2 : $\overline{RD}$ = 0, (PC) $\leftarrow$ (PC)+1, AD_7- $AD_0 \leftarrow$ M(AB)

S_1 = 1 T_3 : $\overline{RD}$ = 1, ↑. (IR) $\leftarrow$ (AD_7- AD_0)

S_0 = 1 T_4 : CALL = 1

$\{T_0, T_6$: (sp) $\leftarrow$ (sp) - 1

MC - 2

MRMC T_1 : AD_7- $AD_0 \leftarrow$ (PCL) , $A_{15} - A_8 \leftarrow$ (PCH) ,ALE =

IO/$\overline{M}$ = 0 T_2 : $\overline{RD}$ = 0, (PC) $\leftarrow$ (PC)+1, AD_7- $AD_0 \leftarrow$ M(AB)

S_1 = 1 T_3 : $\overline{RD}$ = 1, ↑. (Z) $\leftarrow$ (AD_7- AD_0)

S_0 = 1

MC - 3

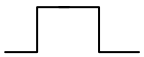
MRMC T_1 : AD_7- AD_0 ← (PCL) , A_{15} – A_8← (PCH) ,ALE = 

IO/$\overline{M}$ = 0 T_2 : $\overline{RD}$ = 0, (PC) ← (PC)+ 1, (AD_7- AD_0) ← M(AB)

S_1 = 1 T_3 : $\overline{RD}$ = 1, ↑. (W) ← (AD_7- AD_0)

S_0 = 1

MC - 4

RMC T_1 : AD_7- AD_0 ← (SPL) , A_{15} – A_8← (SPH) ,ALE = 

IO/$\overline{M}$ = 0 T_2 : $\overline{WR}$ = 0, (AD_7- AD_0) ← (PCH),(SP) ←(SP)-1

S_1 = 1 T_3 : $\overline{WR}$ = 1, ↑. M(AB) ← (AD_7- AD_0) , (SP) ←(SP)-1

S_0 = 1

MC - 5

NRMC T_1 : AD_7- AD_0 ← (SPL) , A_{15} – A_8← (SPH), ALE = 

IO/$\overline{M}$ = 0 T_2 : $\overline{WR}$ = 0, (AD_7- AD_0) ← (PCL),

S_1 = 1 T_3 : $\overline{WR}$ = 1, ↑. M(AB) ← (AD_7- AD_0) ,

S_0 = 1

T_1 : A_{15}- A_8 ← (W) , AD_1 – AD_0← (Z) , ALE = 

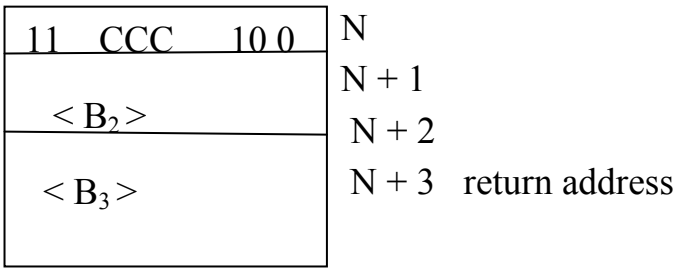
FEO T_2 : $\overline{RD}$ = 0, 1 (PC) ← (WZ) +1,

Thus it requires 5 machine cycles and total18 states the largest instruction cycle is 8085.using 4MH_3 crystal, is 2 MH_3 internal lock it require 9μ sec to execute this instruction there is no variation in this instruction.

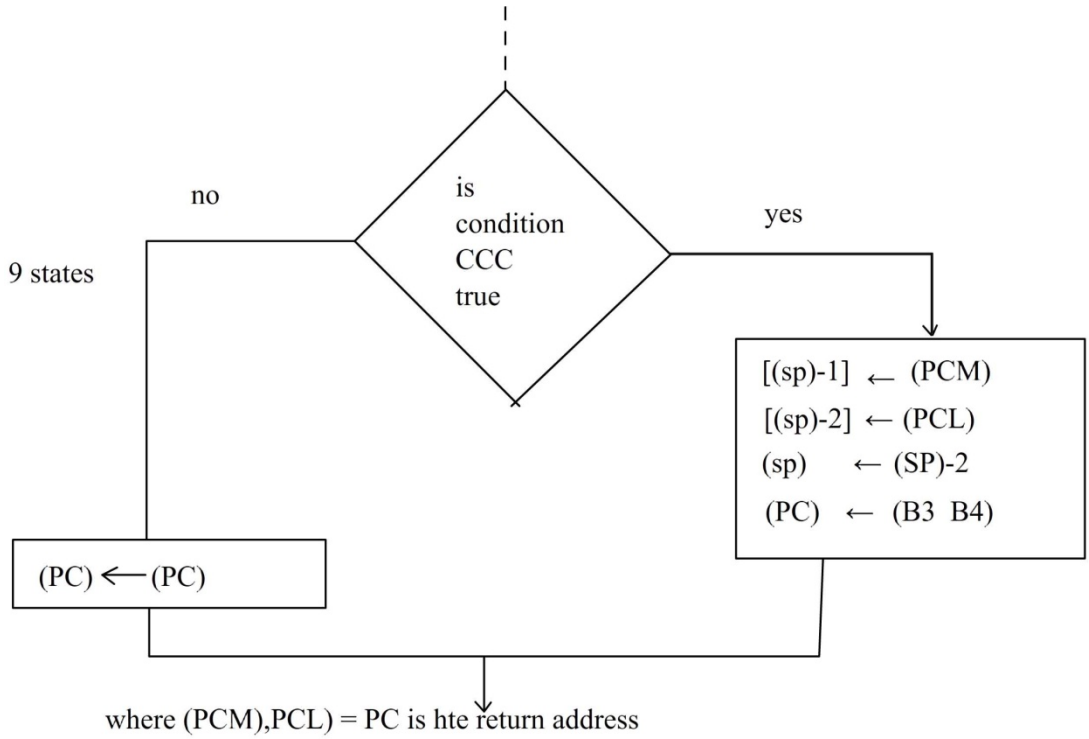
4) C cend ADDR (condition call):

This is an ALP statement, this is also 3-byte instruction, 2nd and 3rd byte give the address of the subroutine when this instruction is executed, the μp jumps to the subroutine if the condition tested is TRUE. 2f the condition is

not true then μp goes to execute the next instruction the instruction format is,



This has 8 variations for CCC, 000 to 111 the corresponding instructions are CNZ, CZ, CNC, CC, CPO, CPE, CP, CM the macro RTL implemented is shown in Fig.



If has immediate addressing mode Δ register indirect addressing mode.

If the specified condition is true, the execution specified in the CALL

Instruction are performed otherwise control continues sequentially. The micro RTL flow is,

MC - 1

OFMC T_1 : AD_7- $AD_0 \leftarrow$ (PCL) , $A_{15} - A_8 \leftarrow$ (PCH), ALE = 

IO/$\overline{M}$ = 0 T_2 : $\overline{RD}$ = 0, (PC) $\leftarrow$ (PC)+1, AD_7- $AD_0 \leftarrow$ M(AB)

S_1 = 1 T_3 : $\overline{RD}$ = 1, ↑. (IR) $\leftarrow$ (AD_7- AD_0)

S_0 = 1 T_4 : C cend = 1

$\begin{cases} T_5 \\ T_6 \end{cases}$: (sp) of condition is $\leftarrow$ (sp) - 1

MC - 2

MRMC T_1 : AD_7- $AD_0 \leftarrow$ (PCL) , $A_{15} - A_8 \leftarrow$ (PCH), ALE = 

IO/$\overline{M}$ = 0 T_2 : $\overline{RD}$ = 0, (PC) $\leftarrow$ (PC)+1, AD_7- $AD_0 \leftarrow$ M(AB)

S_1 = 1 T_3 : $\overline{RD}$ = 1, ↑. (Z) $\leftarrow$ (AD_7- AD_0)

S_0 = 1

MC - 3

MRMC T_1 : AD_7- $AD_0 \leftarrow$ (PCL) , $A_{15} - A_8 \leftarrow$ (PCH) ,ALE = 

IO/$\overline{M}$ = 0 T_2 : $\overline{RD}$ = 0, (PC) $\leftarrow$ (PC)+ 1, (AD_7- AD_0) $\leftarrow$ M(AB)

S_1 = 1 T_3 : $\overline{RD}$ = 1, ↑. (W) $\leftarrow$ (AD_7- AD_0)

S_0 = 1

MC - 4

MRMC T_1 : AD_7- $AD_0 \leftarrow$ (SPL) , $A_{15} - A_8 \leftarrow$ (SPH) ,ALE = 

IO/$\overline{M}$ = 0 T_2 : $\overline{WR}$ = 0, (SP) $\leftarrow$(SP)-1 (AD_7- AD_0) $\leftarrow$ (PCH),

S_1 = 1 T_3 : $\overline{WR}$ = 1, ↑. M(SP) $\leftarrow$ (AD_7- AD_0) ,

S_0 = 1

MC - 5

MWCMC T_1 : AD_7- $AD_0 \leftarrow$ (SPL) , $A_{15} - A_8 \leftarrow$ (SPH) ,ALE = 

IO/$\overline{M}$ = 0 T_2 : $\overline{WR}$ = 0, (AD_7- AD_0) $\leftarrow$ (PCL),

$S_1 = 1$ T_3 : $\overline{WR} = 1, \uparrow$. $M(AB) \leftarrow (AD_7 - AD_0)$,

$S_0 = 1$

$T_1 : A_{15} - A_8 \leftarrow (W)$, $AD_1 - AD_0 \leftarrow (Z)$,ALE

FEO $T_2 : (PC) \leftarrow (WZ) + 1$,

Thus if condition is true it requires 18 states and otherwise 9 states are required.

5) RET (Return):

This is an ALP statement, stands for RETURN. The meaning OS return to the main program from the subroutine unconditionally, obviously the instruction should be a part of the subroutine program. This is a single byte instruction the operation code format is,

11 CCC 10 0	N = $C9_H$

The macro RTL implemented is,

(PCL)← M(SP)

(PCH)← M[(sp) + 1]

(sp) ← (sp)+2

When this instruction is executed the 16 bit, address data available at the top of the stack shall be loaded into the (PC) and stack print is readjusted a that it again print to the top of the stack the content of the memory location whose address is specified in register SP is moved to the low order 8 bits of the memory location whose address is one more than the content of register SP register is moved to the high order 8 bits of pc, the content of the register SP is incremented by 2. 2f is for the used to set to it that the proper RETURN ADDR is available correctly on the top of the stack before asking the μ p to execute the RET instruction

The micro RTL flow is,

MC - 1

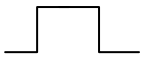
OFMC T_1 : AD_7- AD_0 ← (PCL) , A_{15} – A_8← (PCH) , ALE = 

IO/$\overline{M}$ = 0 T_2 : $\overline{RD}$ = 0, (PC) ← (PC)+1, AD_7- AD_0 ← M(AB)

S_1 = 1 T_3 : $\overline{RD}$ = 1, ↑. (IR) ← (AD_7- AD_0)

S_0 = 1 T_4 : RET = 1

MC - 2

MRMC T_1 : AD_7- AD_0 ← (SPL) , A_{15} – A_8← (SPH) , ALE = 

IO/$\overline{M}$ = 0 T_2 : $\overline{RD}$ = 0, (SP) ← (SP)+1, AD_7- AD_0 ← M(AB)

S_1 = 1 T_3 : $\overline{RD}$ = 1, ↑. (PCL) ← (AD_7- AD_0)

S_0 = 1

MC - 3

MRMC T_1 : AD_7- AD_0 ← (SPL) , A_{15} – A_8← (PCH) ,ALE = 

IO/$\overline{M}$ = 0 T_2 : $\overline{RD}$ = 0, (SP) ← (SP)+ 1, (AD_7- AD_0) ← M(AB)

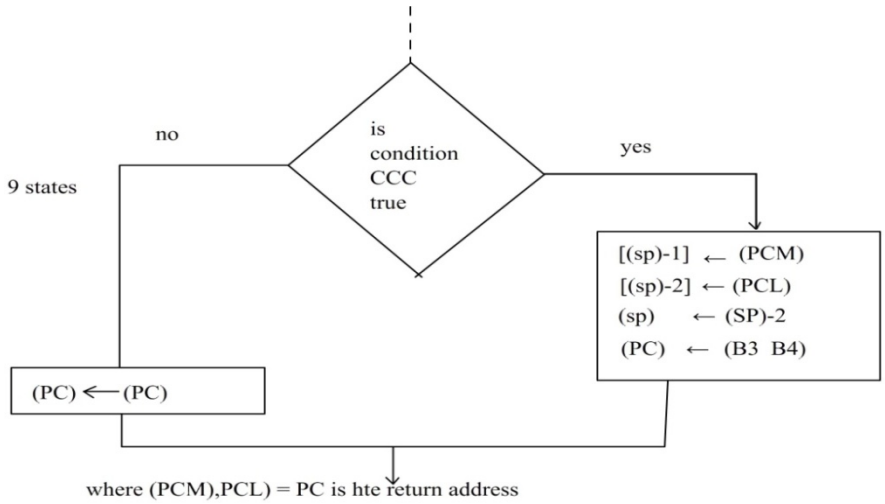
S_1 = 1 T_3 : $\overline{RD}$ = 1, ↑. (CH) ← (AD_7- AD_0)

S_0 = 1

Thus it requires 3m/c cycles and 10states, for 2MH_3 internal clock the time required is 5 μ sec, the address mode is register indirect.

Rn: This is a conditional return statement, if is also a part of the subroutine. Whenever this instruction is executed μ p checks up the condition (condition flags).

If the condition is true then the μ p returns to the main program by loading the PC with the return address stored at the top of the stack of the conditional is not true then the next instruction is the subroutine will be executed. The macro RTL Implemented is shown as a flow chart.



This is a single byte instruction the OP code is

11 C C C 0 0 0	N
Next instruction	N + 1

There are 8 variations in this statement depending upon CCC. They are RNZ, RZ, RNC, RC, RPD, RPE, RP and RM. The addressing mode is register indirect because the return address is available in the memory location pointed by SP the micro RTL flow is given.

MC - 1

OFMC T_1 : AD_7- AD_0 ← (PCL) , A_{15} – A_8← (PCH), ALE = ⎍

IO/$\overline{M}$ = 0 T_2 : $\overline{RD}$ = 0, (PC) ← (PC)+1, AD_7- AD_0 ← M(AB)

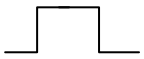
S_1 = 1 T_3 : $\overline{RD}$ = 1, ↑. (IR) ← (AD_7- AD_0)

S_0 = 1 T_4 : R cond = 1

$\begin{cases} T_5 \\ T_6 \end{cases}$: 2f (ccc) = true teen go for MC_2 8 MC 3 else, go for MC_1

Of the next instruction.

MC - 2

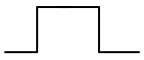
MRMC T_1 : AD_7- $AD_0 \leftarrow (SPL)$, $A_{15} - A_8 \leftarrow (SPH)$,ALE = 

IO/$\overline{M}$ = 0 T_2 : $\overline{RD}$ = 0, (SP) ← (SP)+1, AD_7- AD_0 ← M(AB)

S_1 = 1 T_3 : $\overline{RD}$ = 1, ↑. (PCL) ← (AD_7- AD_0)

S_0 = 1

MC - 3

MRMC T_1 : AD_7- $AD_0 \leftarrow (SPL)$, $A_{15} - A_8 \leftarrow (SPH)$,ALE = 

IO/$\overline{M}$ = 0 T_2 : $\overline{RD}$ = 0, (SP) ← (SP)+ 1, (AD_7- AD_0) ← M(AB)

S_1 = 1 T_3 : $\overline{RD}$ = 1, ↑. (PCH) ← (AD_7- AD_0)

S_0 = 1

Thus if the conditions is true it needs 12 states otherwise 6 states.