Lecture-20

(11) LDAX rp: This is an ALP statement LDAX is the mnemonic for LOAD THE ACCUMULATOR INDIRECTLY. The alphabet x in the mnemonic is for tells that a register pair is involved in the instruction. Rp is known as operant field. The meaning of the instruction is load the accumulator from the memory location whose address is available in register pair only one operand in involved in this instruction & the operand is available in the memory location. Whose address is a register pair the macro RTL implements shall be

$$(A) \leftarrow H(rpH, rpL)$$

This is a single byte instruction. The instruction format is

00 RP1 010	N

There are two variations in this instruction RP =00 for (B, C) pair and RP= 0 form DE pair note that RP=10 and 11 are not allowed in this instruction. The micro RTL is

MC – 1	
OFMC	$T1: AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (PCH),\ ALE =$
$IO/\overline{M} = 0$	$T2: \overline{RD} = 0, (PC) \leftarrow (PC) + 1,\ AD_7 - AD_0 \leftarrow M(AB)$
S1 =1	$T3: \overline{RD} = 1, \uparrow, (IR) \leftarrow (AD_7 - AD_0)$
S0 =1	$T4: LDAX rp = 1$
MC – 2	
MRMC	$T1: AD_7 - AD_0 \leftarrow (rpL),\ A_{15} - A_8 \leftarrow (rpH),\ ALE =$
$IO/\overline{M} = 0$	$T2: \overline{RD} = 0, (PC) \leftarrow (PC) + 1,\ AD_7 - AD_0 \leftarrow M(AB)$
S1 =1	$T3: \overline{RD} = 1, \uparrow, (A) \leftarrow (AD_7 - AD_0)$
S0 =0	

This instruction requires 2 m/c cycles OFMC & MRMC and 7 states. It needs 3.5 μsec using 2MHz clock. The addressing mode is register indirect addressing mode.

(12) STAX rp: This is an mnemonic for STAX accumulator indirectly using register indirect addressing mode. The meaning of the instruction is the content of the accumulator should be moved to the memory location whose address is available in register pair. The macro RTL implemented shall be

$M(rpH, rpL) \leftarrow (A)$. This is a single byte instruction. The instruction format is

00 RP0 010	N

Here also only two variations RP=00 and 01 are allowed. The micro RTL flow is

$MC-1$
OFMC
$IO/\overline{M}=0$
$S1=1$
$S0=1$

T1: $AD_7-AD_0 \leftarrow (PCL)$, $A_{15}-A_8 \leftarrow (PCH)$, ALE=
T2: $\overline{RD}=0, (PC) \leftarrow (PC)+1$, $AD_7-AD_0 \leftarrow M(AB)$
T3: $\overline{RD}=1, \uparrow$, $(IR) \leftarrow (AD_7-AD_0)$
T4: STAX rp = 1

$MC-2$
MWRMC
$IO/\overline{M}=0$
$S1=0$
$S0=1$

T1: $AD_7-AD_0 \leftarrow (rpL)$, $A_{15}-A_8 \leftarrow (rpH)$, ALE=
T2: $\overline{WR}=0$, $AD_7-AD_0 \leftarrow (A)$
T3: $\overline{WR}=1, \uparrow$, $M(AB) \leftarrow (AD_7-AD_0)$

It requires only 2 m/c cycles OFMC & MWRMC and 7 states. It needs 3.5μsec using 2MHz clock.

IN PORT & OUT PORT:

Data is transferred from the microprocessor to an output device in to the transfer and from an input device to the microprocessor in an input transfer. Output devices certain one or more register each of which is addressable and strobe by the MP to the latched data on the data bus at the appropriate time during an output transfer. Input devices contain a register the MP and an addressable three-state

buffer that is enabled by a strobe from the Mp at the appropriate time to place data on data bus.

The 8085 A CPU outputs a signal IO/$\overline{M}$ which is 1 when an I/0 port is being accessed and O when memory is being accessed. This can be used to distinguish between I/O & memory READ & WRITE operations 2f IO/$\overline{M}$ =1 is used to select any I/O port than it is known as I/O mapped I/O structure or isolated I/O, 2f IO/$\overline{M}$ =0 is used to select any I/o port then system will not distinguish between I/O & memory. An I/O port will then be treated as just another memory.

Location:

This is referred to as memory mapped I/O. In this case, same of the GK addressable locations are used to identify the I/O port & not memory.

IN PORT:

This is an ALP statement port is the symbolic name given to Q-kit address of the input device available as a 2nd byte of the instruction. In this the mnemonic for INPUT. The meaning of the instruction is an 8 kit data from the output device. Whose address is available as a 2nd byte of the instructions is loaded into the accumulator, the macro RTL implemented is,

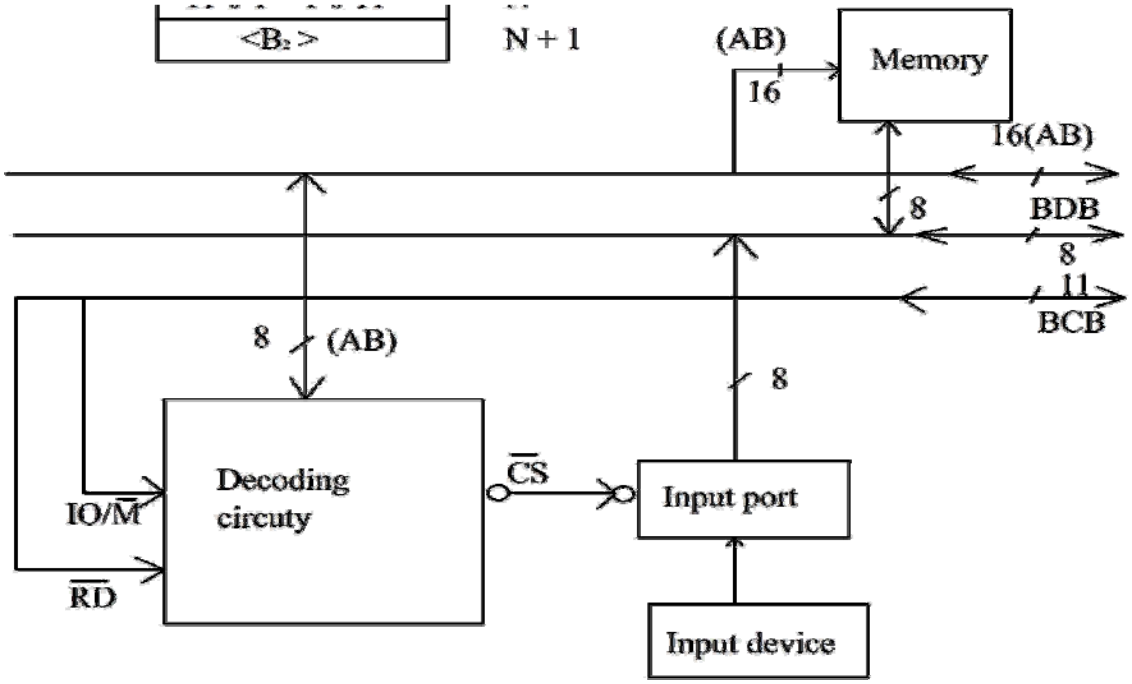
(A) ← I/O (port)

(A) ← I/O (<B_2>)

The necessary interfering circuitry between MP & the input device is shows below for inputting an 8-bit data from an input device whose port address is B_2 the Instructions format is,

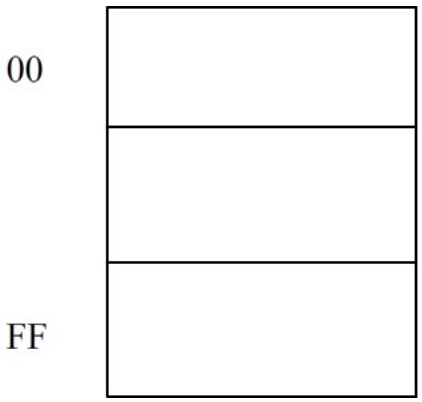
This is a 2 byte instruction. The instruction format is

11 011 011	N
<B_2>	N+1



The data generated by an i9nput device is stored temporarily in some register which can be used by the MP when necessary 2n order to place the contents of the input register and the MP system bus, the outputs the connected to the data bus through a three, state input instructions places an Q- bit devices address at the address bus, where it is duplicated an higher & lower order bus An external decoder decodes the device address, the IO/$\overline{M}$, & the $\overline{RD}$ pulse in order to generate an input device select pulse state buffer, the addressed input part's three state buffer, thus placing the input port's data an the data bus.

The IN port is a2- byte instructions, the first byte is the OP code and the second byte is the 8-bit input device address. The address may be any varying from 00 to FF. Thus , a total of 256 input devices can be connected directly, through updated I/O structure, where the source register to identified by an explicit 8-bit address, the corresponding I/O structure is shown by the map.



The micro RTL flow for executing this instruction is as follows:

MC- 1 OFMC T_1 : AD,- AD ← (PCL) , A_{15} – A_8← (PCH), ALE =

IO/$\overline{M}$ = 0 T_2 : $\overline{RD}$ = 0, (PC) ← (PC) + 1, AD_1- AD_0 ← M(AB)

S_1 = 1 T_3 : $\overline{RD}$ = 1, ↑. (IR) ← (AD_7- AD_0)

S_0 = 1 T_4 : IN = 1

Mc – 2 MRMC

IO/$\overline{M}$ = 0 T_1 : AD_1- AD_0 ← (PCL), ΔD_5 – A_8← (PCH),ALE =

S_1 = 1 T_2 : $\overline{RD}$ = 0, (PC) ← (PC) + 1, AD_1- AD_0 ← M(AB)

S_0 = 1 T_3 : $\overline{RD}$ = 1, ↑. (W) ← (AD_7- AD_0) (Z) ← (AD_7- AD_0)

Mc–3 IORMC T_1 : AD_7- AD_0 ← (Z), ΔD_5 – A_8← (W), ALE =

IO/$\overline{M}_2$ T_2 : $\overline{RD}$ = 0, (AD,-AD) ← A_0(Y,Y_0 Y, Y_0)

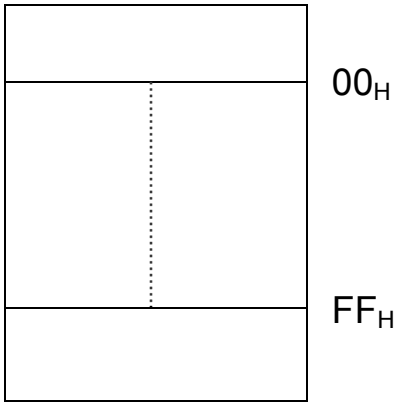
S_1 = 1 T_3 : $\overline{RD}$ = 1, ↑. (A) ← (AD_7- AD_0)

S_0 = 1

Thus at the end of 2nd m/c cycle W register together shall certain

(Y,Y_0 Y, Y_0), where Y, Y_0 it is the 2nd byte data happen to be the address.

Whenever an input device is interface as shown in fig 12, and the data is inputted using IN PORT instruction. It is known as I/O mapped I/O structure or isolated I/O structure. The input device address can be any 8 bits dependently upon the user varying from 00_H to FF_H . thus a total of 256 input devices can be connected directly through isolated I/O structure. The corresponding I/O space is shown by map in fig 13.



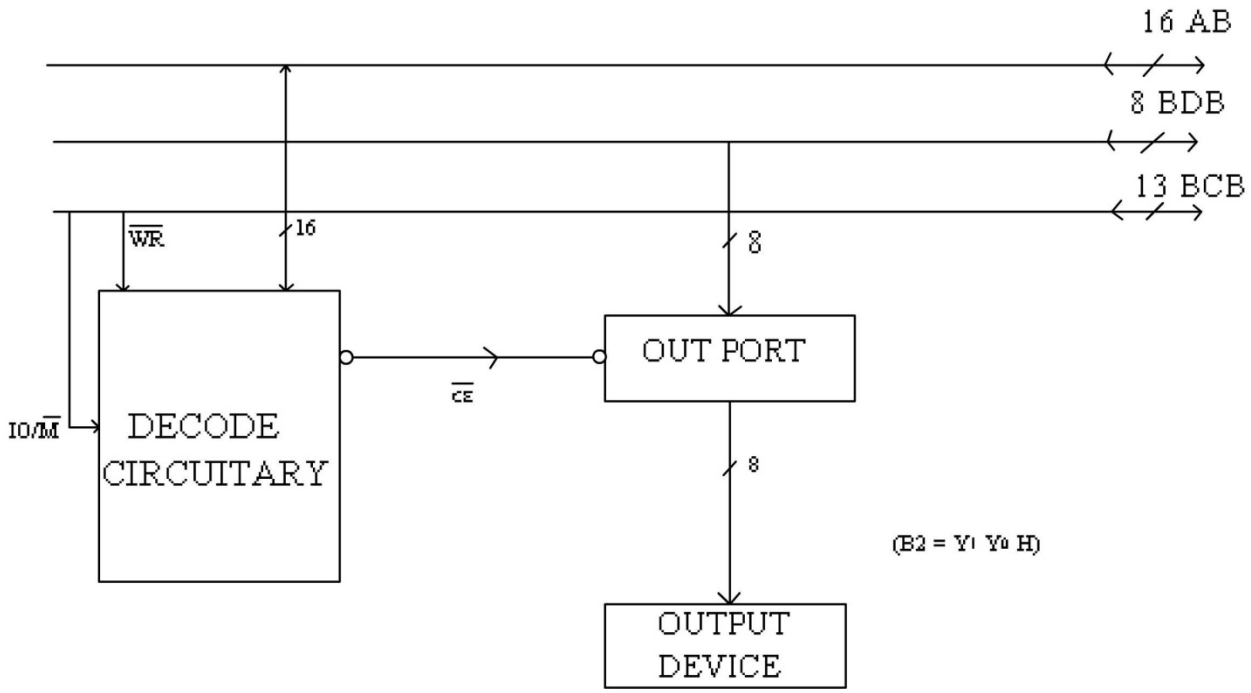
$IO/\overline{M}=1$

$S1 = 1$`

$S0 = 0$

$\overline{RD}=0$

(14) <u>OUT PORT :</u> This is an ALP statement fig 14 given the interfacing circuitry for outputting an 8 bit data into an output device whose address is the symbolic name PORT in the output instruction OUTPORT.



OUTPORT is a 2 byte instruction. PORT is the symbolic name given to the address of the output device available as the 2nd byte of instruction. The instruction format is

110 100 11	N
<B_2>	N+1

The meaning is the content of the accumulator is outputted to the output device whose address is the 2nd byte of the instruction. The macro RTL implemented should be

$$I/O(PORT) \leftarrow (A)$$

or

$$I/O(B_2) \leftarrow (A)$$

It is directed addressing mode and has no variations. The micro RTL flow is

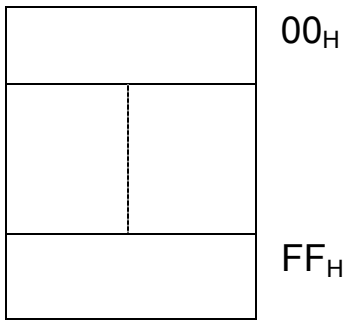
MC−1	
OFMC	T1: $AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (PCH),\ ALE =$
$IO/\overline{M} = 0$	T2: $\overline{RD} = 0,\ (PC) \leftarrow (PC) + 1,\ AD_7 - AD_0 \leftarrow M(AB)$
$S1 = 1$	T3: $\overline{RD} = 1, \uparrow,\ (IR) \leftarrow (AD_7 - AD_0)$
$S0 = 1$	T4: $OUTPORT = 1$

MC−2	
MRMC	T1: $AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (PCH),\ ALE =$
$IO/\overline{M} = 0$	T2: $\overline{RD} = 0,\ (PC) \leftarrow (PC) + 1,\ AD_7 - AD_0 \leftarrow M(AB)$
$S1 = 1$	T3: $\overline{RD} = 1, \uparrow,\ (Z) \leftarrow (AD_7 - AD_0)\ \&\ (W) \leftarrow (AD_7 - AD_0)$
$S0 = 0$	

Thus address is duplicated.

MC−3	
IOWRMC3	T1: $AD_7 - AD_0 \leftarrow (rpL),\ A_{15} - A_8 \leftarrow (rpH),\ ALE =$
$IO/\overline{M} = 1$	T2: $\overline{WR} = 0,\quad AD_7 - AD_0 \leftarrow (A)$
$S1 = 0$	T3: $\overline{WR} = 1, \uparrow,\ M(AB) \leftarrow (AD_7 - AD_0)$
$S0 = 1$	

Thus it requires 3m/c cycles OFMC, MRMC & IOWRMC and total 10 states. It needs 5μsec using 2 MHz internal clock. If the output device is interfaced for communications using this instruction then the structure is known as isolated I/O structure I/O structure or I/O map I/O structure. We can address directly 256 output devices addressed from 00_H to FF_H. Shown in fig19a.



$IO/\overline{M}=0$

$\overline{WB}=0$

$(AB)=(B_0,B_1)H$

$=(Y_1Y_0Y_1Y_0)H$

fig 14 a output I/O space

(15) XCHG: This is an ALP statement. This is a single byte instruction. The meaning is the contents of (H, L) register pair is exchanged with the contents of (D,E) pair. The macro RTL implemented is

$$(H) \leftarrow (D)$$
$$(L) \leftarrow (E)$$
or
$$(H,L) \leftrightarrow (D,E)$$

The single byte operation CODE IS

11	10	10
11		

N

The micro RTL flow is

$MC-1$

$OFMC$

$IO/\overline{M}=0$

$S1=1$

$S0=1$

$T1: AD_7-AD_0 \leftarrow (PCL),\ A_{15}-A_8 \leftarrow (PCH),\ ALE=$

$T2: \overline{RD}=0, (PC) \leftarrow (PC)+1,\ AD_7-AD_0 \leftarrow M(AB)$

$T3: \overline{RD}=1, \uparrow, (IR) \leftarrow (AD_7-AD_0)$

$T4: XCHG=1, (H,L) \leftrightarrow (D,E)$