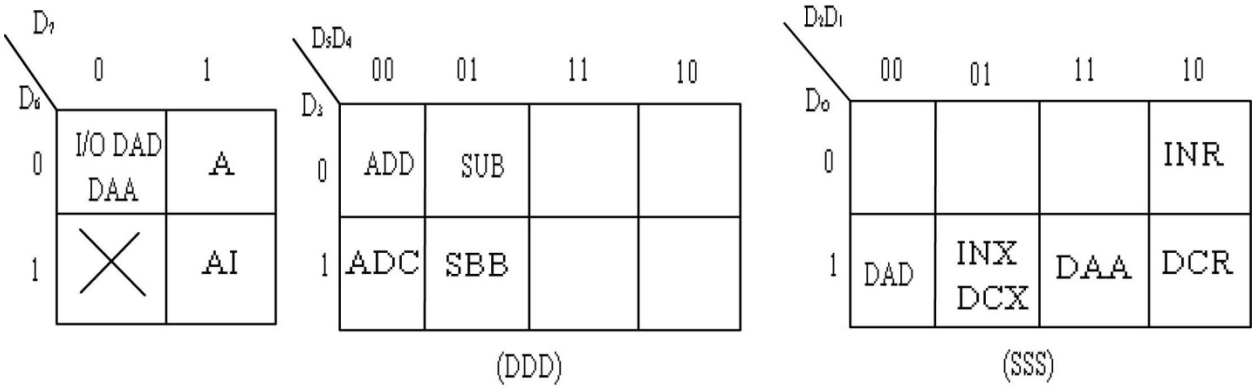
Lecture-21

2) ARITHMETIC GROUP: This group perform the arithmetic operation on the operands normally the operands are necessary for any arithmetic operation one of the operand is always seen in the accumulator the other operand can be seen in one of the three positions.(a) an internal general purpose register (r) .

(b) In a memory location pointed by M pointer (H, L) pair.

(c) Immediately in the instruction itself as a 2nd byte.

All of the flags are effected as per standard rule. The format of the operation code is shown in fig 15.



There are 20 basic instructions in this group.

(1)ADD v: The macro RTL implemented is

$$(A) \leftarrow (A)+(v)$$

This is a single byte instruction. The meaning is add the content of register (v) to the content of accumulator and store it back to the accumulator. The operation code is 10 000 SSS. It has 7 variations. The micro RTL flow is given below:

MC – 1
OFMC
$IO/\overline{M}=0$
S1 =1
S0 =1

T1: $AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (PCH),\ ALE=$
T2: $\overline{RD}=0, (PC) \leftarrow (PC)+1,\ AD_7 - AD_0 \leftarrow M(AB)$
T3: $\overline{RD}=1, \uparrow, (IR) \leftarrow (AD_7 - AD_0)$
T4: $(A) \leftarrow (A) + (v)$

It requires single m/c cycle OFMC requiring 4 states. It is register addressing mode.

(2) ADD M: The macro RTL implemented is

$$(A) \leftarrow (A) + M(H, L)$$

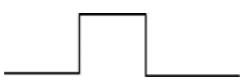
This is a single byte instruction. The meaning is add the content of memory location whose address is in (H, L) pair to the content of accumulator and store it back to the accumulator. The operation code is 10 000 110 or 86_H. It has no variations. It is register indirect addressing mode. The micro indirect addressing mode. The micro RTL flow is given below,

MC – 1
OFMC
$IO/\overline{M}=0$
S1 =1
S0 =1

T1: $AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (PCH),\ ALE=$
T2: $\overline{RD}=0, (PC) \leftarrow (PC)+1,\ AD_7 - AD_0 \leftarrow M(AB)$
T3: $\overline{RD}=1, \uparrow, (IR) \leftarrow (AD_7 - AD_0)$
T4: ADD M=1

MC – 2
MRMC
$IO/\overline{M}=0$
S1 =1
S0 =0
FEO

T1: $AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (PCH),\ ALE=$
T2: $\overline{RD}=0, (PC) \leftarrow (PC)+1,\ AD_7 - AD_0 \leftarrow M(AB)$
T3: $\overline{RD}=1, \uparrow, (TEMP) \leftarrow (AD_7 - AD_0), (A) \leftarrow (A) + (TEMP) FEO$



IT requires two m/c cycle OFMC, MRMC, and 7 state.

(3) ADI DATA: It is a two byte instruction. The second operand is seen in the instruction itself. The operation code is

11 000 110	N
$<B_2>$	N+1

The macro RTL implemented is

$$(A) \leftarrow (A) + < B_2 >$$

The meaning of the instruction is add the content available as the second byte of the instruction to the content of accumulation and store the result back to the accumulator. It has no variations and it is immediate addressing mode. The micro RTL flow is,

$MC-1$
OFMC
$IO/\overline{M}=0$
$S1=1$
$S0=1$

$T1: AD_7-AD_0 \leftarrow (PCL),\ A_{15}-A_8 \leftarrow (PCH),\ ALE=$
$T2: \overline{RD}=0, (PC) \leftarrow (PC)+1,\ AD_7-AD_0 \leftarrow M(AB)$
$T3: \overline{RD}=1, \uparrow, (IR) \leftarrow (AD_7-AD_0)$
$T4: ADI\ DATA\ \ M=1$

$MC-2$
MRMC
$IO/\overline{M}=0$
$S1=1$
$S0=0$

$T1: AD_7-AD_0 \leftarrow (PCL),\ A_{15}-A_8 \leftarrow (PCH),\ ALE=$
$T2: \overline{RD}=0, (PC) \leftarrow (PC)+1,\ AD_7-AD_0 \leftarrow M(AB)$
$T3: \overline{RD}=1, \uparrow, (TEMP) \leftarrow (AD_7-AD_0),\ (A) \leftarrow (A)+(TEMP)$
FEO

(4) ADC v: The meaning of the instruction is add the content of register (v) to the content of accumulator with carry. The macro RTL implemented is

$$(A) \leftarrow (A) + (v) + (cy)$$

It is a single byte instruction. The opcode is 10 001 SSS. It has 7 variations. It is register addressing mode. The micro RTL flow is

MC – 1	$T1: AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (PCH),\ ALE =$
OFMC	$T2: \overline{RD} = 0, (PC) \leftarrow (PC) + 1,\ AD_7 - AD_0 \leftarrow M(AB)$
$IO/\overline{M} = 0$	$T3: \overline{RD} = 1, \uparrow, (IR) \leftarrow (AD_7 - AD_0)$
S1 = 1	$T4: (A) \leftarrow (A) + (v) + (cy)$
S0 = 1	FEO

It requires one m/c cycle OFMC and 4 states.

(5) <u>ADC M:</u> The meaning of the instruction is add the contents of memory location whose address is in (H, L) pair to the contents of accumulator with carry, the macro RTL implemented is

$$(A) \leftarrow (A) + M(H, L) + (cy)$$

It is a single byte instruction. The opcode is 10 001 110. It has no variation. It is register indirect addressing mode. The micro RTL flow is-

MC – 1	$T1: AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (PCH),\ ALE =$
OFMC	$T2: \overline{RD} = 0, (PC) \leftarrow (PC) + 1,\ AD_7 - AD_0 \leftarrow M(AB)$
$IO/\overline{M} = 0$	$T3: \overline{RD} = 1, \uparrow, (IR) \leftarrow (AD_7 - AD_0)$
S1 = 1	T4: ADC M M=1
S0 = 1	
MC – 2	$T1: AD_7 - AD_0 \leftarrow (L),\ A_{15} - A_8 \leftarrow (H),\ ALE =$
OFMC	$T2: \overline{RD} = 0,\ AD_7 - AD_0 \leftarrow M(AB)$
$IO/\overline{M} = 0$	$T3: \overline{RD} = 1, \uparrow, (TEMP) \leftarrow (AD_7 - AD_0)$
S1 = 1	$(A) \leftarrow (A) + (TEMP) + (cy)$
S0 = 0	FEO

It requires two m/c cycles and 7 states

(6) <u>ACI DATA:</u> The meaning of the instruction is add the content available the second byte of instruction itself to the content to accumulator with carry

and store the result back to the accumulator. It is a two byte instruction. The opcode is

11 001 110	N
<B_2>	N+1

The macro RTL implemented is

$$(A) \leftarrow (A) + (B_2) + (cy)$$

It has no variations. It is immediate addressing mode. The micro RTL flow is

MC – 1
OFMC
$IO/\overline{M} = 0$
S1 = 1
S0 = 1

T1: $AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (PCH),\ ALE =$
T2: $\overline{RD} = 0,\ (PC) \leftarrow (PC) + 1,\ AD_7 - AD_0 \leftarrow M(AB)$
T3: $\overline{RD} = 1, \uparrow,\ (IR) \leftarrow (AD_7 - AD_0)$
T4: $ACI\ DATA = 1$

MC – 2
MRMC
$IO/\overline{M} = 0$
S1 = 1
S0 = 0

T1: $AD_7 - AD_0 \leftarrow (L),\ A_{15} - A_8 \leftarrow (H),\ ALE =$
T2: $\overline{RD} = 0,\ (PC) \leftarrow (PC) + 1,\ AD_7 - AD_0 \leftarrow M(AB)$
T3: $\overline{RD} = 1, \uparrow,\ (TEMP) \leftarrow (AD_7 - AD_0)$
$(A) \leftarrow (A) + (TEMP) + (cy)$
FEO

It require two m/c cycles OFMC & MRMC and 7 states.

(7) SUB v: The meaning of the instruction is subtract the content of register from the content of accumulator and stored the result back into accumulator. The macro RTL implemented is

$$(A) \leftarrow (A) - (v)$$

It is a single byte instruction. The operation code is 10 010 SSS. It has 7 variations. It is register addressing mode.

The micro RTL flow is

MC – 1	T1: $AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (PCH),\ ALE =$
OFMC	T2: $\overline{RD} = 0, (PC) \leftarrow (PC) + 1,\ AD_7 - AD_0 \leftarrow M(AB)$
$IO/\overline{M} = 0$	T3: $\overline{RD} = 1, \uparrow, (IR) \leftarrow (AD_7 - AD_0)$
S1 = 1	T4: SUB v = 1 (A) ← (A) – (V)
S0 = 1	FEO

It requires one m/c cycles OFMC and 4 cycles.

(8) SUB M: The meaning of the instruction is subtract the content of the memory location. Whose address is in (H, L) pair from the content of accumulator and store the result back in the accumulator. The macro RTL flow is

$$(A) \leftarrow (A) - M(H, L)$$

It is a single byte instruction. The operation code is 10 010 110. It has no variation. It is register indirect address mode. The micro RTL flow is.

MC – 1	T1: $AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (PCH),\ ALE =$
OFMC	T2: $\overline{RD} = 0, (PC) \leftarrow (PC) + 1,\ AD_7 - AD_0 \leftarrow M(AB)$
$IO/\overline{M} = 0$	T3: $\overline{RD} = 1, \uparrow, (IR) \leftarrow (AD_7 - AD_0)$
S1 = 1	T4: SUB M = 1
S0 = 1	

MC – 2	T1: $AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (PCH),\ ALE =$
MRMC	T2: $\overline{RD} = 0,\ AD_7 - AD_0 \leftarrow M(AB)$
$IO/\overline{M} = 0$	T3: $\overline{RD} = 1, \uparrow, (TEMP) \leftarrow (AD_7 - AD_0)\ (A) \leftarrow (A) - (TEMP)$
S1 = 1	FEO
S0 = 1	

It requires two m/c cycle OFMC and MRMC and 7 states.

(9) SUI DATA: The meaning of the instruction is subtraction the content available as a second byte of instruction from the content of accumulator and

store the result back in the accumulator. It is a two byte instruction. The operation code is

11 010 110	N
$<B_2>$	N+1

The macro RTL implemented is

$$(A) \leftarrow (A) - < B_2 >$$

It has no variation. It is immediate addressing mode. The micro RTL implemented is

MC−1
OFMC
IO / $\overline{M}$ = 0
S1 =1
S0 =1

T1: $AD_7 - AD_0 \leftarrow (PCL)$, $A_{15} - A_8 \leftarrow (PCH)$, ALE =
T2: $\overline{RD} = 0, (PC) \leftarrow (PC) + 1$, $AD_7 - AD_0 \leftarrow M(AB)$
T3: $\overline{RD} = 1, \uparrow$, $(IR) \leftarrow (AD_7 - AD_0)$
T4: SUI DATA = 1

MC−2
MRMC
IO / $\overline{M}$ = 0
S1 =1
S0 =0

T1: $AD_7 - AD_0 \leftarrow (PCL)$, $A_{15} - A_8 \leftarrow (PCH)$, ALE =
T2: $\overline{RD} = 0$, $AD_7 - AD_0 \leftarrow M(AB)$
T3: $\overline{RD} = 1, \uparrow$, $(TEMP) \leftarrow (AD_7 - AD_0)$ $(A) \leftarrow (A) - (TEMP)$
FEO

It require two m/c cycles OFMC, MRMC and 7 states

(10) SBB v: The meaning of the instruction is subtract the content of register from the content of accumulator with borrow and store the result back in the accumulator. The macro RTL implemented is

$$(A) \leftarrow (A) - (v) - (cy)$$

It is a single byte instruction the operation code is 10011 SSS. It has 7 variation. It is register addressing mode. The micro RTL flow is

MC−1 OFMC $IO/\overline{M}=0$ S1 =1 S0 =1	T1: $AD_7-AD_0 \leftarrow (PCL),\ A_{15}-A_8 \leftarrow (PCH),\ ALE=$ T2: $\overline{RD}=0, (PC) \leftarrow (PC)+1,\ AD_7-AD_0 \leftarrow M(AB)$ T3: $\overline{RD}=1, \uparrow, (IR) \leftarrow (AD_7-AD_0)$ T4: SBBv = 1

It require one m/c cycle OFMC and 4 states

(11) SBB M: The meaning of the instruction is subtract the content of memory location whose address is in (H,L) pair with from the content of accumulator with barrows and store the result back in the accumulator. The macro RTL implemented is

$$(A) \leftarrow (A) - M(H,L) - (cy)$$

It is a single byte instruction. The operation code is 10 011 110. It has no variation. It is a register indirect address mode. The micro RTL flow is

MC−1 OFMC $IO/\overline{M}=0$ S1 =1 S0 =1	T1: $AD_7-AD_0 \leftarrow (PCL),\ A_{15}-A_8 \leftarrow (PCH),\ ALE=$ T2: $\overline{RD}=0, (PC) \leftarrow (PC)+1,\ AD_7-AD_0 \leftarrow M(AB)$ T3: $\overline{RD}=1, \uparrow, (IR) \leftarrow (AD_7-AD_0)$ T4: SBB M = 1
MC−2 MRMC $IO/\overline{M}=0$ S1 =1 S0 =0	T1: $AD_7-AD_0 \leftarrow (PCL),\ A_{15}-A_8 \leftarrow (PCH),\ ALE=$ T2: $\overline{RD}=0,\ AD_7-AD_0 \leftarrow M(AB)$ T3: $\overline{RD}=1, \uparrow, (TEMPR) \leftarrow (AD_7-AD_0)\ (A) \leftarrow (A)-(TEMP)$ FEO

It require two m/c cycles OFMC and MRMC and 7 states.

(12) SBI DATA: The meaning of the instruction is subtract the content available as a second byte of the instruction from from content of accumulator with barrow and store the result back in accumulator. It is a two byte instruction. The operation code is

11 011 110	N
<B_2>	N+1

It has no variations. It is immediate addressing mode. The micro RTL flow is

MC – 1
OFMC
IO / $\overline{M}$ = 0
S1 = 1
S0 = 1

T1: $AD_7 - AD_0 \leftarrow (PCL)$, $A_{15} - A_8 \leftarrow (PCH)$, ALE =
T2: $\overline{RD} = 0, (PC) \leftarrow (PC) + 1$, $AD_7 - AD_0 \leftarrow M(AB)$
T3: $\overline{RD} = 1, \uparrow, (IR) \leftarrow (AD_7 - AD_0)$
T4: SBI DATA = 1

MC – 2
MRMC
IO / $\overline{M}$ = 0
S1 = 1
S0 = 0

T1: $AD_7 - AD_0 \leftarrow (PCL)$, $A_{15} - A_8 \leftarrow (PCH)$, ALE =
T2: $\overline{RD} = 0, (PC) \leftarrow (PC) + 1, AD_7 - AD_0 \leftarrow M(AB)$
T3: $\overline{RD} = 1, \uparrow, (TEMPR) \leftarrow (AD_7 - AD_0) (A) \leftarrow (A) - (TEMP) - (cy)$
FEO

It requires two m/c 7 states.

Note: In all these above instruction all the flow are affected as per rule.