Lecture-22

(13) INR v: The meaning of the instruction is incremented the content of register v by 1 and store it back to the register r. the macro RTL implemented is

$$(v) \leftarrow (v) + 1$$

The operation code is 00 DDD 100. It is a single byte instruction. It is register addressing mode. It has 7 variations in this all the flags are affected except carry flag. The micro RTL flow is

MC−1	T1: $AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (PCH), ALE =$
OFMC	T2: $\overline{RD} = 0, (PC) \leftarrow (PC) + 1,\ AD_7 - AD_0 \leftarrow M(AB)$
$IO/\overline{M} = 0$	T3: $\overline{RD} = 1, \uparrow, (IR) \leftarrow (AD_7 - AD_0)$
S1 =1	T4: INRv = 1 (TEMP) ← v, (v) ← (TEMPp)a
S0 =1	

It require one M/C OFMC and 4 state

(14) INR M: The meaning of the instruction is increment the content of memory location by 1 whose address available in (H, L) pair and store the result back in the same location. The macro RTL implemented is

$$M(H, L) \leftarrow M(H, L) + 1$$

It is a single byte instruction. The operation code is 00 110 100. It has no variations. It is register indirect addressing mode. The micro RTL flow is

MC−1	T1: $AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (PCH), ALE =$
OFMC	T2: $\overline{RD} = 0, (PC) \leftarrow (PC) + 1,\ AD_7 - AD_0 \leftarrow M(AB)$
$IO/\overline{M} = 0$	T3: $\overline{RD} = 1, \uparrow, (IR) \leftarrow (AD_7 - AD_0)$
S1 =1	T4: INR M = 1
S0 =1	

MC − 2	
MRMC	T1: $AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (PCH),\ ALE =$
$IO/\overline{M} = 0$	T2: $\overline{RD} = 0,\ AD_7 - AD_0 \leftarrow M(AB)$
S1 = 1	T3: $\overline{RD} = 1, \uparrow,\ (TEMP) \leftarrow (AD_7 - AD_0),\ (ALU) - (TEMP) + 1$
S0 = 0	

MC − 3	
MWRMC3	T1: $AD_7 - AD_0 \leftarrow (L),\ A_{15} - A_8 \leftarrow (H),\ ALE =$
$IO/\overline{M} = 0$	T2: $\overline{WR} = 0,\quad AD_7 - AD_0 \leftarrow (A)$
S1 = 0	T3: $\overline{WR} = 1, \uparrow,\ M(AB) \leftarrow (AD_7 - AD_0)$
S0 = 1	

It requires 3 m/c cycles OFMC, MRMC, MWRMC, and 10 states.

(15) DCR v: the meaning of the instruction is decremented of register v by one and content result back in the register. The macro RTL implemented is

$(v) \leftarrow (v) - 1$

It is a single byte instruction. The operation code is 00 DDD 101. It has 7 variation. It is a register direct addressing mode. The micro RTL flow is

MC − 1	
OFMC	T1: $AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (PCH),\ ALE =$
$IO/\overline{M} = 0$	T2: $\overline{RD} = 0, (PC) \leftarrow (PC) + 1,\ AD_7 - AD_0 \leftarrow M(AB)$
S1 = 1	T3: $\overline{RD} = 1, \uparrow,\ (IR) \leftarrow (AD_7 - AD_0)$
S0 = 1	T4: DCR v = 1, $(v) \leftarrow (v) - 1$

It require one cycle OFMC and 4 states.

(16) DCR M: The meaning of the instruction is decremented the content of memory location whose address is stored in (H, L) pair by the same location. The macro RTL implemented is

$M(H,L) \leftarrow M(H,L)$

It is a single byte instruction. The operation code is 00 110 101. It has no variation. It is a register indirect addressing mode. The micro RTL flow is

$MC-1$
OFMC
$IO/\overline{M}=0$
S1 =1
S0 =1
T1: $AD_7-AD_0 \leftarrow (PCL),\ A_{15}-A_8 \leftarrow (PCH),\ ALE=$
T2: $\overline{RD}=0, (PC) \leftarrow (PC)+1,\ AD_7-AD_0 \leftarrow M(AB)$
T3: $\overline{RD}=1, \uparrow, (IR) \leftarrow (AD_7-AD_0)$
T4: DCR M = 1

$MC-2$
MRMC
$IO/\overline{M}=0$
S1 =1
S0 =0
T1: $AD_7-AD_0 \leftarrow (L),\ A_{15}-A_8 \leftarrow (H),\ ALE=$
T2: $\overline{RD}=0, AD_7-AD_0 \leftarrow M(AB)$
T3: $\overline{RD}=1, \uparrow, (TEMP) \leftarrow (AD_7-AD_0),\ (ALU)-(TEMP)-1$

$MC-3$
MWRMC
$IO/\overline{M}=0$
S1 =0
S0 =1
T1: $AD_7-AD_0 \leftarrow (L),\ A_{15}-A_8 \leftarrow (H),\ ALE=$
T2: $\overline{WR}=0,\quad AD_7-AD_0 \leftarrow (A)$
T3: $\overline{WR}=1, \uparrow, M(AB) \leftarrow (AD_7-AD_0)$

It require three m/c cycles and 10 states. In above 4 instructions and 10 states. In above 4 instructions all flag are affected except CY.

(17) <u>INX rp:</u> The meaning of the instruction is incremented the register pair (rp) implemented is

$(rp) \leftarrow (rp)+1$

It is a single byte instruction. The operation code is 00 RP 0011. It has 4 variations. It is register addressing mode. The micro RTL flow is

MC–1	T1: $AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (PCH), ALE =$
OFMC	T2: $\overline{RD} = 0, (PC) \leftarrow (PC) + 1,\ AD_7 - AD_0 \leftarrow M(AB)$
$IO/\overline{M} = 0$	T3: $\overline{RD} = 1, \uparrow, (IR) \leftarrow (AD_7 - AD_0)$
$S1 = 1$	T4: INX RP = 1, $(rpH) \leftarrow (rpL) + 1$
$S0 = 0$	T5 : T6 : IF $(rpL = 00H), (rpH) \leftarrow (rpH) + 1$
	ELSE NOTHING

It require one m/c cycle OFMC and 6 states.

(18) <u>DCX rp:</u> The meaning of the instruction is decrement the register pair (rp) together by1. The macro RTL implemented is

$(rp) \leftarrow (rp) - 1$

MC–1	T1: $AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (PCH), ALE =$
OFMC	T2: $\overline{RD} = 0, (PC) \leftarrow (PC) + 1,\ AD_7 - AD_0 \leftarrow M(AB)$
$IO/\overline{M} = 0$	T3: $\overline{RD} = 1, \uparrow, (IR) \leftarrow (AD_7 - AD_0)$
$S1 = 1$	T4: INX RP = 1, $(rpL) \leftarrow (rpL) - 1$
$S0 = 0$	T5 : T6 : IF $(rpL) = FFH), (rpH) \leftarrow (rpH) - 1$
	ELSE NOTHING

It requires one m/c cycle OFMC and 6 states. In above two instructions no flag is affected.

(19) <u>DAD rp:</u> The meaning is double precision addition is add the content of (H,L) pair to the content of register pair (rp) and store the result back is in the (H,L) pair. The macro RTL implemented in

$(H, L) \leftarrow (H, L) + (rpH, rpL)$

Only the CY flag is effected as per rule. It is a single byte instruction. The operation code is 00 RP 1001. It has memory is needed, if the opcode is read from the memory therefore it goes into bus m/c cycle because to requires 10 states even single byte instruction. The micro RTL flow

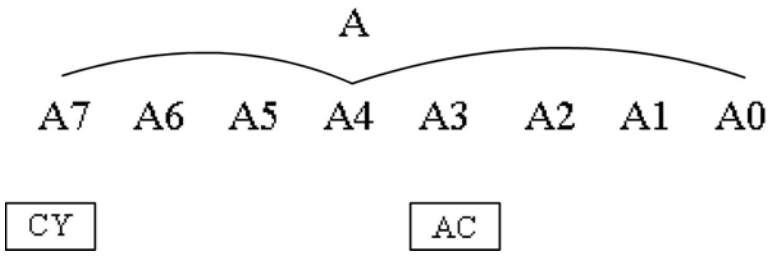
MC−1 OFMC $IO/\overline{M}=0$ S1 =1 S0 =0	T1: $AD_7-AD_0 \leftarrow (Z+1),\ A_{15}-A_8 \leftarrow (W),\ ALE=$ T2: $\overline{RD}=0,\ (PC) \leftarrow (PC)+1,\ AD_7-AD_0 \leftarrow M(AB)$ T3: $\overline{RD}=1, \uparrow,\ (IR) \leftarrow (AD_7-AD_0)$ T4: DAD rp = 1
MC−2 BIMC $IO/\overline{M}=0$ S1 =0 S0 =1	T1: (W) ← (A), (Z) ← (PR) T2: (A) ← (rpL), (TEMP) ← (rpL) T3: (L) ← (L) + (rpL) (cy flag is SET or RESET)
MC−3 BIMC $IO/\overline{M}=0$ S1 =0 S0 =1 $\overline{RD}=1$	T1: (A) ← (rpH), (TYR) ← (rpH) T2: (H) ← (H) + 1, (rpH) + CY T3: (A) ← (W) + (PR) ← (S, ZAC, P)

This requires 3 m/c cycles OFMC and two BIMC.

DAD H: This statement means $(H,L) \leftarrow (H,L)+(H,L)$

The meaning of this multiplying the 10 byte content of (H,L) by 2. It actually shift all the 16 bits content of (H, L) to left by one bit position.

(20) <u>DAA:</u> Meaning is decimal adjust accumulator. It is specifically used for BCD addition operation. It adjusts the content of accumulator to two bit BCD. It performs the following operation on 8 bit data in the accumulator.



When DAD is executed:

(1) if the lower order 4 bits A_3 A_2 A_1 A_0 is an illegal BCD code or if AC is SET then 06_H is added to accumulator.

(2) thereafter if the higher order 4 bits A_7 A_6 A_5 A_4 is an illegal BCD code or if CY is SET then 60_H is added to accumulator else no action. It is a single byte instruction. The operation code is 00100111 or 27_h. it has no variations. The micro RTL flow is

$MC-1$	$T1: AD_7 - AD_0 \leftarrow (PCL),\ A_{15} - A_8 \leftarrow (PCH),\ ALE =$
OFMC	$T2: \overline{RD} = 0,\ (PC) \leftarrow (PC) + 1,\ (AD_7 - AD_0) \leftarrow M(AB)$
$IO/\overline{M} = 0$	$T3: \overline{RD} = 1, \uparrow,\ (IR) \leftarrow (AD_7 - AD_0)$
$S1 = 1$	$T4: DAD\ M = 1$
$S0 = 1$	FEO
	Adjust A & flags