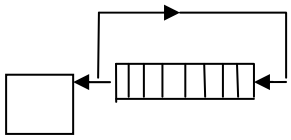
Lecture-24

13) RLC: This is an ALP statement. The macro RTL implemented is,

$(A_0 + 1) \leftarrow (A_1)$ $\quad 0 = 0$ to 6
$(A_0) \leftarrow (A_7)$
$(CY) \leftarrow (A_7)$



The meaning of the instruction is not the left the content of the accumulator by one bit the lower order bit & the CY flag are both set to the value shifted out the high order bit position. Only the CY flag is affected. The operation code is,

1 0 1 0 1 S S S	N	07_4

If has no variations. The addressing mode is implied addressing mode the macro RTL flow is,

OFMC $\quad T_1 : AD_7\ AD_0 \leftarrow (PCL)$, $A_{15} - A_8 \leftarrow (PCH)$, ALE =
IO/$\overline{M}$ = 0 $\quad T_2 : \overline{RD} = 0,$ $\quad (PC) \leftarrow (PC)$ H, AD_7- $AD_0 \leftarrow$ M(AB)
$S_1 = 1$ $\quad T_3 : \overline{RD} = 1,$ $\quad (IR) \leftarrow (AD_7 - AD_0)$
$S_0 = 1$ $\quad T_4 : RLC = 1,$ $\quad (ALV) \leftarrow (A)$

Mc – 2 $\quad T_1 :$ FEO (rotate left)
$T_2 : (A) \leftarrow (ALV)$;

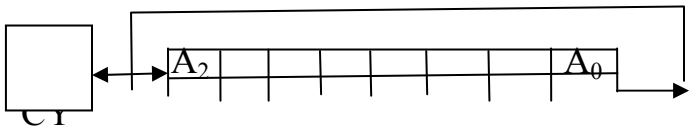
Therefore, one M/C cycle OFMC of 4 states is required. This instruction is used to check any

14) RRC: This is an ALP statement the macro RTL implemented is

$(A_i) \leftarrow (A_i + 1)$ $\quad i = 0$ to 6

$(A_7) \leftarrow (A_0)$, $\quad (CY) \leftarrow (A_0)$

The content of the accumulator is rotate right by one bit position as shown In fig



The high order bit & the Cy flag can both set to the value of shifted out of the low order bit position only the Cy flag is affected the operation is

1 0 1 0 1 1 1 1 1	N is OF_m

If has no variations. Only OFMC of 4 states is required. The addressing mode is register and implied addressing mode.

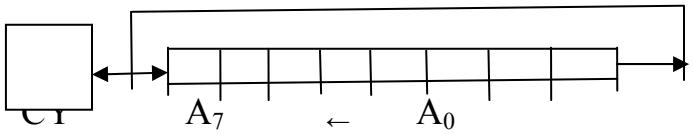
15) RAL: (Rotate left through carry), this is an ALP statement the macro RTL implemented is,

$(A_i + 1) \leftarrow (A_i)$ $\quad i = 0$ to 6

$(CY) \leftarrow (A_7)$,

$(A_0) \leftarrow (CY)$

The content of the accumulator is rotate left one position through the CY flag. The low order bit is set equal to the CY flag. The CY flag is set to the value shifted out of the A_7 bit as shown in fig



Only the CY flag is affected the operation code is

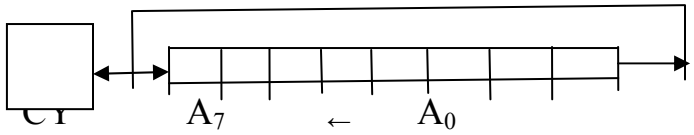
1 0 1 0 1 1 1 1 1	N = 17_H

If has no variations, the addressing mode is implied addressing mode. Only one M/C cycle OFMC of 4 states is required.

16) RAR: (Rotate accumulator right through carry), this is an ALP statement the macro RTL implemented is,

$(A_i) \leftarrow (A_i + 1)$ $\quad i = 0$ to 6
$(CY) \leftarrow (A_0)$,
$(A_7) \leftarrow (CY)$

The content of the accumulator is rotate right one bit position through the CY flag. The high order bit is set equal to the CY flag and The CY flag is set to the value shift$_{10}$ out of the A_0 only the flag is affected.



The operation code is,

0 0 0 1 1 1 1 1 1	=	$(IF)_H$

This is a single byte instruction. The M/C cycles required is only one OFMC- 4 the addressing mode is implied addressing mode.

17) CMA: (complement accumulator), this is an ALP statement; the macro RTL implemented is,

$(A) \leftarrow (\overline{A})$

The content of the accumulator is complemented bit by bit and the result is stored back into the acc no flags are affected, the operation code is,

0 0 0 1 1 1 1 1 1	N=	$2F_H$

It is a single byte instruction & no variation. The addressing mode is implied addressing mode requires one M/C- 4.

18) CMC: (complement carry), this is an ALP statement, and the macro RTL implemented is,

(CY) ← ($\overline{CY}$)

The CY flag is complement and it is stored back into the same CY flag position. The operation code is,

0 0 1 1 1 1 1 1 1 1	=	$(3F)_H$

It is a single byte instruction & no variation. 2f this no other flags are affected, it requires the M/C cycle OFMC-4.

T_4: CMC = 1, (ALU) ← (CY)

FEO : FEO, ALU ← ($\overline{CY}$)

(CY) ← (ALU)

Therefore only 4 states are required.

19) STC: (set carry), the macro RTL is,

(EY) ← 1

The carry flag is set to 1 and no others flags are affected, the operation code is,

0 0 1 1 0 1 1 1	N=	$3T_4$

It has no variation. 2f requires one M/C cycle of - 4 states only. i.e. OFMC- 4.

Branch group:

This group of instructions are used to alter the normal required flaw and for the program to proceed from a different point. Conditions flags are

not affected by any instruction in this group only PC is affected; sometimes stretch also comes into picture. Branch instruction can be of two types conditional & unconditional. Unconditional branch instruction simply cause the program to branch to the indicated instruction whenever it is encountered is PC is located with a new address conditional branch instructions examine the stares of one of the four processor flags (Z, CY, P, S) to determine if the specified tested is TRUE, it causes is not used for specifying condition the 8 conditions that are tested are given below.

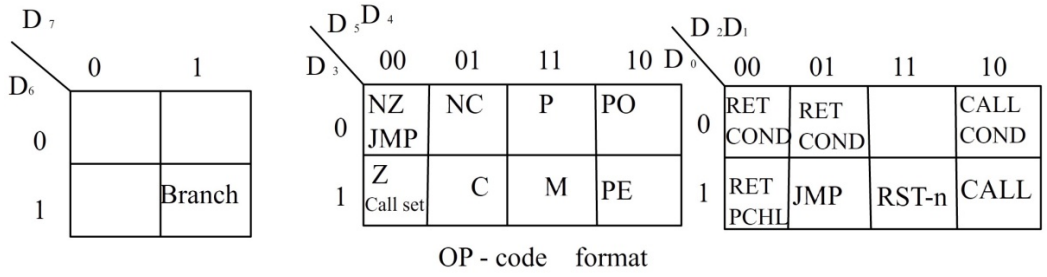
Conditions		flag tested	identification code CCC
NZ	not zero	Z = 0	000
Z	zero	Z = 1	001
NC	not carry	CY = 0	010
C	carry	CY = 1	011
PO	parity odd	P = 0	100
PE	parity even	p = 1	101
P	plus	S = 0	110
M	minus	S = 1	111

2f Z = 0 is not true, then NZ is true

Z = 0 is true, and then NZ is not true.

The identification code CCC when involved in an instruction shall be seen on the bit $D_5D_4D_3$ of the operation code

There are 8 basic operations in this group the operation code format is shown,

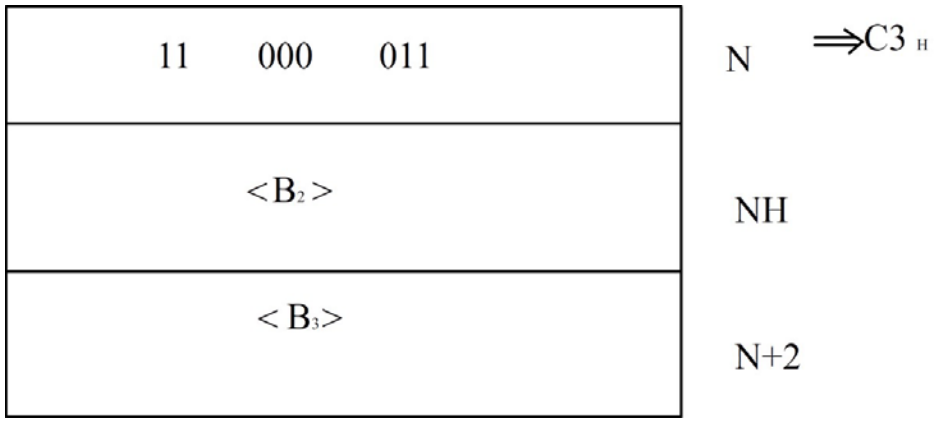


OP - code format

JMP Δ DDR:

This is an ALP statement Δ DDR is the symbolic name given to the 16- bit address data available as the second & the third byte of the instruction. JMP is the mnemonic for jump the meaning of the instruction is

load the PC with the 16- bit data available in the instruction itself so that he next instruction is fetched cycle. This is a 3 –byte instruction the instruction formed being.

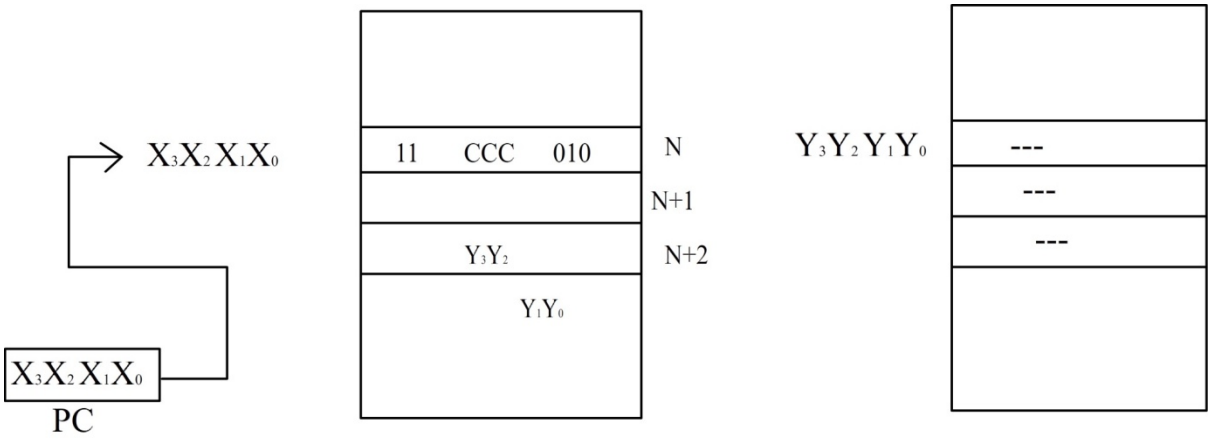


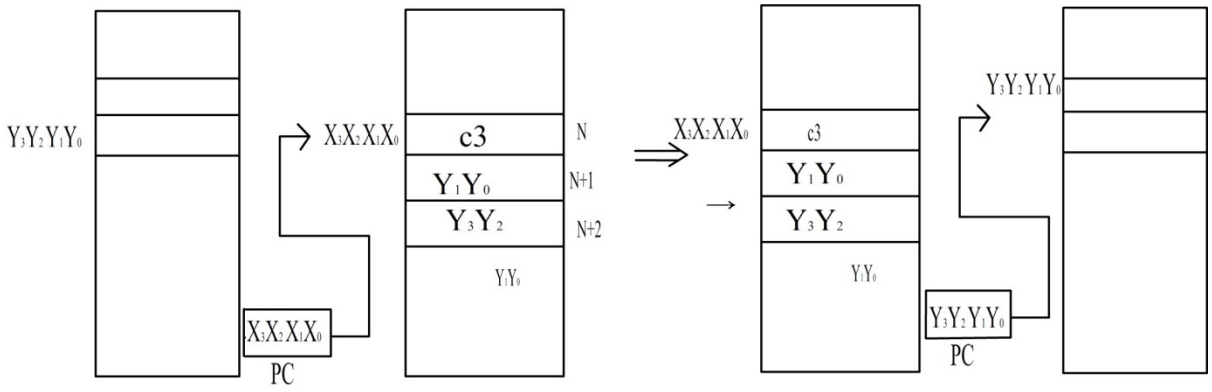
The macro RTL implemented is

(PCH) ← < B_3 >

(PCL) ← < B_2 >

Conditions before & after the execution of JM addr instruction are shown below.





The macro RTL flow is as shown below.

MC - 1

OFMC T_1 : AD_1 AD_0 ← (PCL) , A_{15} – A_8← (PCH), ALE =

IO/$\overline{M}$ = 0 T_2 : $\overline{RD}$ = 0, (PC) ← (PC)+1, AD_7- AD_0 ⇐

M(AB)

S_1 = 1 T_3 : $\overline{RD}$ = 1, ↑. (IR) ← (AD_7- AD_0)

S_0 = 1 T_4 : instruction is decoded JMP = 1

MC - 2

MRMC T_1 : AD_1 AD_0 ← (PCL) , A_{15} – A_8← (PCH), ALE =

IO/$\overline{M}$ = 0 T_2 : $\overline{RD}$ = 0, (PC) ← (PC)+1, AD_7- AD_0 ←

M(AB)

S_1 = 1 T_3 : $\overline{RD}$ = 1, ↑. (Z) ← (AD_7- AD_0)

S_0 = 1

MC - 3

MRMC T_1 : AD_1 AD_0 ← (PCL) , A_{15} – A_8← (PCH), ALE =

IO/$\overline{M}$ = 0 T_2 : $\overline{RD}$ = 0, (PC) ← (Z), (AD_7- AD_0) ← M(AB)

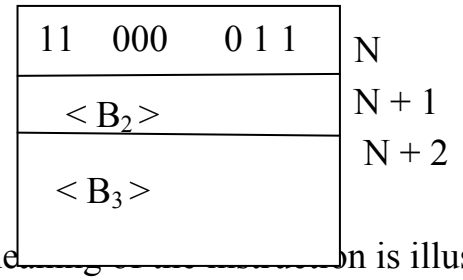
S_1 = 1 T_3 : $\overline{RD}$ = 1, ↑. (PCH) ← (AD_7- AD_0)

S_0 = 1 W FEO =WZ+1 Wz → pc ^{wt}

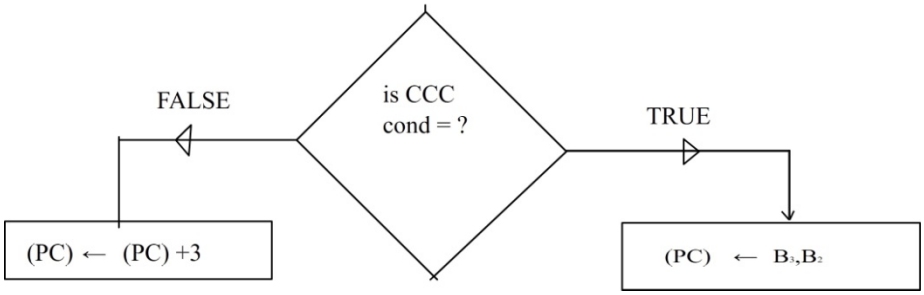
Thus, it requires three machine cycle OFMC, MRMC & MRMC and total 10 states using a 2 MH_3 internal clock it requires 5μ sec. No variation in this instruction. The addressing the mode in their case is immediate

addressing mode because the 16 bit address data is immediately in the instruction itself to be loaded into the PC.

2. J cend ADDR: There are 8 variations for this instructions depending upon the conditions to be tested. They are JNZ, JZ, JNC, JC, JPO, JPF, JP, and JM. This is also an ALP statement. This is a 3 byte instruction the operation code format is,



The me[illegible]n is illustrated in the flow chart



Where (PC) = $(X_3X_2X_1X_0)4$ just at the start of instruction exit.

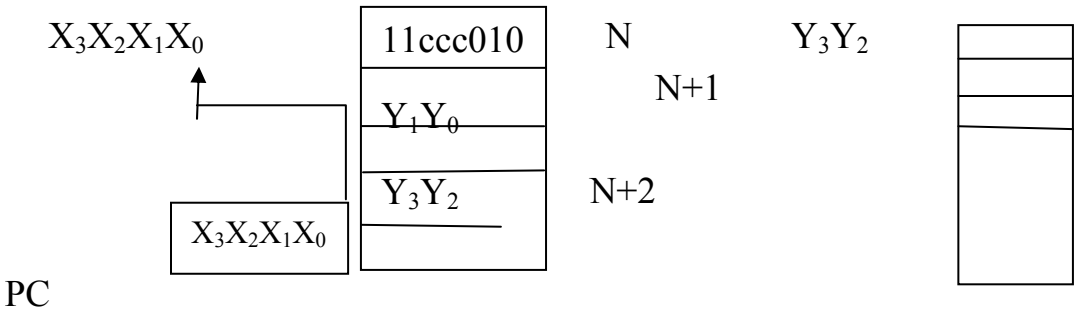


Fig shows the condition existing just before the stand of instruction cycle J cend ADDR the IC, b address in the PC just often the end of the instruction cycle depends upon the condition to be tested PC will be loaded

with B_3B_2 if the given condition is TRUE, otherwise (PC) will go to (PC) where (PC) shall be the address $X_3X_2X_1X_0$ which points to the operation code 11 CCC 010. The micro RTL flow given below.

MC - 1

OFMC T_1 : AD_1 AD_0 ← (PCL) , A_{15} – A_8← (PCH), ALE =

IO/$\overline{M}$ = 0 T_2 : $\overline{RD}$ = 0, (PC) ← (PC)+1, AD_7- AD_0 ← M(AB)

S_1 = 1 T_3 : $\overline{RD}$ = 1, ↑. (IR) ← (AD_7- AD_0)

S_0 = 1 T_4 : J cond = 1

MC - 2

MRMC T_1 : AD_1 AD_0 ← (PCL) , A_{15} – A_8← (PCH) , ALE =

IO/$\overline{M}$ = 0 T_2 : $\overline{RD}$ = 0, (PC) ← (PC)+1, AD_7- AD_0 ← M(AB)

S_1 = 1 T_3 : $\overline{RD}$ = 1, ↑. (Z) ← (AD_7- AD_0)

S_0 = 1 if condition = true, go to MC-3 else (PC) ←(PC) + 1

MC - 3

MRMC T_1 : AD_1 AD_0 ← (PCL) , A_{15} – A_8← (PCH) ,ALE =

IO/$\overline{M}$ = 0 T_2 : $\overline{RD}$ = 0, (PCL) ← (Z), (AD_7- AD_0) ← M(AB)

S_1 = 1 T_3 : $\overline{RD}$ = 1, ↑. (PCH) ← (AD_7- AD_0)

S_0 = 1 W FEO =WZ+1 Wz → pc ^{wt}

Therefore if the condition is true it takes 10 states to get instruction executed 2f the condition is not true then it takes 7 states for the instruction to be executed. The addressing mo0de is immediate addressing mode Z and no flags affected.