Introduction to Timer-2 in 8052

Adapted from 8052 datasheet

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Timer 2 Modes

89C5131 device has timer 2 because it is 8052 architecture. Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is updated every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency. This section briefly explains the modes.
Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON. For details of timer 2 modes, refer datasheet of 8052 microcontroller.

- Auto-reload Mode: This mode provides 16 bit counter with auto-reload mode. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin. In count up mode, TH2 and TL2 increments upto 0FFFFH and then sets the TF2 bit upon overflow. Overflow causes the timer registers to be reloaded with the 16 bit value in RCAP2H and RCAP2L. In count down mode, the timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.
- Baud rate generator: Timer 2 can be configured to provide Rx clock and Tx clock in this mode.
- Capture Mode: In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt.
  If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt.

Timer-2 Configuration

Control and status bits are contained in registers T2CON and T2MOD for Timer 2. Following are brief details about Timer-2 registers.

T2MOD: Address of the register is 0C9H. It is byte addressable.

T2MOD Register

Bit No.	7	6	5	4	3	2	1	0
Bit Name	-	-	-	-	-	-	T2OE	DCEN

- T2OE: Timer 2 Output Enable bit.
- DCEN: When set, this bit allows Timer 2 to be configured as an up/down counter.

T2CON: Address of the register is 0C8H. It is bit addressable.

T2CON Register

Bit No.	7	6	5	4	3	2	1	0
Bit Name	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
Bit Addr	CF	CE	CD	CC	CB	CA	C9	C8

- TF2: Set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1
- EXF2: Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
- RCLK: Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
- TCLK:Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock
- EXEN2: Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX
- TR2: Start/Stop control for Timer 2. TR2 = 1 starts the timer
- C/T2: Timer or counter select for Timer 2. C/T2 = 0 for timer function. C/T2 = 1 for external event counter (falling edge triggered).
- CP/RL2: Capture/Reload select. CP/RL2 = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/RL2 = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow

INTERRPUPT

To enable interrupts for timer 2, we have to do -

SETB EA ; (or SETB IE.7) To enable interrupts
SETB ET2; (or SETB IE.5) To enable interrupts from T2

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

PROGRAMMABLE CLOCK OUT

We can use this mode to generate a PWM output in Labwork. A 50 percent duty cycle clock can be programmed to come out on P1.0 from timer 2. To generate the clock, configure the Timer/Counter 2 as a clock generator:
Bit C/T2 (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer. The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in the following equation.

$$\text{Clock-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536-(\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 roll-overs will not generate an interrupt. Following diagram shows the timer 2 hardware configuration for the programmable clock out mode.