Sounder Rajendran

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Education

- **North Carolina State University** — Raleigh, NC
  Masters of Science, Computer Engineering — *Aug 2022 - May 2024**
  Courses: ASIC and FPGA Design using Verilog, Microprocessor Architecture, Architecture of Parallel Computers
- **Coimbatore Institute of Technology** — Coimbatore, India
  Bachelor of Electrical and Electronics Engineering; CGPA: 8.23/10.0 - First class) — *Aug 2015 - April 2019*

Skills Summary

- **Languages**: Verilog, System Verilog, TCL, Perl, Python, C, C++, JS, Dart, SQL, LabVIEW, Unix scripting
- **Tools**: Synopsys, Xilinx ISE-design, Keil, Multisim, MATLAB, OpenCV, Azure IoT, ROS
- **Processors worked with**: ARM Cortex-M series, Cortex-A8 (32 bit), Cortex-A72 (Broadcom BCM2711)

Experience

- **Bosch Global Software Technologies** — Coimbatore, India
  Senior Software Engineer - IoT, HMI and Embedded Systems — *Sept 2019 - June 2022*
  - **IoT Development**: Designed Integrated IoT systems for remote accessibility and control of HMI test framework.
    Initiated RD of security threat mitigation in firmware layer of Bosch IoT gateways.
    Developed end-to-end IoT 4.0 Cyber-Physical Systems monitoring and control tool
  - **Embedded systems and HMI Development**: Proposed, designed, and developed a new generation HMI test automation framework - Closed Loop Testing of Voice and Extended Reality Systems. Designed and programmed Sensor fusion for enhanced positional data for Bosch Sensortec

Academic Projects

- **Deep Neural Network using Verilog**: Currently designing a multi-stage neural network, including a convolutional layer, a fully connected layer, and a max pooling layer for ECE 564 course under Prof. Paul Franzon
- **Cache Simulation and Memory Hierarchy Design**: Currently designing a flexible cache and memory hierarchy simulator to compare the performance, area, and energy of different memory hierarchy configurations using microbenchmarks, including write-back and write-allocate policy to update data into cache set.
- **16-bit RISC Processor using Verilog**: Designed a 16-bit RISC processor and modeled its components using Verilog. The processor is based on Harvard architecture. Adders, registers, and blocks such as ALU and memory are simulated structurally using logic gates.
- **Intelligent distributed generation in cloud-connected urban microgrids**: Designed and built a hybrid isolated micro-grid based on renewable resources to mitigate reliability threats in conventional electric grids. The grid incorporated block-chain mechanism for peer-to-peer electricity transactions and overall monitoring. Incremental conductance algorithm changes the gating pulse applied to DC/DC converter in the solar photovoltaic system.

Leadership and Volunteer work

- Active Member (Rotaract Club of NC State - 2022*)
- Innovation Champion, HMI Center of Excellence (Bosch Global Software Technologies 2020-2022)
- District Priority Projects Chairman (Rotaract Club of Coimbatore Spectrum 2020-2022)
- Board Member and Active Volunteer (Youth Red Cross, CIT 2015-2019)

Honors and Awards

- Best Student Entrepreneur Award, (CIT 2019)
- Best Project Award, Confederation of Indian Industries and JKKN educational institutions (2019)
- Runners up, EO GSEA (Global Student Entrepreneur Awards), (India Chapter, 2018)
- Outstanding Social Project Award, Rotaract South East Asia Conference Rotasia 2020-21
- Rotaract Outstanding Avenue Recognition, Rotaract South Asia Multi-District Information Organization
- Runner-up, Robot design competition Runner-up at Open Hackathon at National Technical Fest, Amrita University, 2018