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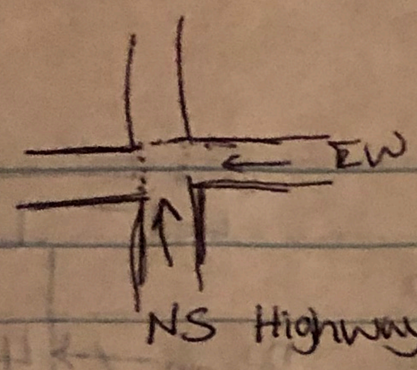
12/8/23

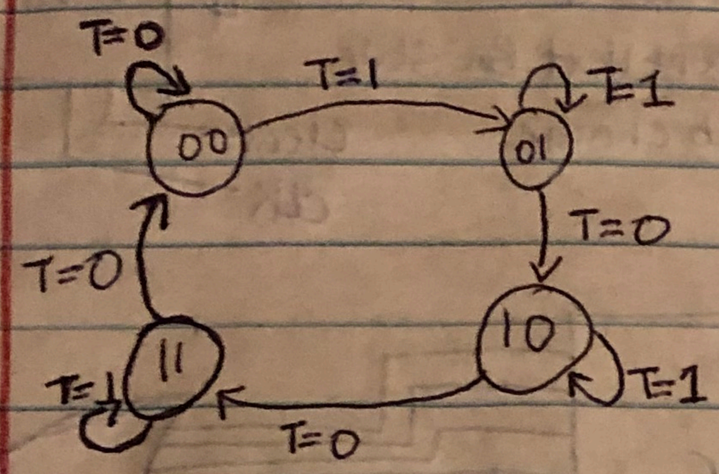
Bonus Assignment 2



R_{NS}, Y_{NS}, G_{NS} } outputs
R_{EW}, Y_{EW}, G_{EW} }
T → input

everything else off!

S_0 = NS green on, EW red on
S_1 = NS yellow on
S_2 = NS red on, EW green on
S_3 = EW yellow on



A	B	R_{NS}	Y_{NS}	G_{NS}	R_{EW}	Y_{EW}	G_{EW}
0	0	0	0	1	0	0	0
0	1	0	1	0	1	0	0
1	0	1	0	0	0	0	1
1	1	1	0	0	0	1	0

$R_{NS} = A$
$Y_{NS} = A'B$
$G_{NS} = A'B'$
$R_{EW} = A'$
$Y_{EW} = AB$
$G_{EW} = AB'$

A	B	T	A_{NH}	B_{NH}	D_A	D_B
0	0	0	0	0	0	0
0	1	0	1	0	1	0
1	0	0	1	1	1	1
1	1	0	0	0	0	0
0	0	1	0	1	0	1
0	1	1	0	1	0	1
1	0	1	1	0	1	0
1	1	1	1	1	1	1

D_A

AB \ T	0	1
00	0	0
01	1	1
11	0	1
10	1	1

$D_A = AB' + AT + A'BT'$

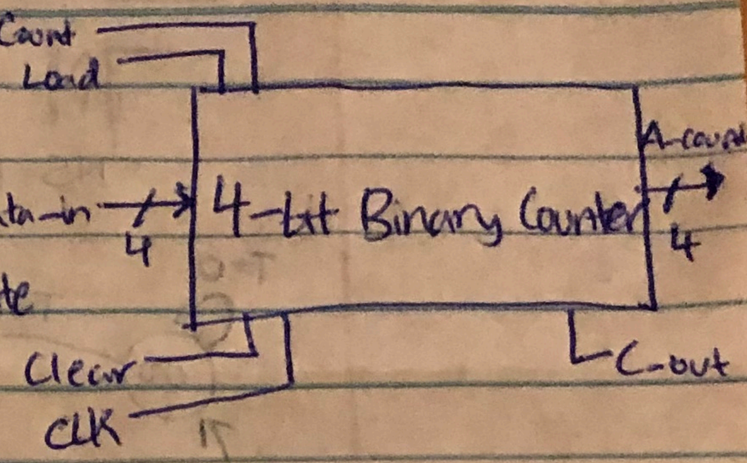
D_B

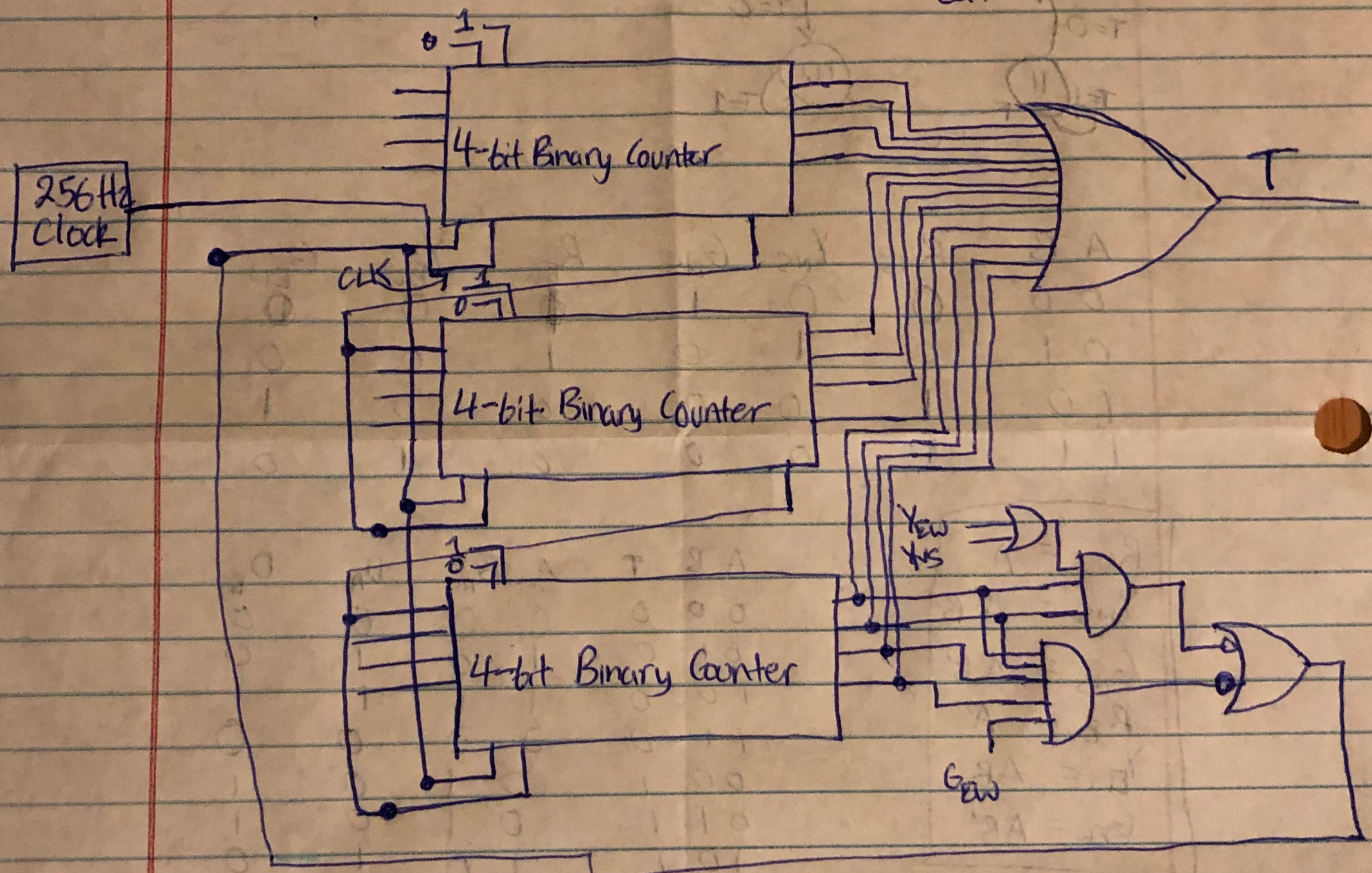
AB \ T	0	1
00	0	1
01	0	1
11	0	1
10	1	0

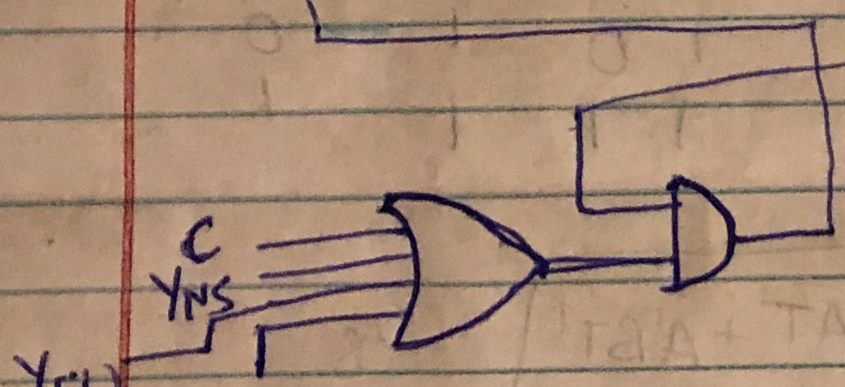
$D_B = AB'T' + A'T + BT$

Timer

Clear	CLK	Load	Count	Function
0	X	X	X	Clear to 0
1	↑	1	X	Load Inputs
1	↑	0	1	Count Next Bn. State
1	↑	0	0	No change







*Assume initial inputs is all 0.

Notes: Load=0, Count=1, This counter counts up to $256 \cdot 3 = 768 \rightarrow (0011\text{-}0000\text{-}0000)_2$ or to $256 \cdot 15 = 3840 \rightarrow (1111\text{-}0000\text{-}0000)_2$. Hence combinational logic is used around highest 4-bit counter to set clear to 0 (to transition to next state) when 3sec or 15sec is achieved depending on outputs (see previous page). T is or of all outputs.