RA8P1 Group
Renesas Microcontrollers

R01DS0439EJ0083
Rev.0.83
Apr 19, 2024

High-performance 1 GHz Arm® Cortex®-M85 core, 250 MHz Arm® Cortex®-M33 core, up to 1 MB code MRAM, and 2 MB SRAM with ECC. High-integration with Arm® Ethos™-U55 NPU, Layer 3 Ethernet Switch Module, USB 2.0 High-Speed, CANFD, SDHI, I3C, Octal SPI, Decryption on-the-fly, Graphics LCD Controller, 2D Drawing Engine, MIPI DSI/CSI, and advanced analog. Integrated Renesas Security IP with cryptography accelerators, key management support, tamper detection and power analysis resistance in concert with Arm® TrustZone for integrated Secure element functionality.

Features

Arm® Cortex®-M85 Core

- Armv8.1-M architecture profile
- Armv8-M Security Extension
- Maximum operating frequency: 1 GHz
- Memory Protection Unit (Arm MPU)
  - Protected Memory System Architecture (PMSAv8)
  - Secure MPU (MPU_S): 8 regions
  - Non-secure MPU (MPU_NS): 8 regions
- SysTick timer
  - Embeds two Systick timers: Secure and Non-secure instance
  - Driven by CPUCLK0 or MOCO divided by 8
- CoreSight™ ETM-M85

Arm® Cortex®-M33 core

- Armv8-M architecture profile
- Armv8-M Security Extension
- Maximum operating frequency: 250 MHz
- Memory Protection Unit (Arm MPU)
  - Protected Memory System Architecture (PMSAv8)
  - Secure MPU (MPU_S): 8 regions
  - Non-secure MPU (MPU_NS): 8 regions
- SysTick timer
  - Embeds two Systick timers: Secure and Non-secure instance
  - Driven by CPUCLK1 or MOCO divided by 8
- CoreSight™ ETM-M33

Memory

- Up to 1-MB MRAM
- 2 MB SRAM including 256 KB of CM85 TCM and 128 KB of CM33 TCM

Connectivity

- Serial Communications Interface (SCI) × 10, up to 60 Mbps
  - Asynchronous interfaces
  - 8-bit clock synchronous interface
  - Smart card interface
  - Simple IIC
  - Simple SPI
  - Manchester coding
  - Simple LIN
- I^2C bus interface (IIC) × 3
- I^3C bus interface (I3C)
- Serial Peripheral Interface (SPI) × 2, up to 166 Mbps
- Octal Serial Peripheral Interface (OSPI) × 2, up to 333 MBps
- USB 2.0 Full-Speed Module (USBFS)
- USB 2.0 High-Speed Module (USBHS)
- CAN with Flexible Data-rate (CANFD) × 2
- Layer 3 Ethernet Switch Module (ESWM)
  - PHY interface × 2
  - Ethernet switch
  - Ethernet MAC × 2
- SD/MMC Host Interface (SDHI) × 2
- Serial Sound Interface Enhanced (SSIE) × 2
- Pulse Density Modulation Interface (PDMIF)

Analog

- 16-bit A/D Converter (ADC16) × 2
- 12-bit D/A Converter (DAC12) × 2
- High-Speed Analog Comparator (ACMPHS) × 4
- Temperature Sensor (TSN)

Timers

- General PWM Timer 32-bit (GPT32) with High Resolution × 4
  - 52 ps resolution in 300 MHz
- General PWM Timer 32-bit (GPT32) × 10
- Low Power Asynchronous General Purpose Timer (AGT) × 2
- Ultra-Low-Power Timer (ULPT) × 2

Security and Encryption

- Renesas Security IP (RSIP-E50D)
  - Symmetric algorithms: AES and ChaCha20-Poly1305
  - Asymmetric algorithms: RSA and ECC
  - Hash-value generation: SHA224, SHA256, SHA384, SHA512 and SHA3
  - 128-bit unique ID
- Arm® TrustZone®
  - Up to two regions for the code MRAM
  - Up to two regions for the SRAM
  - Individual Secure or Non-secure security attribution for each peripheral
- Privileged control
- Device lifecyle management
- Secure boot
  - Immutable first stage boot loader in OTP
- Decryption on-the-fly (DOTF)
- Pin function
  - Up to three tamper-resistant pins
  - Secure pin multiplexing
- HUK zeroization

System and Power Management

- Low power modes
- Battery backup function (VBATT)
- Realtime Clock (RTC) with calendar and VBATT support
- Event Link Controller (ELC)
- Data Transfer Controller (DTC) × 2
- DMA Controller (DMAC) × 16
- Power-on reset
- Programable Voltage Detection (PVD) with voltage settings
- Watchdog Timer (WDT) × 2
- Independent Watchdog Timer (IWDT)

Human Machine Interface (HMI)

- Graphics LCD Controller (GLCDC)
- 2D Drawing Engine (DRW)
- Capture Engine Unit (CEU)
- MIPI DSI/CSI

Arm® Ethos™-U55 NPU

- Number of 8x8 MACs: 256 units
- Network: 8-bit and 16-bit integer quantized Convolutional Neural Networks (CNN) and Recurrent Neural Networks (RNN)
- Compression: 8-bits weights
- Maximum operating frequency: 500 MHz

Multiple Clock Sources

- Main clock oscillator (MOSC) (8 to 48 MHz)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (16/18/20/32/48 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- PLL1/PLL2
- Clock out support

General-Purpose I/O Ports

- 5-V tolerance, open drain, input pull-up, switchable driving ability

Operating Voltage

- VCC/VCC2: 1.62 to 3.63 V

Operating Junction Temperature and Packages

- Tj = 0 °C to +95 °C
  - 289-pin BGA (12 mm × 12 mm, 0.65 mm pitch)
  - 224-pin BGA (11 mm × 11 mm, 0.65 mm pitch)
- Tj = -40 °C to +105 °C

– 289-pin BGA (12 mm × 12 mm, 0.65 mm pitch)
– 224-pin BGA (11 mm × 11 mm, 0.65 mm pitch)

1. Overview

The MCU integrates multiple series of software-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm® Cortex®-M85 core running up to 1 GHz and Arm® Cortex®-M33 core running up to 250 MHz with the following features:

- Up to 1 MB MRAM
- 2 MB SRAM (256 KB of CM85 TCM RAM, 128 KB CM33 TCM RAM, 1664 KB of user SRAM)
- Arm® Ethos™-U55 NPU
- Octal Serial Peripheral Interface (OSPI)
- Layer 3 Ethernet Switch Module (ESWM), USBFS, USBHS, SD/MMC Host Interface
- Graphics LCD Controller (GLCDC)
- 2D Drawing Engine (DRW)
- MIPI DSI/CSI interface
- Analog peripherals
- Security and safety features

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm® Cortex®-M85 core	• Maximum operating frequency: up to 1 GHz • Arm® Cortex®-M85 core – Revision: (r0p2-00rel0) – ARMv8.1-M architecture profile – Armv8-M Security Extension – Floating Point Unit (FPU) compliant with the ANSI/IEEE Std 754-2008 Scalar half, single, and double-precision floating-point operation – M-profile Vector Extension (MVE) Integer, half-precision, and single-precision floating-point MVE (MVE-F) • Arm® Memory Protection Unit (Arm MPU) – Protected Memory System Architecture (PMSAv8) – Secure MPU (MPU_S): 8 regions – Non-secure MPU (MPU_NS): 8 regions • SysTick timer – Embeds two Systick timers: Secure instance (SysTick_S) and Non-secure instance (SysTick_NS) – Driven by CPUCLK0 or MOCO divided by 8 • CoreSight™ ETM-M85
Arm® Cortex®-M33 core	• Maximum operating frequency: up to 250 MHz • Arm® Cortex®-M33 core – Revision: (r0p4-00rel2) – ARMv8-M architecture profile – Armv8-M Security Extension – Armv8-DSP Extension – Floating Point Unit (FPU) compliant with the ANSI/IEEE Std 754-2008 single-precision floating-point operation • Arm® Memory Protection Unit (Arm MPU) – Protected Memory System Architecture (PMSAv8) – Secure MPU (MPU_S): 8 regions – Non-secure MPU (MPU_NS): 8 regions • SysTick timer – Embeds two Systick timers: Secure instance (SysTick_S) and Non-secure instance (SysTick_NS) – Driven by CPUCLK1 or MOCO divided by 8 • CoreSight™ ETM-M33

Table 1.2 Memory

Feature	Functional description
Code MRAM	Maximum 1 MB of code MRAM.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset.
SRAM	On-chip high-speed SRAM with Error Correction Code (ECC).
OTP	On-chip OTP contains First Stage Bootloader (FSBL) General purpose 96-byte OTP

Table 1.3 System

Feature	Functional description
Operating modes	Three operating modes: ● Single-chip mode ● JTAG boot mode ● SCI/USB boot mode
Resets	This MCU provides the following 21 types of reset.
Programable Voltage Detection (PVD)	The Programable Voltage Detection (PVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The PVD module consists of five separate voltage level detectors (PVD0, PVD1, PVD2, PVD4, PVD5). These PVDs measure the voltage level input to the VCC pin. PVD registers allow your application to configure detection of VCC changes at various voltage thresholds.
Clocks	● Main clock oscillator (MOSC) ● Sub-clock oscillator (SOSC) ● High-speed on-chip oscillator (HOCO) ● Middle-speed on-chip oscillator (MOCO) ● Low-speed on-chip oscillator (LOCO) ● PLL1/PLL2 ● Clock out support
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), DMA Controller (DMAC) module and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.
Low power modes	Power consumption can be reduced in multiple ways, including setting clock dividers, controlling EBCLK output, controlling SDCLK output, stopping modules, power gating control, selecting operating power control modes in normal operation, and transitioning to low power modes and processor low power modes.
Battery backup function	A battery backup function is provided for partial powering by a battery. The battery-powered area includes the RTC, SOSC, backup register, tamper detection and VBATT_R voltage drop detection and switch between VCC and VBATT.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR_S and PRCR_NS).
Memory Protection Unit (MPU)	All bus masters have Memory Protection Units (MPUs).

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.
DMA Controller (DMAC)	The 8-channel direct memory access controller (DMAC) that can transfer data without intervention from the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address.

Table 1.6 External bus interface

Feature	Functional description
External buses	• CS area (ECBI): Connected to the external devices (external memory interface) • SDRAM area (ECBI): Connected to the SDRAM (external memory interface) • OSPI0 area (OSPI0BI): Connected to the OSPI0 (external device interface) • OSPI1 area (OSPI1BI): Connected to the OSPI1 (external device interface)

Table 1.7 Timers

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with GPT32 × 14 channels. PWM waveforms can be generated by controlling the up-counter, down- counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer.
PWM Delay Generation Circuit (PDG)	The PWM Delay Generation circuit (PDG) has 4 channels delay circuits that can connect to the GPT. The PDG can control the rise and fall edge timing with which the PWM output for the GPT320 through the GPT323.
Port Output Enable for GPT (POEG)	The Port Output Enable (POEG) function can place the General PWM Timer (GPT) output pins in the output disable state
Low Power Asynchronous General Purpose Timer (AGT)	The Low Power Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register.
Ultra-Low-Power Timer (ULPT)	The Ultra-Low-Power Timer (ULPT) is a 32-bit timer which can be used for outputting pulses or counting external events. This 32-bit timer consists of reload registers and a down-counter. The reload registers and the down-counter are allocated to the same address and can be accessed through the ULPTCNT register.
Realtime Clock (RTC)	The realtime clock (RTC) has two counting modes, calendar count mode and binary count mode, that are used by switching register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar.
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) has a 14-bit down-counter, which resets the MCU by a reset output when the down-counter underflows. Alternatively, generation of an interrupt request when the counter underflows can be selected. This enables detection of a program runaway taking the refresh interval into account. The IWDT has two start modes: auto start mode, in which counting automatically starts after release from the reset state, and register start mode, in which counting is started by refreshing (writing to a specific register).

Table 1.8 Communication interfaces (1 of 2)

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) × 10 channels have asynchronous and synchronous serial interfaces: ● Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) ● 8-bit clock synchronous interface ● Simple IIC (master-only) ● Simple SPI ● Smart card interface ● Manchester interface ● Simple LIN interface The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. All channels have FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. The maximum rate supported on this MCU. Refer to the electrical characteristics for the actual rate.
I^2C Bus interface (IIC)	The I^2C Bus interface (IIC) has 3 channels. The IIC module conforms with and provides a subset of the NXP I^2C (Inter-Integrated Circuit) bus interface functions.
I3C Bus Interface (I3C)	The I3C Bus Interface (I3C) has 1 channel. The I3C module conform with and provide a subset of the NXP I^2C (Inter-Integrated Circuit) bus interface functions and a subset of the MIPI I3C.
Serial Peripheral Interface (SPI)	The Serial Peripheral Interface (SPI) provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices. The maximum rate supported on this MCU. Refer to the electrical characteristics for the actual rate.
Control Area Network with Flexible Data-Rate Module (CANFD)	The CAN with Flexible Data-Rate (CANFD) module can handle classical CAN frames and CANFD frames complied with ISO 11898-1 standard. The module supports 4 transmit buffers per channel and 16 receive buffers per channel.
USB 2.0 Full-Speed module (USBFS)	The USB 2.0 Full-Speed module (USBFS) can operate as a host controller or device controller. The module supports full-speed and low-speed (host controller only) transfer as defined in Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on your system.
USB 2.0 High-speed Module (USBHS)	The USB 2.0 High-Speed Module (USBHS) that operates as a host or a device controller compliant with the Universal Serial Bus (USB) Specification revision 2.0. The host controller supports USB 2.0 high-speed, full speed, and low-speed transfers, and the device controller supports USB 2.0 high-speed and full-speed transfers. The USBHS has an internal USB transceiver and supports all of the transfer types defined in the USB 2.0 specification. The USBHS has FIFO buffer for data transfers, providing a maximum of 10 pipes.
Octal Serial Peripheral Interface (OSPI)	The Octal Serial Peripheral Interface (OSPI) is a memory controller that supports Expanded Serial Peripheral Interface (xSPI) (JEDEC Standard JESD251, JESD251-1 and JESD252) . The OSPI supports 1-bit, 2-bit, 4-bit and 8-bit protocols. JESD251 specifies two interface profiles where profile 1.0 is Octal SPI and profile 2.0 is HyperBus™ (HyperRAM™ and HyperFlash™). OSPI supports QSPI protocol.
Serial Sound Interface Enhanced (SSIE)	The Serial Sound Interface Enhanced (SSIE) peripheral provides functionality to interface with digital audio devices for transmitting I^2S/Monaural/TDM audio data over a serial bus. The SSIE supports an audio clock frequency of up to 50 MHz, and can be operated as a slave or master receiver, transmitter, or transceiver to suit various applications. The SSIE includes 32-stage FIFO buffers in the receiver and transmitter, and supports interrupts and DMA-driven data reception and transmission.
SD/MMC Host Interface (SDHI)	The Secure Digital (SD) Card and Multi Media Card (MMC) Host Interface provides the functionality required to connect a variety of external memory cards to the MCU. The SDHI supports both 1- and 4-bit buses for connecting memory cards that support SD, SDHC, and SDXC formats. When developing host devices that are compliant with the SD Specifications, you must comply with the SD Host/Ancillary Product License Agreement (SD HALA). The MMC interface supports 1-bit, 4-bit, and 8-bit MMC buses that provide eMMC 4.51 (JEDEC Standard JESD 84-B451) device access. This interface also provides backward compatibility and supports high-speed SDR transfer modes.

Table 1.8 Communication interfaces (2 of 2)

Feature	Functional description
Layer 3 Ethernet Switch Module (ESWM)	The Layer 3 Ethernet Switch Module (ESWM) consists on an Ethernet switch with higher level routing capability and multi-protocol interface support. It allows autonomous frame routing within same and between different network interfaces protocols (for now only Ethernet) for optimized gateway applications.
Pulse Density Modulation Interface (PDMIF)	PDM-IF has maximum three channels that are connectable with external microphone which outputs the pulse density modulated (PDM) signal. PDM-IF is connectable with up to three external microphones. PDM-IF can filter and convert 1-bit digital data streams that were pulse density modulated at a high sampling rate into 20-bit or 16-bit digital data at a lower sampling rate.

Table 1.9 Analog

Feature	Functional description
16-bit A/D Converter (ADC16)	A 16-bit A/D Converter is provided. Up to 23 analog input channels are selectable. Temperature sensor output, and internal reference voltage and VBATT 1/6 voltage monitor are selectable for conversion.
12-bit D/A Converter (DAC12)	A 12-bit D/A Converter (DAC12) is provided.
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC16 for conversion and can be further used by the end application. The sensor outputs an abnormal temperature detection signal to the reset control circuit and can be used to prevent the malfunction due to abnormal temperature.
High-Speed Analog Comparator (ACMPHS)	The High-Speed Analog Comparator (ACMPHS) can be used to compare an analog input voltage with a reference voltage and to provide a digital output based on the result of conversion. Both the analog input voltage and the reference voltage can be provided to the ACMPHS from internal sources (D/A converter output or internal reference voltage) and an external source. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion.

Table 1.10 Human machine interfaces (1 of 2)

Feature	Functional description
Graphics LCD Controller (GLCDC)	The Graphics LCD Controller (GLCDC) provides multiple functions and supports various data formats and panels. Key GLCDC features include: ● GLCDC0BI/GLCDC1BI master function for accessing graphics data ● Superimposition of three planes (single-color background plane, graphic 1-plane, and graphic 2-plane) ● Support for many types of 32-bit or 16-bit per pixel graphics data and 8-bit, 4-bit, or 1-bit LUT data format ● Digital interface signal output supporting a video image size of WXGA.
2D Drawing Engine (DRW)	The 2D Drawing Engine (DRW) provides flexible functions that can support almost any object geometry rather than being bound to only a few specific geometries such as lines, triangles, or circles. The edges of every object can be independently blurred or antialiased. Rasterization is executed at one pixel per clock on the bounding box of the object from left to right and top to bottom. The DRW can also raster from bottom to top to optimize the performance in certain cases. In addition, optimization methods are available to avoid rasterization of many empty pixels of the bounding box. The distances to the edges of the object are calculated by a set of edge equations for every pixel of the bounding box. These edge equations can be combined to describe the entire object. If a pixel is inside the object, it is selected for rendering. If it is outside, it is discarded. If it is on the edge, an alpha value can be chosen proportional to the distance of the pixel to the nearest edge for antialiasing. Every pixel that is selected for rendering can be textured. The resulting ARGB quadruple can be modified by a general raster operation approach independently for each of the four channels. The ARGB quadruples can then be blended with one of the multiple blend modes of the DRW. The DRW provides two inputs (texture read and framebuffer read), and one output (framebuffer write). The internal color format is always ARGB (8888). The color formats from the inputs are converted to the internal format on read and a conversion back is made on write.
Capture Engine Unit (CEU)	The Capture Engine Unit (CEU) is a capture module that fetches image data externally input and transfers it to the memory.

Table 1.10 Human machine interfaces (2 of 2)

Feature	Functional description
MIPI DSI interface	The MIPI DSI interface module has a Transmitter function for MIPI Alliance Specification for Display Serial Interface 2 (DSI-2). This module supports MIPI Alliance Specification for Display Serial Interface 2 (DSI-2) Specification. And it works with MIPI Alliance Specification for D-PHY Specification. This module provides a solution for transmitting MIPI DSI-2 compliant digital video and packets.
MIPI CSI interface	The MIPI CSI consists of a MIPI CSI-2 block and a Video Input Module block. 1. MIPI CSI-2 This block can receive signals conforming to the MIPI CSI-2 standard, extracts video data from various packets, and sends them to Video Input Module in the subsequent stage. 2. Video Input Module (VIN) This block can receive video data received from MIPI CSI-2 block, and perform appropriate image processing for each. The image-processed data is temporarily stored in the FIFO and transferred to an external memory.

Table 1.11 Neural processing

Feature	Functional description
Arm® Ethos™-U55 NPU	• Maximum operating frequency: 500 MHz • Arm® Ethos™-U55 NPU – Revision: r2p0_01eac0 – Number of 8x8 MACs: 256 units – Network: 8-bit and 16-bit integer quantized Convolutional Neural Networks (CNN) and Recurrent Neural Networks (RNN) – Compression: 8-bits weights

Table 1.12 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 32-bits data. When a selected condition applies, 32-bit data is compared and an interrupt can be generated.

Table 1.13 Security

Feature	Functional description
Security function	• ARMv8-M TrustZone security • Privileged control • Device lifecycle management • Authentication Level (AL) • Key injection • Secure pin multiplexing • HUK zeroization • VBATT backup registers zeroization • Secure boot • Secure factory programming
Renesas Secure IP (RSIP-E50D)	• Symmetric cryptography: AES and ChaCha20-Poly1305 • Asymmetric cryptography: RSA and ECC • Message digest computation: HASH, HMAC • 128-bit true random number generation circuit • 256-bit Hardware Unique Key (HUK) • 128-bit unique ID • OEM boot loader version • Key data for the decryption on-the-fly (DOTF) • SPA/DPA Protections
Decryption on-the-fly (DOTF)	Decryption on-the-fly (DOTF) decrypts the encrypted content stored in the external memory in real-time.

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

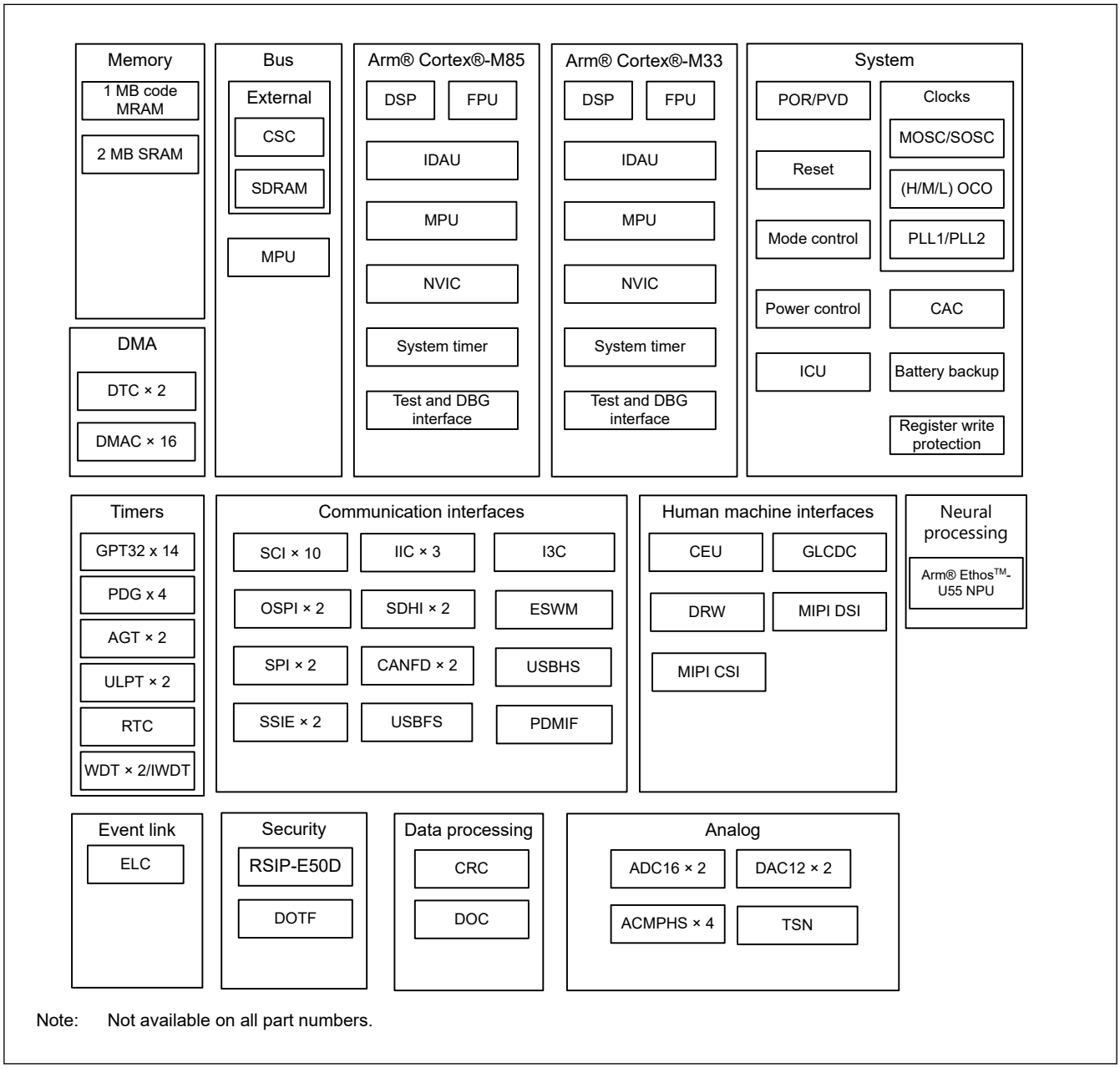

Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.14 shows a list of products.

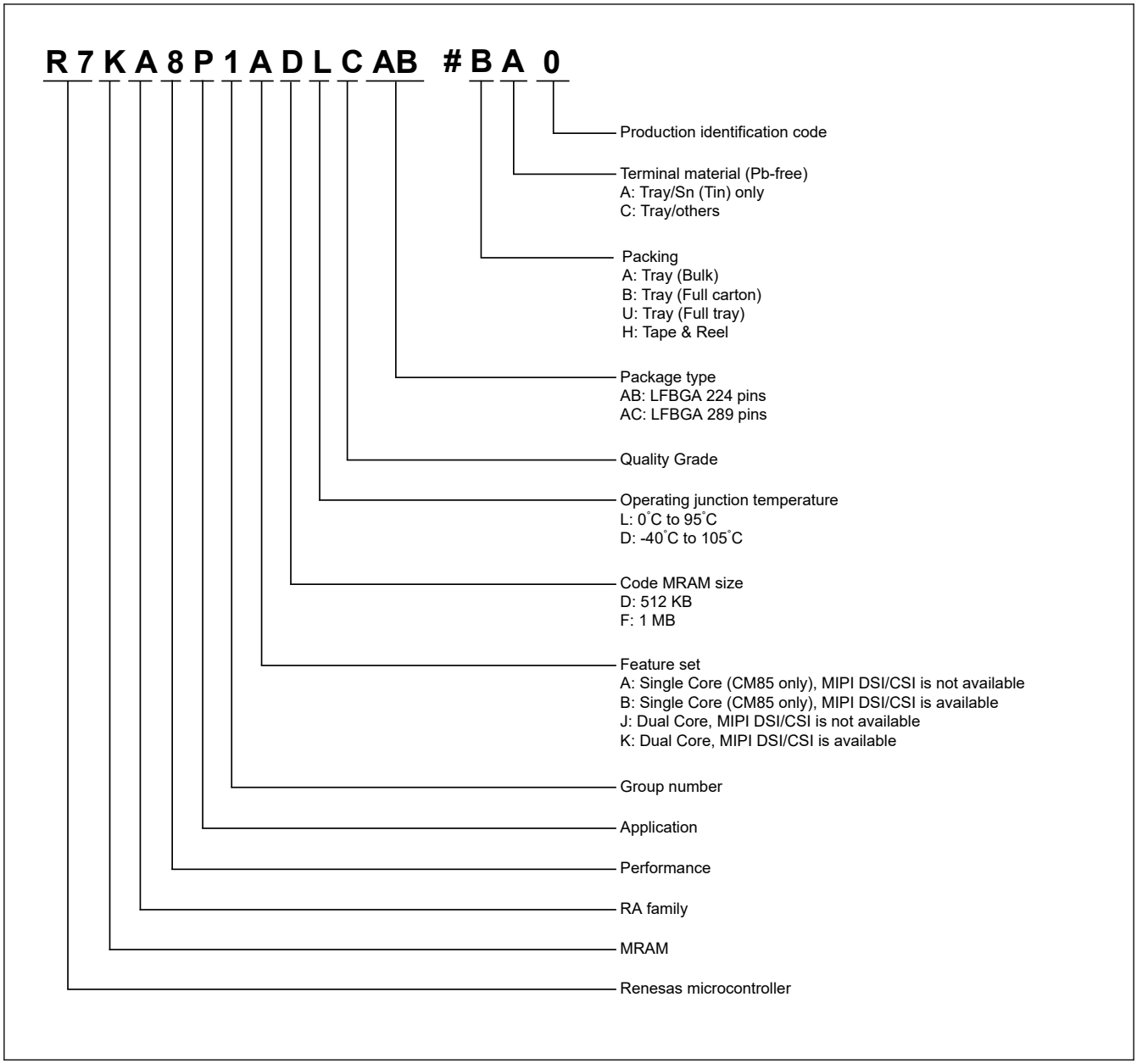

Figure 1.2 Part numbering scheme

Table 1.14 Product list

Product part number	CPU	MIPI DSI/CSI	Package code	Code MRAM	SRAM	Operating junction temperature
R7KA8P1ADLCAB	Single	—	PLBG0224JA-A	512 KB	2 MB	0 to 95 °C
R7KA8P1ADLCAC			PLBG0289JA-A			
R7KA8P1ADDCAB			PLBG0224JA-A			-40 to 105 °C
R7KA8P1ADDCAC			PLBG0289JA-A			
R7KA8P1AFLCAB			PLBG0224JA-A	1 MB		0 to 95 °C
R7KA8P1AFLCAC			PLBG0289JA-A			
R7KA8P1AFDCAB			PLBG0224JA-A			-40 to 105 °C
R7KA8P1AFDCAC			PLBG0289JA-A			
R7KA8P1BDLCAB		✔	PLBG0224JA-A	512 KB		0 to 95 °C
R7KA8P1BDLCAC			PLBG0289JA-A			
R7KA8P1BDDCAB			PLBG0224JA-A			-40 to 105 °C
R7KA8P1BDDCAC			PLBG0289JA-A			
R7KA8P1BFLCAB			PLBG0224JA-A	1 MB		0 to 95 °C
R7KA8P1BFLCAC			PLBG0289JA-A			
R7KA8P1BFDCAB			PLBG0224JA-A			-40 to 105 °C
R7KA8P1BFDCAC			PLBG0289JA-A			
R7KA8P1JFLCAB	Dual	—	PLBG0224JA-A	1 MB		0 to 95 °C
R7KA8P1JFLCAC			PLBG0289JA-A			
R7KA8P1JFDCAB			PLBG0224JA-A			-40 to 105 °C
R7KA8P1JFDCAC			PLBG0289JA-A			
R7KA8P1KFLCAB		✔	PLBG0224JA-A			0 to 95 °C
R7KA8P1KFLCAC			PLBG0289JA-A			
R7KA8P1KFDCAB			PLBG0224JA-A			-40 to 105 °C
R7KA8P1KFDCAC			PLBG0289JA-A			

1.4 Function Comparison

Table 1.15 Function Comparison (1 of 2)

Parts number		R7KA8P1A xxCAC	R7KA8P1B xxCAC	R7KA8P1J xxCAC	R7KA8P1K xxCAC	R7KA8P1A xxCAB	R7KA8P1B xxCAB	R7KA8P1J xxCAB	R7KA8P1K xxCAB
Pin count		289				224			
Package		BGA							
I/O Port		208	199	208	199	149	142	149	142
Code MRAM		1 MB, 512 KB							
CPU0 TCM		256 KB							
CPU1 TCM		No		128 KB		No		128 KB	
CPU0 I/D Caches		32 KB							
CPU1 C/S Caches		No		32 KB		No		32 KB	
SRAM		1792 KB		1664 KB		1792 KB		1664 KB	
DMA	DTC	1		2		1		2	
	DMAC	8		16		8		16	
BUS	External bus	32-bit bus				16-bit bus			
	SDRAM	32-bit bus				16-bit bus			
System	CPU0 clock	1 GHz (max.)							
	CPU1 clock	No		250 MHz (max.)		No		250 MHz (max.)	
	CPUs clock sources	MOSC, SOSC, HOCO, MOCO, LOCO, PLL1P							
	CAC	Yes							
	WDT	1		2		1		2	
	IWDT	Yes							
	Backup register	128 B							
Communication	SCI	10				9			
	IIC	3							
	I3C	Yes							
	SPI	2							
	CANFD	2							
	USBFS	Yes							
	USBHS	Yes							
	OSPI	2				1			
	SSIE	2							
	SDHI/MMC	2							
	ESWM	MII, RMII, GMII, RGMII				MII, RMII, RGMII			
	PDMIF	Yes							
Timers	GPT32*1	14							
	PDG	4							
	AGT*1	2							
	ULPT*1	2							
	RTC	Yes							

Table 1.15 Function Comparison (2 of 2)

Parts number		R7KA8P1A xxCAC	R7KA8P1B xxCAC	R7KA8P1J xxCAC	R7KA8P1K xxCAC	R7KA8P1A xxCAB	R7KA8P1B xxCAB	R7KA8P1J xxCAB	R7KA8P1K xxCAB
Analog	ADC16	Unit 0: 15, Unit 1: 15				Unit 0: 7, Unit 1: 5			
	DAC12	2							
	ACMPHS	4							
	TSN	Yes							
HMI	GLCDC	RGB888							
	DRW	Yes							
	MIPI DSI/CSI	No	Yes	No	Yes	No	Yes	No	Yes
	CEU	Yes							
Neural processing	NPU	Yes							
Data processing	CRC	Yes							
	DOC	Yes							
Event control	ELC	Yes							
Security		RSIP-E50D, Secure Debug, OTP, TrustZone, and Lifecycle management							

Note: The product name differs depend on the memory size and MIPI DSI is supported. see section 1.3. Part Numbering.
Note 1. Available pins depend on the Pin count, about details see section 1.7. Pin Lists.

1.5 Pin Functions

Table 1.16 Pin functions (1 of 7)

Function	Signal	I/O	Description
Power supply	VCC_01 to VCC_10, VCC2_11 to VCC2_15	Input	Power supply pin. Connect it to the system power supply. Connect this pin to the same numbered VSS_01 to VSS_15 by a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VCC_DCDC	Input	Switching regulator power supply pin.
	VLO	I/O	Switching regulator pin.
	VCL0 to VCL11	Input	Connect this pin to the same numbered VSS0 to VSS11 pin by the smoothing capacitor used to stabilize the internal power supply.
	VBATT	Input	Battery Backup power pin
	VSS_01 to VSS_15, VSS0 to VSS11, VSS_DCDC	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	EXCIN	Input	External sub-clock input
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
On-chip emulator	TMS	Input	On-chip emulator or boundary scan pins
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TCLK	Output	Output clock for synchronization with the trace data
	TDATA0 to TDATA3	Output	Trace data output
	SWO	Output	Serial wire trace output pin
	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQn	Input	Maskable interrupt request pins
	IRQn-DS	Input	Maskable interrupt request pins that can also be used in Deep Software Standby mode

Table 1.16 Pin functions (2 of 7)

Function	Signal	I/O	Description
External bus interface	EBCLK	Output	Outputs the external bus clock for external devices
	RD	Output	Strobe signal indicating that reading from the external bus interface space is in progress, active-low
	WR	Output	Strobe signal indicating that writing to the external bus interface space is in progress, in 1-write strobe mode, active-low
	WRn	Output	Strobe signals indicating that either group of data bus pins (D07 to D00, D15 to D08, D23 to D16 or D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode, active-low
	BCn	Output	Strobe signals indicating that either group of data bus pins (D07 to D00, D15 to D08, D23 to D16 or D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode, active-low
	ALE	Output	Address latch signal when address/data multiplexed bus is selected
	WAIT	Input	Input pin for wait request signals in access to the external space, active-low
	CSn	Output	Select signals for CS areas, active-low
	A00 to A23	Output	Address bus
	D00 to D31	I/O	Data bus
	A00/D00 to A15/D15	I/O	Address/data multiplexed bus
SDRAM interface	SDCLK	Output	Outputs the SDRAM-dedicated clock
	CKE	Output	SDRAM clock enable signal
	SDCS	Output	SDRAM chip select signal, active low
	RAS	Output	SDRAM low address strobe signal, active low
	CAS	Output	SDRAM column address strobe signal, active low
	WE	Output	SDRAM write enable signal, active low
	DQMn	Output	SDRAM I/O data mask enable signal for DQ07 to DQ00, DQ15 to DQ08, DQ23 to DQ16 or DQ31 to DQ24
	A00 to A16	Output	Address bus
	DQ00 to DQ31	I/O	Data bus
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins
	GTIOCnA, GTIOCnB	I/O	Input capture, output compare, or PWM output pins
	GTADSM0, GTADSM1	Output	A/D conversion start request monitoring output pins
	GTCPPOn	Output	Toggle output synchronized with PWM period
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)

Table 1.16 Pin functions (3 of 7)

Function	Signal	I/O	Description
AGT	AGTEEn	Input	External event input enable signals
	AGTIOn	I/O	External event input and pulse output pins
	AGTOn	Output	Pulse output pins
	AGTOAn	Output	Output compare match A output pins
	AGTOBn	Output	Output compare match B output pins
ULPT	ULPTEEn	Input	External count control input
	ULPTEVIn	Input	External event input
	ULPTEEn-DS	Input	External count control input that can also be used in Deep Software Standby mode 1
	ULPTEVIn-DS	Input	External event input that can also be used in Deep Software Standby mode 1
	ULPTOn	Output	Pulse output
	ULPTOAn	Output	Output compare match A output
	ULPTOBn	Output	Output compare match B output
	ULPTOn-DS	Output	Pulse output that can also be used in Deep Software Standby mode 1
	ULPTOAn-DS	Output	Output compare match A output that can also be used in Deep Software Standby mode 1
	ULPTOBn-DS	Output	Output compare match B output that can also be used in Deep Software Standby mode 1
RTC	RTCOUT	Output	Output pin for 1-Hz or 64-Hz clock
	RTCICn	Input	Time capture event input pins
SCI	SCKn	I/O	Input/output pins for the clock (clock synchronous mode)
	RXDn	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXDn	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTSn_RTSn	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active- low.
	CTSn	Input	Input for the start of transmission.
	DEn	Output	Driver enable signal for RS-485
	SCLn	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDAn	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCKn	I/O	Input/output pins for the clock (simple SPI mode)
	MISOn	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSIn	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SSn	Input	Chip-select input pins (simple SPI mode), active-low
IIC	SCLn	I/O	Input/output pins for the clock
	SDAn	I/O	Input/output pins for data
I3C	I3C_SCL0	I/O	Input/output pins for the clock
	I3C_SDA0	I/O	Input/output pins for data
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Input or output pins for data output from the master
	MISOA, MISOB	I/O	Input or output pins for data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pins for slave selection

Table 1.16 Pin functions (4 of 7)

Function	Signal	I/O	Description
CANFD	CRXn	Input	Receive data
	CTXn	Output	Transmit data
USBFS	VCC_USB	Input	Power supply pin
	VSS_USB	Input	Ground pin
	USB_DP	I/O	D+ pin of the USB on-chip transceiver. Connect this pin to the D+ pin of the USB bus.
	USB_DM	I/O	D- pin of the USB on-chip transceiver. Connect this pin to the D- pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. Connect this pin to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a function controller.
	USB_EXICEN	Output	Low-power control signal for external power supply (OTG) chip
	USB_VBUSEN	Output	VBUS (5 V) supply enable signal for external power supply chip
	USB_OVRCURA, USB_OVRCURB	Input	Connect the external overcurrent detection signals to these pins. Connect the VBUS comparator signals to these pins when the OTG power supply chip is connected.
	USB_OVRCURA-DS, USB_OVRCURB-DS	Input	Overcurrent pins for USBFS that can also be used in Deep Software Standby mode 1. Connect the external overcurrent detection signals to these pins. Connect the VBUS comparator signals to these pins when the OTG power supply chip is connected.
	USB_ID	Input	Connect the MicroAB connector ID input signal to this pin during operation in OTG mode
USBHS	VCC_USBHS	Input	Power supply pin
	VSS1_USBHS, VSS2_USBHS	Input	Ground pin
	AVCC_USBHS	Input	Analog power supply
	USBHS_RREF	I/O	Reference current source pin for the USBHS Must be connected to the AVSS_USBHS pin through a 2.2-kΩ (±1%) resistor.
	USBHS_DP	I/O	Input/output pin for the D+ data line of the USB bus
	USBHS_DM	I/O	Input/output pin for the D- data line of the USB bus
	USBHS_EXICEN	Output	Must be connected to the OTG power supply IC
	USBHS_ID	input	Must be connected to the OTG power supply IC
	USBHS_VBUSEN	Output	VBUS power supply enable pin for the USBHS
	USBHS_OVRCURA, USBHS_OVRCURB	Input	Overcurrent pin for the USBHS
	USBHS_OVRCURA-DS, USBHS_OVRCURB-DS	Input	Overcurrent pin for the USBHS that can also be used in Deep Software Standby mode 1.
	USBHS_VBUS	Input	USB cable connection monitor input pin

Table 1.16 Pin functions (5 of 7)

Function	Signal	I/O	Description
OSPI	OM_n_SCLK	Output	Clock output (OCTACLK divided by 2)
	OM_n_SCLKN	Output	Inverted clock output (OCTACLK divided by 2)
	OM_n_CSn	Output	Chip select signal for an OctaFlash device, active-low
	OM_n_DQS	I/O	Read data strobe/write data mask signal
	OM_n_SIOn	I/O	Data input/output
	OM_n_RESET	Output	Reset signal for both slave devices, active-low
	OM_n_ECSINT1	Input	Error Correction Status and Interrupt for slave1
	OM_n_RSTO1	Input	Slave reset status for slave1
	OM_n_WP1	Output	Write Protect for slave1, active-low
SSIE	SSIBCK0, SSIBCK1	I/O	SSIE serial bit clock pins
	SSILRCK0/SSIFS0, SSILRCK1/SSIFS1	I/O	LR clock/frame synchronization pins
	SSITXD0	Output	Serial data output pin
	SSIRXD0	Input	Serial data input pin
	SSIDATA1	I/O	Serial data input/output pins
	AUDIO_CLK	Input	External clock pin for audio (input oversampling clock)
SDHI/MMC	SDnCLK	Output	SD clock output pins
	SDnCMD	I/O	Command output pin and response input signal pins
	SDnDAT0 to SDnDAT7	I/O	SD and MMC data bus pins
	SDnCD	Input	SD card detection pins
	SDnWP	Input	SD write-protect signals

Table 1.16 Pin functions (6 of 7)

Function	Signal	I/O	Description
ESWM	ETn_GTX_CLK	Output	1000 Mb/s transmit clock
	ETn_TX_CLK	Input	100 Mb/s,10 Mb/s transmit clock
	ETn_RX_CLK	Input	Receive clock
	ETn_TX_EN	Output	Transmit enable
	ETn_TXD0 to ETn_TXD7	Output	Transmit data
	ETn_TX_ER	Output	Transmit coding error
	ETn_RX_DV	Input	Receive data valid
	ETn_RXD0 to ETn_RXD7	Input	Receive data
	ETn_RX_ER	Input	Receive error
	ETn_MDC	Output	Management data clock
	ETn_MDIO	I/O	Management data input/output
	RGMIIn_TXC	Output	Transmit clock
	RGMIIn_RXC	Input	Receive clock
	RGMIIn_TX_CTL	Output	Transmit control
	RGMIIn_TXD0 to RGMIIn_TXD3	Output	Transmit data
	RGMIIn_RX_CTL	Input	Receive control
	RGMIIn_RXD0 to RGMIIn_RXD3	Input	Receive data
	RMIIn_REF50CK	Input	Synchronous clock reference
	RMIIn_TX_EN	Output	Transmit enable
	RMIIn_TXD0 to RMIIn_TXD1	Output	Transmit data
	RMIIn_CRS_DV	Input	Carrier sense/Receive data valid
	RMIIn_RXD0 to RMIIn_RXD1	Input	Receive data
	RMIIn_RX_ER	Input	Receive error
	ETn_LINKSTA	Input	PHY Link Status
	ETn_INT	Input	PHY interrupt
	ETn_WOL	Output	Wake-on-LAN. This signal indicates that a Magic Packet was received.
	GPTPm_CAPTURE	Input	Media clock capture input
	GPTPm_MATCH	Output	Media clock recovery output
	GPTPm_PPS	Output	PPS signal
	GPTP_PTPOUT0 to GPTP_PTPOUT3	Output	PTP Pulse generator signal
	ET_TAS_STA0 to ET_TAS_STA3	Output	TAS status monitor
	ETHPHYCLK	Output	Clock output for PHY
PDMIF	PDMCLK0 to PDMCLK2	Output	Clock output pin
	PDMDAT0 to PDMDAT2	Input	Data input pin

Table 1.16 Pin functions (7 of 7)

Function	Signal	I/O	Description
Analog power supply	AVCC0	Input	Analog voltage supply pin. This is used as the analog power supply for the respective modules.
	AVSS0	Input	Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin.
	VREFH	Input	Analog reference voltage supply pin for the ADC16 (unit 1) and D/A Converter. Connect this pin to AVCC0 when not using the ADC16 (unit 1) and D/A Converter.
	VREFL	Input	Analog reference ground pin for the ADC16 and D/A Converter. Connect this pin to AVSS0 when not using the ADC16 (unit 1) and D/A Converter.
	VREFH0	Input	Analog reference voltage supply pin for the ADC16 (unit 0). Connect this pin to AVCC0 when not using the ADC16 (unit 0).
	VREFL0	Input	Analog reference ground pin for the ADC16. Connect this pin to AVSS0 when not using the ADC16 (unit 0).
ADC16	ANxxx	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRGm	Input	Input pins for the external trigger signals that start the A/D conversion, active-low.
	ADSTm	Output	AD conversion start
	ADmFLAG1	Output	AD conversion end
	ADSYNC	Output	Synchronization signal between units
DAC12	DAn	Output	Output pins for the analog signals processed by the D/A converter.
ACMPHS	VCOUT	Output	Comparator output pin
	IVREFn	Input	Reference voltage input pins for comparator
	IVCMPn	Input	Analog voltage input pins for comparator
I/O ports	Pmn	I/O	General-purpose input/output pins (m: port number, n: pin number)
	P200	Input	General-purpose input pin
GLCDC	LCD_DATA23 to LCD_DATA00	Output	Data output pins for panel
	LCD_TCON3 to LCD_TCON0	Output	Output pins for panel timing adjustment
	LCD_CLK	Output	Panel clock output pin
	LCD_EXTCLK	Input	Panel clock source input pin
MIPI	VCC18_MIPI	Input	Power supply pin
	AVCC_MIPI	Input	Analog power supply
	VSS_MIPI	Input	Ground pin
	MIPI_CL_P	Output	DSI/CSI Clock Lane positive pin
	MIPI_CL_N	Output	DSI/CSI Clock Lane negative pin
	MIPI_DL0_P	I/O	DSI/CSI Data Lane 0 positive pin
	MIPI_DL0_N	I/O	DSI/CSI Data Lane 0 negative pin
	MIPI_DL1_P	Output	DSI/CSI Data Lane 1 positive pin
	MIPI_DL1_N	Output	DSI/CSI Data Lane 1 negative pin
	DSI_TE	Input	DSI Tearing Effect pin
CEU	VIO_D15 to VIO_D0	Input	CEU data bus pins
	VIO_CLK	Input	CEU clock pins
	VIO_VD	Input	CEU vertical sync pins
	VIO_HD	Input	CEU horizontal sync pins
	VIO_FLD	Input	Field signal pins

1.6 Pin Assignments

The following figures show the pin assignments from the top view.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	P609	P113	P115	P112	P302	P915	VLO	VLO	VSS_DCDC	VCC_DCDC	VCC_DCDC	P309	P906	P905	P907	P904	P207	A
B	P813	PA12	P114	PA11	P300	P303	VLO	VLO	VSS_DCDC	VCC_DCDC	VCC_DCDC	P311	P908	P909	P206	PD01	PD02	B
C	PA06	P613	PA13	P301	P200	P210/TMS/SWDIO	P208/TDI	P110	P308	P305	P307	P911	P312	PD04	PD03	PD05	PD06	C
D	PA04	P611	P610	PA14	RES	P211/TCK/SWCLK	P109	P108	P903	P304	P306	P912	PB04	PB07	PB05	PB03	PB01	D
E	PA15	P615	P614	P612	P914	P201/MD	P209/TDO	P111	P902	P310	P910	P913	PB02	PB06	PD07	PB00	P706	E
F	PA02	PA10	PA08	PA09	PC14	VCC_08	VSS_08	VSS3	VCL3	VSS_07	VCC_07	P700	P702	P406	P701	P707	P705	F
G	PA00	PA03	PA05	PA07	PC12	VCC_09	VSS_09	VSS4	VCL4	VSS_06	VCC_06	P405	P704	P703	VSS_03	VCC_05	VSS_05	G
H	P504	P503	P505	PA01	PC11	VCC_10	VSS_10	VSS7	VCL5	VSS5	VCC_04	VSS_04	P403	VCC_03	VCC_USBHS	USBHS_DP	USBHS_DM	H
J	P506	P507	P508	P509	PC13	VCC2_11	VSS_11	VCL7	VCL6	VSS6	VCL2	VSS2	P404	VSS_02	USBHS_RREF	VSS2_USBHS	VSS1_USBHS	J
K	PC15	P608	P510	PD00	PC07	VSS_12	VSS9	VCL9	VCL8	VSS8	VCL1	VSS1	P410	VCC_02	AVCC_USBHS	P213/XTAL	P212/EXTAL	K
L	PC03	PC02	PC04	PC09	PC05	VCC2_12	VSS_14	VSS_15	VSS10	VCL10	VCL0	VSS0	P414	P402	VCC_01	P214/XCOUT	P215/XCIN/EXCIN	L
M	PC00	P607	PC01	PC08	PC10	P104	VCC2_14	VCC2_15	P810	VSS11	VCL11	P412	P710	P411	P408	VBATT	VSS_01	M
N	P605	P604	P606	PC06	P107	P106	P105	P811	P013	P011	P807	P708	P712	P714	P711	P713	P401	N
P	P603	P602	P600	P601	P102	P801	P803	P812	P012	P010	P009	P805	P512	P413	P515	P709	P400	P
R	VCC2_13	VCC18_MIPI	VSS_MIPI	P103	P101	P802	P804	P501	AVCC0	AVSS0	P005	P003	P513	P514	P415	P409	P407	R
T	MIPI_DL0_P	MIPI_CL_P	MIPI_DL1_P	AVCC_MIPI	P809	P800	P502	P014	VREFL	VREFL0	P004	P007	P001	P806	P715	P815/USB_DM	VSS_USB	T
U	MIPI_DL0_N	MIPI_CL_N	MIPI_DL1_N	VSS_13	P808	P100	P500	P015	VREFH	VREFH0	P008	P006	P000	P002	P511	P814/USB_DP	VCC_USB	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 1.3 Pin assignment for BGA 289-pin

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	P609	P113	P115	P112	P302	P915	VLO	VLO	VSS_DCDC	VCC_DCDC	VCC_DCDC	P309	P906	P905	P907	P904	P207	A
B	P813	PA12	P114	PA11	P300	P303	VLO	VLO	VSS_DCDC	VCC_DCDC	VCC_DCDC	P311	P908	P909	P206	PD01	PD02	B
C	PA06	P613	PA13	P301	P200	P210/TMS/SWDIO	P208/TDI	P110	P308	P305	P307	P911	P312	PD04	PD03	PD05	PD06	C
D	PA04	P611	P610	PA14	RES	P211/TCK/SWCLK	P109	P108	P903	P304	P306	P912	PB04	PB07	PB05	PB03	PB01	D
E	PA15	P615	P614	P612	P914	P201/MD	P209/TDO	P111	P902	P310	P910	P913	PB02	PB06	PD07	PB00	P706	E
F	PA02	PA10	PA08	PA09	PC14	VCC_08	VSS_08	VSS3	VCL3	VSS_07	VCC_07	P700	P702	P406	P701	P707	P705	F
G	PA00	PA03	PA05	PA07	PC12	VCC_09	VSS_09	VSS4	VCL4	VSS_06	VCC_06	P405	P704	P703	VSS_03	VCC_05	VSS_05	G
H	P504	P503	P505	PA01	PC11	VCC_10	VSS_10	VSS7	VCL5	VSS5	VCC_04	VSS_04	P403	VCC_03	VCC_USBHS	USBHS_DP	USBHS_DM	H
J	P506	P507	P508	P509	PC13	VCC2_11	VSS_11	VCL7	VCL6	VSS6	VCL2	VSS2	P404	VSS_02	USBHS_RREF	VSS2_USBHS	VSS1_USBHS	J
K	PC15	P608	P510	PD00	PC07	VSS_12	VSS9	VCL9	VCL8	VSS8	VCL1	VSS1	P410	VCC_02	AVCC_USBHS	P213/XTAL	P212/EXTAL	K
L	PC03	PC02	PC04	PC09	PC05	VCC2_12	VSS_14	VSS_15	VSS10	VCL10	VCL0	VSS0	P414	P402	VCC_01	P214/XCOUT	P215/XCIN/EXCIN	L
M	PC00	P607	PC01	PC08	PC10	P104	VCC2_14	VCC2_15	P810	VSS11	VCL11	P412	P710	P411	P408	VBATT	VSS_01	M
N	P605	P604	P606	PC06	P107	P106	P105	P811	P013	P011	P807	P708	P712	P714	P711	P713	P401	N
P	P603	P602	P600	P601	P102	P801	P803	P812	P012	P010	P009	P805	P512	P413	P515	P709	P400	P
R	VCC2_13	P315	P900	P103	P101	P802	P804	P501	AVCC0	AVSS0	P005	P003	P513	P514	P415	P409	P407	R
T	P205	P203	P313	P901	P809	P800	P502	P014	VREFL	VREFL0	P004	P007	P001	P806	P715	P815/USB_DM	VSS_USB	T
U	P204	P202	P314	VSS_13	P808	P100	P500	P015	VREFH	VREFH0	P008	P006	P000	P002	P511	P814/USB_DP	VCC_USB	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 1.4 Pin assignment for without_MIPI_BGA 289-pin

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	NC	PA11	P114	P112	P300	VLO	VLO	VSS_DCDC	VCC_DCDC	VCC_DCDC	P309	P312	P908	P905	P206	A
B	P610	PA12	P115	P113	P302	VLO	VLO	VSS_DCDC	VCC_DCDC	VCC_DCDC	P311	P310	P906	P907	P909	B
C	P612	P611	PA13	P609	P301	RES	P210/TMS/SWDIO	P211/TCK/SWCLK	P304	P306	P305	P307	PB03	PB00	PB01	C
D	P615	P613	P614	PA14	P200	P208/TDI	P201/MD	P209/TDO	P902	P308	PB02	PB04	P705	P707	P706	D
E	PA15	PA08	P813	PA09	VCC_08	VSS_08	VSS5	VCL5	VSS_07	VCC_07	P405	P702	P704	P406	P701	E
F	PA06	PA10	PA05	PA07	VCC_09	VSS_09	VSS6	VCL6	VCL4	VSS4	P700	P703	VSS_03	VCC_05	VSS_05	F
G	PA04	PA02	PA01	PA03	VCC_10	VSS_10	VSS7	VCL7	VCL3	VSS3	P404	VCC_03	VCC_USBHS	USBHS_DP	USBHS_DM	G
H	PA00	P504	P503	P505	PC14	VSS_15	VSS8	VCL8	VCL2	VSS2	P403	VSS_02	USBHS_RREF	VSS2_USBHS	VSS1_USBHS	H
J	P506	P510	P507	P508	PC12	VCC2_15	VSS9	VCL9	VCL1	VSS1	P402	VCC_02	AVCC_USBHS	P213/XTAL	P212/EXTAL	J
K	PC15	P608	PD00	P509	VCC2_14	VSS_14	VSS10	VCL10	VCL0	VSS0	P410	P407	VCC_01	P214/XCOUT	P215/XCIN/EXCIN	K
L	PC13	P604	P603	P107	P106	P104	P105	VSS11	VCL11	P409	P414	P408	P415	VBATT	VSS_01	L
M	PC11	P602	P600	P601	P102	P801	P803	P009	P007	P708	P411	P710	P709	P711	P401	M
N	VCC2_12	VCC18_MIPI	VSS_MIPI	P103	P101	P802	P804	AVCC0	AVSS0	P005	P001	P712	P714	P713	P400	N
P	MIPI_DL0_P	MIPI_CL_P	MIPI_DL1_P	AVCC_MIPI	P809	P800	P015	VREFL	VREFL0	P006	P002	P003	P512	P815/USB_DM	VSS_USB	P
R	MIPI_DL0_N	MIPI_CL_N	MIPI_DL1_N	VSS_12	P808	P100	P014	VREFH	VREFH0	P008	P004	P000	P511	P814/USB_DP	VCC_USB	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Figure 1.5 Pin assignment for BGA 224-pin

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	NC	PA11	P114	P112	P300	VLO	VLO	VSS_DCDC	VCC_DCDC	VCC_DCDC	P309	P312	P908	P905	P206	A
B	P610	PA12	P115	P113	P302	VLO	VLO	VSS_DCDC	VCC_DCDC	VCC_DCDC	P311	P310	P906	P907	P909	B
C	P612	P611	PA13	P609	P301	RES	P210/TMS/SWDIO	P211/TCK/SWCLK	P304	P306	P305	P307	PB03	PB00	PB01	C
D	P615	P613	P614	PA14	P200	P208/TDI	P201/MD	P209/TDO	P902	P308	PB02	PB04	P705	P707	P706	D
E	PA15	PA08	P813	PA09	VCC_08	VSS_08	VSS5	VCL5	VSS_07	VCC_07	P405	P702	P704	P406	P701	E
F	PA06	PA10	PA05	PA07	VCC_09	VSS_09	VSS6	VCL6	VCL4	VSS4	P700	P703	VSS_03	VCC_05	VSS_05	F
G	PA04	PA02	PA01	PA03	VCC_10	VSS_10	VSS7	VCL7	VCL3	VSS3	P404	VCC_03	VCC_USBHS	USBHS_DP	USBHS_DM	G
H	PA00	P504	P503	P505	PC14	VSS_15	VSS8	VCL8	VCL2	VSS2	P403	VSS_02	USBHS_RREF	VSS2_USBHS	VSS1_USBHS	H
J	P506	P510	P507	P508	PC12	VCC2_15	VSS9	VCL9	VCL1	VSS1	P402	VCC_02	AVCC_USBHS	P213/XTAL	P212/EXTAL	J
K	PC15	P608	PD00	P509	VCC2_14	VSS_14	VSS10	VCL10	VCL0	VSS0	P410	P407	VCC_01	P214/XCOUT	P215/XCIN/EXCIN	K
L	PC13	P604	P603	P107	P106	P104	P105	VSS11	VCL11	P409	P414	P408	P415	VBATT	VSS_01	L
M	PC11	P602	P600	P601	P102	P801	P803	P009	P007	P708	P411	P710	P709	P711	P401	M
N	VCC2_12	P315	VSS_13	P103	P101	P802	P804	AVCC0	AVSS0	P005	P001	P712	P714	P713	P400	N
P	P205	P203	P313	VCC2_13	P809	P800	P015	VREFL	VREFL0	P006	P002	P003	P512	P815/USB_DM	VSS_USB	P
R	P204	P202	P314	VSS_12	P808	P100	P014	VREFH	VREFH0	P008	P004	P000	P511	P814/USB_DP	VCC_USB	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Figure 1.6 Pin assignment for without_MIPI_BGA 224-pin

1.7 Pin Lists

Table 1.17 Pin list (1 of 8)

BGA289	BGA289 without MIPI	BGA224	BGA224 without MIPI	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/ USBHS/OSPI/SSIE/SDHI/MMC/ ESWM(GMII,RGMII,MII,RMII)/ PDMIF	GPT/AGT/ULPT/RTC	ADC16/ DAC12/ ACMPHS	MIPI/ GLCDC/ CEU
A1	A1	C4	C4	—	P609	D7/DQ7	IRQ29	TXD0_C/SDA0_C/MOSI0_C/ MISOA_B/CTX1	GTIU/GTIOC5B/ULPTOA1-DS	—	—
A2	A2	B4	B4	—	P113	D4/DQ4	IRQ28	RXD0_A/SCL0_A/MISO0_A/ SSLA1_B/SSILRCK0/SSIFS0_B/ SD0DAT5	GTIOC2A/ULPTOA0-DS	—	—
A3	A3	B3	B3	—	P115	D6/DQ6	IRQ31-DS	CTS0_A/MOSIA_B/SSITXD0_B/ SD0DAT7	GTIOC5A	—	—
A4	A4	A4	A4	—	P112	D3/DQ3	IRQ27	TXD0_A/SDA0_A/MOSI0_A/ SSLA2_B/SSIBCK0_B/SD0DAT4	GTIOC3B/ULPTOB0-DS	—	—
A5	A5	B5	B5	—	P302	D0/DQ0	IRQ5	RXD6_B/SCL6_B/MISO6_B/ SD0DAT1	GTOUUP/GTIOC4A/ ULPTO0-DS	—	—
A6	A6	—	—	—	P915	—	IRQ8	CTS6_B	GTIOC5A	—	—
A7	A7	A6	A6	VLO	—	—	—	—	—	—	—
A8	A8	A7	A7	VLO	—	—	—	—	—	—	—
A9	A9	A8	A8	VSS_DCDC	—	—	—	—	—	—	—
A10	A10	A9	A9	VCC_DCDC	—	—	—	—	—	—	—
A11	A11	A10	A10	VCC_DCDC	—	—	—	—	—	—	—
A12	A12	A11	A11	—	P309	—	IRQ25-DS	CTS9_B/ET1_GTX_CLK/ RGMII1_TXC	GTCPPO8	—	VIO_D10
A13	A13	B13	B13	—	P906	—	IRQ9	CTS6_A/SSILRCK1/SSIFS1_A/ ET1_RXD0/RGMII1_RXD0/ RMII1_RXD0/PDMDAT0	GTIOC13B/ULPTO1	—	VIO_D5
A14	A14	A14	A14	—	P905	—	IRQ8	RXD3_B/SCL3_B/MISO3_B/ ET1_RX_CLK/RGMII1_RXC/ RMII1_REF50CK/PDMDAT1	GTCPPO13	—	VIO_D6
A15	A15	B14	B14	—	P907	—	IRQ10	SCK6_A/DE6/SSIBCK1_A/ ET1_RXD1/RGMII1_RXD1/ RMII1_RXD1/PDMCLK2	GTIOC13A/ULPTEE1	—	VIO_D4
A16	A16	—	—	—	P904	—	IRQ2	ET1_RXD4	GTIOC11B	—	—
A17	A17	—	—	—	P207	—	IRQ25	ET1_RXD5	GTCPPO3	—	—
B1	B1	E3	E3	—	P813	SDCS	IRQ15	SCK7_A/DE7/PDMCLK2	GTIOC7B	—	VIO_D13
B2	B2	B2	B2	—	PA12	D9/DQ9	IRQ11	RXD9_C/SCL9_C/MISO9_C	GTIW/GTIOC6B	—	—
B3	B3	A3	A3	—	P114	D5/DQ5	IRQ30-DS	CTS_RTS0_A/SS0_A/DE0/ SSLA0_B/SSIRXD0_B/SD0DAT6	GTIOC2B	—	—
B4	B4	A2	A2	—	PA11	D8/DQ8	IRQ10	SCK9_C/DE9	GTIV/GTIOC6A	—	—
B5	B5	A5	A5	—	P300	D2/DQ2	IRQ4	SCK0_A/DE0/SSLA3_B/SD0DAT3	GTIOC3A/ULPTEVI0-DS	—	—
B6	B6	—	—	—	P303	—	IRQ29-DS	SCK6_B/DE6	GTIOC7B	—	—
B7	B7	B6	B6	VLO	—	—	—	—	—	—	—
B8	B8	B7	B7	VLO	—	—	—	—	—	—	—
B9	B9	B8	B8	VSS_DCDC	—	—	—	—	—	—	—
B10	B10	B9	B9	VCC_DCDC	—	—	—	—	—	—	—
B11	B11	B10	B10	VCC_DCDC	—	—	—	—	—	—	—
B12	B12	B11	B11	—	P311	—	IRQ23-DS	SCK3_B/DE3/CRX0/ET1_TX_CLK	GTADSM1/GTCPPO6/ AGTOB1	—	VIO_D8
B13	B13	A13	A13	—	P908	—	IRQ11	TXD6_A/SDA6_A/MOSI6_A/ CRX1/ET1_RXD2/RGMII1_RXD2/ PDMCLK1	GTIOC12B/ULPTEVI1	—	VIO_D3
B14	B14	B15	B15	—	P909	—	IRQ21-DS	RXD6_A/SCL6_A/MISO6_A/ CTX1/ET1_RXD3/RGMII1_RXD3/ PDMCLK0	GTIOC12A/ULPTOA1	—	VIO_D2
B15	B15	A15	A15	—	P206	CS7#	IRQ0-DS	SSIDATA1_A/SD0DAT7/ ET1_RX_DV/RGMII1_RX_CTL/ RMII1_CRS_DV	GTIU/GTCPPO0/ULPTOB1	—	VIO_D0
B16	B16	—	—	—	PD01	—	IRQ22	SCK8_C/DE8/SD0DAT2/ET1_RXD6	GTCPPO2	—	—
B17	B17	—	—	—	PD02	—	IRQ21	TXD8_C/SDA8_C/MOSI8_C/ SD0DAT1/ET1_RXD7	GTCPPO1	—	—
C1	C1	F1	F1	—	PA06	CS1#/CKE	IRQ17	CTS2_C/SD0DAT1/PDMDAT1	GTIOC7B	—	VIO_D11
C2	C2	D2	D2	—	P613	D15/ DQ15	IRQ19	CTS0_C	GTIOC9B/AGTO1	—	—

Table 1.17 Pin list (2 of 8)

BGA289	BGA289 without MIPI	BGA224	BGA224 without MIPI	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/ USBHS/OSPI/SSIE/SDHI/MMC/ ESWM(GMII,RGMII,MII,RMII)/ PDMIF	GPT/AGT/ULPT/RTC	ADC16/ DAC12/ ACMPHS	MIPI/ GLCDC/ CEU
C3	C3	C3	C3	—	PA13	D10/ DQ10	IRQ12	CTS_RTS9_C/SS9_C/DE9	GTOVUP/GTIOC10A	—	—
C4	C4	C5	C5	—	P301	D1/DQ1	IRQ6	TXD6_B/SDA6_B/MOSI6_B/ SD0DAT2	GTOULO/GTIOC4B/ AGTIO0/ULPTEE0-DS	—	—
C5	C5	D5	D5	—	P200	—	NMI	—	—	—	—
C6	C6	C7	C7	TMS/SWDIO	P210	—	IRQ24	CTS_RTS9_B/SS9_B/DE9	GTOULO/GTIOC0B	—	—
C7	C7	D6	D6	TDI	P208	—	IRQ3	RXD9_B/SCL9_B/MISO9_B/CRX1	GTOVLO/GTIOC1B	—	—
C8	C8	—	—	—	P110	—	IRQ20	SD0DAT4	GTIOC9B	—	—
C9	C9	D10	D10	—	P308	—	IRQ26-DS	CTS3_B/SD0CLK/ET1_TX_ER	GTIU/GTCPPO9/ULPTOB1	—	VIO_D11
C10	C10	C11	C11	—	P305	—	IRQ8	SD0WP/ET1_TXD2/RGMII1_TXD2	GTOVUP/GTCPPO12/ ULPTEE1	—	VIO_D14
C11	C11	C12	C12	—	P307	—	IRQ27-DS	CTS_RTS6_A/SS6_A/DE6/ SD0CMD/ET1_TXD0/ RGMII1_TXD0/RMII1_TXD0	GTIV/GTCPPO10/ULPTOA1	—	VIO_D12
C12	C12	—	—	—	P911	—	IRQ6	ET1_TXD5	GTIOC3B	—	—
C13	C13	A12	A12	—	P312	—	IRQ22-DS	CTS_RTS3_B/SS3_B/DE3/CTX0/ ET1_RX_ER/RMII1_RX_ER/ PDMDAT2	GTADSM0/GTCPPO5/ AGTOA1	—	VIO_D7
C14	C14	—	—	—	PD04	—	IRQ20	CTS_RTS8_C/SS8_C/DE8/ SD0CMD/ET0_RXD5	GTIOC3A	—	—
C15	C15	—	—	—	PD03	—	IRQ21	RXD8_C/SCL8_C/MISO8_C/ SD0DAT0/ET0_RXD4	GTIOC3B	—	—
C16	C16	—	—	—	PD05	—	IRQ19	CTS8_C/SD0CLK/ET0_RXD6	GTIOC2B	—	—
C17	C17	—	—	—	PD06	—	IRQ18	SD0WP/ET0_RXD7	GTIOC2A	—	—
D1	D1	G1	G1	—	PA04	A1/ DQM3	IRQ19	SCK2_C/DE2/SD0DAT3	GTIU/GTIOC4B	—	VIO_D9
D2	D2	C2	C2	—	P611	D13/ DQ13	IRQ17	SCK0_C/DE0/MOSIA_B	GTOULO/GTIOC4B	—	—
D3	D3	B1	B1	—	P610	D12/ DQ12	IRQ16	RXD0_C/SCL0_C/MISO0_C/ RSPCKA_B/CRX1	GTOUUP/GTIOC4A/ ULPTOB1-DS	—	—
D4	D4	D4	D4	—	PA14	D11/ DQ11	IRQ13	TXD9_C/SDA9_C/MOSI9_C	GTOVLO/GTIOC10B	—	—
D5	D5	C6	C6	RES	—	—	—	—	—	—	—
D6	D6	C8	C8	TCK/SWCLK	P211	—	IRQ23	SCK9_B/DE9	GTOUUP/GTIOC0A	—	—
D7	D7	—	—	—	P109	—	IRQ23	SD0DAT5	GTIOC10A	—	—
D8	D8	—	—	—	P108	—	IRQ24	SD0DAT6	GTIOC10B	—	—
D9	D9	—	—	—	P903	—	IRQ1	—	GTIOC11A	—	—
D10	D10	C9	C9	—	P304	—	IRQ9	SD0DAT0/ET1_TXD3/RGMII1_TXD3	GTOVLO/GTIOC7A/ULPTO1	—	VIO_D15
D11	D11	C10	C10	—	P306	—	IRQ28-DS	SD0CD/ET1_TXD1/RGMII1_TXD1/ RMII1_TXD1	GTIW/GTCPPO11/ ULPTEVI1	—	VIO_D13
D12	D12	—	—	—	P912	—	IRQ5	ET1_TXD6	GTIOC3A	—	—
D13	D13	D12	D12	—	PB04	—	IRQ9	SCK5_C/DE5/ET0_TXD3/ RGMII0_TXD3	GTCPPO3	—	VIO_CLK
D14	D14	—	—	—	PB07	—	IRQ1	ET0_TXD5	GTIOC9B	—	—
D15	D15	—	—	—	PB05	—	IRQ15	CTS5_C/ET0_TXD7	GTCPPO4	—	—
D16	D16	C13	C13	—	PB03	—	IRQ13	TXD5_C/SDA5_C/MOSI5_C/ ET0_TXD2/RGMII0_TXD2	GTCPPO1	—	VIO_HD
D17	D17	C15	C15	—	PB01	ALE	IRQ12	CTS_RTS1_B/SS1_B/DE1/ ET0_TX_CLK	GTCPPO2	—	VIO_FLD
E1	E1	E1	E1	—	PA15	EBCLK/ SDCLK	IRQ14	CTS9_C/PDMCLK1	GTIOC7A	—	VIO_D14
E2	E2	D1	D1	—	P615	WR2/BC2/ DQM2	IRQ7	TXD7_A/SDA7_A/MOSI7_A	GTCPPO10	—	—
E3	E3	D3	D3	—	P614	WR/WR0/DQM0	IRQ20	RXD7_A/SCL7_A/MISO7_A	GTCPPO9/AGTO0	—	—
E4	E4	C1	C1	—	P612	D14/ DQ14	IRQ18	CTS_RTS0_C/SS0_C/DE0/ SSLA0_B	GTIOC9A	—	—
E5	E5	—	—	—	P914	—	IRQ9	CTS_RTS6_B/SS6_B/DE6	GTIOC5B	—	—
E6	E6	D7	D7	MD	P201	—	IRQ4	—	—	—	—
E7	E7	D8	D8	TDO	P209	—	IRQ25	TXD9_B/SDA9_B/MOSI9_B/CTX1	GTOVUP/GTIOC1A	—	—

Table 1.17 Pin list (3 of 8)

BGA289	BGA289 without MIPI	BGA224	BGA224 without MIPI	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/ USBHS/OSPI/SSIE/SDHI/MMC/ ESWM(GMII,RGMII,MII,RMII)/ PDMIF	GPT/AGT/ULPT/RTC	ADC16/ DAC12/ ACMPHS	MIPI/ GLCDC/ CEU
E8	E8	—	—	—	P111	—	IRQ19	SD0DAT3	GTIOC9A	—	—
E9	E9	D9	D9	—	P902	ALE	IRQ0	AUDIO_CLK	GTCPPO13	—	VIO_D1
E10	E10	B12	B12	—	P310	—	IRQ24-DS	TXD3_B/SDA3_B/MOSI3_B/ ET1_TX_EN/RGMII1_TX_CTL/ RMII1_TX_EN	GTCPPO7/AGTEE1	—	VIO_D9
E11	E11	—	—	—	P910	—	IRQ7	ET1_TXD4	GTCPPO12	—	—
E12	E12	—	—	—	P913	—	IRQ3	ET1_TXD7	GTCPPO11	—	—
E13	E13	D11	D11	—	PB02	—	IRQ11	RXD5_C/SCL5_C/MISO5_C/ ET0_TXD1/RGMII0_TXD1/ RMII0_TXD1	GTCPPO0	—	VIO_VD
E14	E14	—	—	—	PB06	—	IRQ0	CTS_RTS5_C/SS5_C/DE5/ ET0_TXD6	GTIOC9A	—	—
E15	E15	—	—	—	PD07	—	IRQ17	SD0CD/ET0_TXD4	GTCPPO0	—	—
E16	E16	C14	C14	—	PB00	—	IRQ10	SCK1_B/DE1/ET0_TXD0/ RGMII0_TXD0/RMII0_TXD0/ PDMDAT2	GTCPPO4	—	—
E17	E17	D15	D15	—	P706	—	IRQ7	RXD1_B/SCL1_B/MISO1_B/ ET0_GTX_CLK/RGMII0_TXC/ PDMDAT0	GTCPPO2/AGTIO0	—	VIO_D10
F1	F1	G2	G2	—	PA02	A3	IRQ31	RXD2_C/SCL2_C/MISO2_C/ SD0DAT5	GTIW/GTCPPO9	—	VIO_D7
F2	F2	F2	F2	—	PA10	CS2#/RAS	IRQ4	SCK5_B/DE5/PDMCLK0	GTCPPO13	—	VIO_D15
F3	F3	E2	E2	—	PA08	CS0#/WE	IRQ6	RXD5_B/SCL5_B/MISO5_B	GTCPPO11	—	—
F4	F4	E4	E4	—	PA09	CS3#/CAS	IRQ5	TXD5_B/SDA5_B/MOSI5_B	GTCPPO12	—	—
F5	F5	H5	H5	—	PC14	D16/ DQ16	IRQ0	TXD6_C/SDA6_C/MOSI6_C/ ET0_WOL	GTADSM1/GTCPPO9	—	—
F6	F6	E5	E5	VCC_08	—	—	—	—	—	—	—
F7	F7	E6	E6	VSS_08	—	—	—	—	—	—	—
F8	F8	G10	G10	VSS3	—	—	—	—	—	—	—
F9	F9	G9	G9	VCL3	—	—	—	—	—	—	—
F10	F10	E9	E9	VSS_07	—	—	—	—	—	—	—
F11	F11	E10	E10	VCC_07	—	—	—	—	—	—	—
F12	F12	F11	F11	—	P700	—	IRQ16-DS	RXD2_B/SCL2_B/MISO2_B/ MISOA_C/SSIDATA1_B/SD1WP/ ET0_RXD2/RGMII0_RXD2	GTIOC5A	—	VIO_D4
F13	F13	E12	E12	—	P702	—	IRQ18-DS	CTS2_B/RSPCKA_C/SSIBCK1_B/ SD1DAT5/ET0_RXD0/ RGMII0_RXD0/RMII0_RXD0	GTIOC6A/ULPTO0	—	VIO_D6
F14	F14	E14	E14	—	P406	—	IRQ31	TXD2_B/SDA2_B/MOSI2_B/ SSLA3_C/SSIRXD0_A/SD1CD/ ET0_RXD3/RGMII0_RXD3	GTIOC1B	—	VIO_D3
F15	F15	E15	E15	—	P701	—	IRQ17-DS	CTS_RTS2_B/SS2_B/DE2/ MOSIA_C/SSILRCK1/SSIFS1_B/ SD1DAT4/ET0_RXD1/ RGMII0_RXD1/RMII0_RXD1	GTIOC5B/ULPTO1	—	VIO_D5
F16	F16	D14	D14	—	P707	—	IRQ8	TXD1_B/SDA1_B/MOSI1_B/ ET0_TX_ER/PDMDAT1	GTCPPO3	—	VIO_D11
F17	F17	D13	D13	—	P705	—	IRQ19	CTS1_B/SSLA2_C/CRX0/ ET0_TX_EN/RGMII0_TX_CTL/ RMII0_TX_EN/PDMCLK2	GTADSM1/GTCPPO1/ AGTIO0	—	VIO_D9
G1	G1	H1	H1	—	PA00	A5	IRQ22	CTS_RTS5_B/SS5_B/DE5/ SD0DAT7	GTOVLO/GTCPPO7	—	VIO_D5
G2	G2	G4	G4	—	PA03	A2	IRQ20	TXD2_C/SDA2_C/MOSI2_C/ SD0DAT4	GTIV/GTCPPO10	—	VIO_D8
G3	G3	F3	F3	—	PA05	A0/BC0/ DQM1	IRQ18	CTS_RTS2_C/SS2_C/DE2/ SD0DAT2/PDMDAT2	GTIOC4A	—	VIO_D10
G4	G4	F4	F4	—	PA07	RD	IRQ16	CTS7_A/SD0DAT0/PDMDAT0	GTIOC7A	—	VIO_D12
G5	G5	J5	J5	—	PC12	D18/ DQ18	IRQ2	SCK6_C/DE6/ET0_MDIO	GTCPPO11	—	—
G6	G6	F5	F5	VCC_09	—	—	—	—	—	—	—
G7	G7	F6	F6	VSS_09	—	—	—	—	—	—	—
G8	G8	F10	F10	VSS4	—	—	—	—	—	—	—

Table 1.17 Pin list (4 of 8)

BGA289	BGA289 without MIPI	BGA224	BGA224 without MIPI	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/ USBHS/OSPI/SSIE/SDHI/MMC/ ESWM(GMII,RGMII,MII,RMII)/ PDMIF	GPT/AGT/ULPT/RTC	ADC16/ DAC12/ ACMPHS	MIPI/ GLCDC/ CEU
G9	G9	F9	F9	VCL4	—	—	—	—	—	—	—
G10	G10	—	—	VSS_06	—	—	—	—	—	—	—
G11	G11	—	—	VCC_06	—	—	—	—	—	—	—
G12	G12	E11	E11	—	P405	—	IRQ30	SCK2_B/DE2/SSITXD0_A/ SD1DAT3/ET0_RX_DV/ RGMII0_RX_CTL/RMII0_CRS_DV	GTIOC1A/AGTIO1	—	VIO_D2
G13	G13	E13	E13	—	P704	—	IRQ26	SSLA1_C/CTX0/SD1DAT7/ ET0_RX_ER/RMII0_RX_ER/ PDMCLK1	GTADSM0/GTCPPO0/ AGTO0	—	VIO_D8
G14	G14	F12	F12	—	P703	—	IRQ19-DS	SSLA0_C/SD1DAT6/ET0_RX_CLK/ RGMII0_RXC/RMII0_REF50CK/ PDMCLK0	GTIOC6B/AGTO1	—	VIO_D7
G15	G15	F13	F13	VSS_03	—	—	—	—	—	—	—
G16	G16	F14	F14	VCC_05	—	—	—	—	—	—	—
G17	G17	F15	F15	VSS_05	—	—	—	—	—	—	—
H1	H1	H2	H2	—	P504	A7	IRQ7	SD0WP	GTOULO/GTCPPO1	—	VIO_D3
H2	H2	H3	H3	—	P503	A6	IRQ6	SD0CD	GTOUUP/GTCPPO6	—	VIO_D4
H3	H3	H4	H4	—	P505	A8	IRQ8	SD0CLK	GTOWUP/GTCPPO2	—	VIO_D2
H4	H4	G3	G3	—	PA01	A4	IRQ21	CTS5_B/SD0DAT6	GTOVUP/GTCPPO8	—	VIO_D6
H5	H5	M1	M1	—	PC11	D19/ DQ19	IRQ3	CTS_RTS6_C/SS6_C/DE6/ ET0_MDC	GTCPPO12	—	—
H6	H6	G5	G5	VCC_10	—	—	—	—	—	—	—
H7	H7	G6	G6	VSS_10	—	—	—	—	—	—	—
H8	H8	G7	G7	VSS7	—	—	—	—	—	—	—
H9	H9	E8	E8	VCL5	—	—	—	—	—	—	—
H10	H10	E7	E7	VSS5	—	—	—	—	—	—	—
H11	H11	—	—	VCC_04	—	—	—	—	—	—	—
H12	H12	—	—	VSS_04	—	—	—	—	—	—	—
H13	H13	H11	H11	—	P403	—	IRQ14-DS	CTS_RTS1_A/SS1_A/DE1/ SSIBCK0_A/SD1DAT1/ET1_WOL	GTIOC3A/RTCIC1	—	—
H14	H14	G12	G12	VCC_03	—	—	—	—	—	—	—
H15	H15	G13	G13	VCC_USBHS	—	—	—	—	—	—	—
H16	H16	G14	G14	USBHS_DP	—	—	—	—	—	—	—
H17	H17	G15	G15	USBHS_DM	—	—	—	—	—	—	—
J1	J1	J1	J1	—	P506	A9	IRQ9	SD0CMD	GTOWLO/GTCPPO3	—	VIO_D1
J2	J2	J3	J3	—	P507	A10	IRQ10	CTS_RTS7_A/SS7_A/DE7/ ET_TAS_STA0	GTADSM0/GTIOC0A	—	VIO_D0
J3	J3	J4	J4	—	P508	A11	IRQ1	CTS5_A/ET_TAS_STA1	GTADSM1/GTIOC0B	—	VIO_VD
J4	J4	K4	K4	—	P509	A12	IRQ2	CTS_RTS5_A/SS5_A/DE5/ ET_TAS_STA2	GTIOC1A/ULPTEVI1	—	VIO_HD
J5	J5	L1	L1	—	PC13	D17/ DQ17	IRQ1	RXD6_C/SCL6_C/MISO6_C/ ET0_INT	GTCPPO10	—	—
J6	J6	—	—	VCC2_11	—	—	—	—	—	—	—
J7	J7	—	—	VSS_11	—	—	—	—	—	—	—
J8	J8	G8	G8	VCL7	—	—	—	—	—	—	—
J9	J9	F8	F8	VCL6	—	—	—	—	—	—	—
J10	J10	F7	F7	VSS6	—	—	—	—	—	—	—
J11	J11	H9	H9	VCL2	—	—	—	—	—	—	—
J12	J12	H10	H10	VSS2	—	—	—	—	—	—	—
J13	J13	G11	G11	—	P404	—	IRQ15-DS	CTS1_A/SSILRCK0/SSIFS0_A/ SD1DAT2/ET0_WOL	GTIOC3B/RTCIC2	—	—
J14	J14	H12	H12	VSS_02	—	—	—	—	—	—	—
J15	J15	H13	H13	USBHS_RREF	—	—	—	—	—	—	—
J16	J16	H14	H14	VSS2_USBHS	—	—	—	—	—	—	—
J17	J17	H15	H15	VSS1_USBHS	—	—	—	—	—	—	—
K1	K1	K1	K1	—	PC15	A16	IRQ30	CTS6_C/CRX1	GTADSM0	—	—

Table 1.17 Pin list (5 of 8)

BGA289	BGA289 without MIPI	BGA224	BGA224 without MIPI	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/ USBHS/OSPI/SSIE/SDHI/MMC/ ESWM(GMII,RGMII,MII,RMII)/ PDMIF	GPT/AGT/ULPT/RTC	ADC16/ DAC12/ ACMPHS	MIPI/ GLCDC/ CEU
K2	K2	K2	K2	—	P608	A14	IRQ22	TXD5_A/SDA5_A/MOSI5_A	GTOWUP/GTCPPO4	—	VIO_FLD
K3	K3	J2	J2	—	P510	A13	IRQ3	RXD5_A/SCL5_A/MISO5_A/ ET_TAS_STA3	GTIOC1B/ULPTEVI0	—	VIO_CLK
K4	K4	K3	K3	—	PD00	A15	IRQ23	SCK5_A/DE5/CTX1	GTOWLO/GTCPPO5	—	—
K5	K5	—	—	—	PC07	D23/ DQ23	IRQ21	OM_1_RESET	GTCPPO0	—	—
K6	K6	R4	R4	VSS_12	—	—	—	—	—	—	—
K7	K7	J7	J7	VSS9	—	—	—	—	—	—	—
K8	K8	J8	J8	VCL9	—	—	—	—	—	—	—
K9	K9	H8	H8	VCL8	—	—	—	—	—	—	—
K10	K10	H7	H7	VSS8	—	—	—	—	—	—	—
K11	K11	J9	J9	VCL1	—	—	—	—	—	—	—
K12	K12	J10	J10	VSS1	—	—	—	—	—	—	—
K13	K13	K11	K11	—	P410	A19	IRQ5	SCK3_A/DE3/SCL0_A/ GPTP0_MATCH	GTOVLO/GTIOC9B/ AGTOB1	—	—
K14	K14	J12	J12	VCC_02	—	—	—	—	—	—	—
K15	K15	J13	J13	AVCC_USBHS	—	—	—	—	—	—	—
K16	K16	J14	J14	XTAL	P213	—	IRQ2	TXD1_C/SDA1_C/MOSI1_C	GTIOC0A/ULPTEE0	—	—
K17	K17	J15	J15	EXTAL	P212	—	IRQ3	RXD1_C/SCL1_C/MISO1_C	GTIOC0B/AGTEE1	—	—
L1	L1	—	—	—	PC03	D27/ DQ27	IRQ25	TXD7_C/SDA7_C/MOSI7_C/ OM_1_SIO4	GTCPPO4	—	—
L2	L2	—	—	—	PC02	D28/ DQ28	IRQ26	SCK7_C/DE7/OM_1_SIO3	GTCPPO5	—	—
L3	L3	—	—	—	PC04	D26/ DQ26	IRQ24	RXD7_C/SCL7_C/MISO7_C/ OM_1_SIO2	GTCPPO3	—	—
L4	L4	—	—	—	PC09	D21/ DQ21	IRQ5	OM_1_RSTO1	—	—	—
L5	L5	—	—	—	PC05	D25/ DQ25	IRQ23	OM_1_CS1	GTCPPO2	—	—
L6	L6	N1	N1	VCC2_12	—	—	—	—	—	—	—
L7	L7	K6	K6	VSS_14	—	—	—	—	—	—	—
L8	L8	H6	H6	VSS_15	—	—	—	—	—	—	—
L9	L9	K7	K7	VSS10	—	—	—	—	—	—	—
L10	L10	K8	K8	VCL10	—	—	—	—	—	—	—
L11	L11	K9	K9	VCL0	—	—	—	—	—	—	—
L12	L12	K10	K10	VSS0	—	—	—	—	—	—	—
L13	L13	L11	L11	—	P414	A23	IRQ9	RXD4_B/SCL4_B/MISO4_B/ SSLB0_B/CRX1/ET1_MDIO	GTIOC0B	—	VIO_CLK
L14	L14	J11	J11	—	P402	—	IRQ4-DS	SCK1_A/DE1/CRX0/AUDIO_CLK/ SD1DAT0/ET0_LINKSTA	RTCIC0	—	—
L15	L15	K13	K13	VCC_01	—	—	—	—	—	—	—
L16	L16	K14	K14	XCOUT	P214	—	IRQ21	—	—	—	—
L17	L17	K15	K15	XCIN/EXCIN	P215	—	IRQ20	—	—	—	—
M1	M1	—	—	—	PC00	D30/ DQ30	IRQ28	CTS_RTS7_C/SS7_C/DE7/ OM_1_SIO5	GTCPPO7	—	—
M2	M2	—	—	—	P607	D31/ DQ31	IRQ23	OM_1_DQS	—	—	—
M3	M3	—	—	—	PC01	D29/ DQ29	IRQ27	CTS7_C/OM_1_SIO0	GTCPPO6	—	—
M4	M4	—	—	—	PC08	D22/ DQ22	IRQ29	OM_1_CS0	GTCPPO8	—	—
M5	M5	—	—	—	PC10	D20/ DQ20	IRQ4	OM_1_WP1	GTCPPO13	—	—
M6	M6	L6	L6	—	P104	—	IRQ1	CTS9_A/SSLB1_A/OM_0_CS1/ GPTP0_MATCH	GTIOC1B	—	—
M7	M7	K5	K5	VCC2_14	—	—	—	—	—	—	—
M8	M8	J6	J6	VCC2_15	—	—	—	—	—	—	—
M9	M9	—	—	—	P810	—	IRQ21	SCK7_B/DE7/SD1DAT2/PDMCLK0	GTIOC10A/ULPTOA0	—	—

Table 1.17 Pin list (6 of 8)

BGA289	BGA289 without MIPI	BGA224	BGA224 without MIPI	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/ USBHS/OSPI/SSIE/SDHI/MMC/ ESWM(GMII,RGMII,MII,RMII)/ PDMIF	GPT/AGT/ULPT/RTC	ADC16/ DAC12/ ACMPHS	MIPI/ GLCDC/ CEU
M10	M10	L8	L8	VSS11	—	—	—	—	—	—	—
M11	M11	L9	L9	VCL11	—	—	—	—	—	—	—
M12	M12	—	—	—	P412	A21	IRQ20-DS	CTS3_A/GPTP_PTPOUT0	GTOULO/GTCPPO8/ AGTEE1	—	—
M13	M13	M12	M12	—	P710	CS5#	IRQ17	CTS4_B/SSLB3_B/ET0_LINKSTA	GTIOC11B	—	VIO_D12
M14	M14	M11	M11	—	P411	A20	IRQ4	CTS_RTS3_A/SS3_A/DE3/ GPTP_PTPOUT1	GTOVUP/GTIOC9A/ AGTOA1	—	DSI_TE
M15	M15	L12	L12	—	P408	A17	IRQ7	RXD3_A/SCL3_A/MISO3_A/ SCL0_B/GPTP_PTPOUT2	GTOWLO/GTIOC10A/ ULPTOB0	—	—
M16	M16	L14	L14	VBATT	—	—	—	—	—	—	—
M17	M17	L15	L15	VSS_01	—	—	—	—	—	—	—
N1	N1	—	—	—	P605	—	IRQ25	CTS0_B/OM_1_SIO1	GTIOC8A	—	—
N2	N2	L2	L2	—	P604	—	IRQ26	CTS_RTS0_B/SS0_B/DE0/ OM_1_SIO7	GTIOC8B	—	—
N3	N3	—	—	—	P606	WR3/BC3	IRQ24	OM_1_SIO6	—	—	—
N4	N4	—	—	—	PC06	D24/ DQ24	IRQ22	OM_1_ECSINT1	GTCPPO1	—	—
N5	N5	L4	L4	—	P107	—	IRQ31	CTS4_A/OM_0_CS0/ET1_INT	GTOWUP/GTIOC8A/ AGTOA0	—	—
N6	N6	L5	L5	—	P106	—	IRQ16	CTS8_B/SSLB3_A/OM_0_RESET/ ET1_LINKSTA	GTOWLO/GTIOC8B/ AGTOB0/ULPTEE1-DS	—	—
N7	N7	L7	L7	—	P105	—	IRQ0	CTS_RTS8_B/SS8_B/DE8/ SSLB2_A/OM_0_ECSINT1/ GPTP0_CAPTURE	GTIOC1A/ULPTO1-DS	—	—
N8	N8	—	—	—	P811	—	IRQ22	CTS7_B/SD1DAT3/PDMCLK1	GTIOC10B/ULPTOB0	—	—
N9	N9	—	—	—	P013	—	IRQ14	—	—	AN013	—
N10	N10	—	—	—	P011	—	IRQ16	—	—	AN011	—
N11	N11	—	—	—	P807	—	IRQ11	—	GTIOC13A	—	—
N12	N12	M10	M10	—	P708	WR1/BC1	IRQ11	SCK4_B/DE4/SDA2_A/MOSIB_B/ AUDIO_CLK/ET0_MDC	GTCPPO6	—	VIO_VD
N13	N13	N12	N12	—	P712	—	IRQ2	CTS1_C/SSLB1_B/ GPTP1_CAPTURE	GTIOC2B/AGTOB0	—	—
N14	N14	N13	N13	—	P714	—	IRQ13	TXD4_C/SDA4_C/MOSI4_C/ GPTP1_PPS	GTIOC12B	—	DSI_TE
N15	N15	M14	M14	—	P711	—	IRQ3	CTS_RTS1_C/SS1_C/DE1/ SSLB2_B/GPTP0_PPS	GTIOC11A/AGTEE0	—	—
N16	N16	N14	N14	—	P713	—	IRQ14	CTS4_C/GPTP1_MATCH	GTIOC2A/AGTOA0	—	—
N17	N17	M15	M15	—	P401	—	IRQ5-DS	RXD1_A/SCL1_A/MISO1_A/ I3C_SDA0/CTX0/SD1CMD	GTIOC6B	—	VIO_D1
P1	P1	L3	L3	—	P603	—	IRQ27	TXD0_B/SDA0_B/MOSI0_B/ OM_1_SCLK	GTIOC7A/ULPTO0	—	—
P2	P2	M2	M2	—	P602	—	IRQ28	RXD0_B/SCL0_B/MISO0_B/ OM_1_SCLKN	GTIOC7B/ULPTEE0	—	—
P3	P3	M3	M3	—	P600	—	IRQ30	OM_0_RSTO1/ET1_WOL	GTIOC6B/ULPTEVI1-DS	—	—
P4	P4	M4	M4	—	P601	—	IRQ29	SCK0_B/DE0/OM_0_WP1	GTIOC6A/ULPTEVI0/ RTCOUT	—	—
P5	P5	M5	M5	—	P102	—	IRQ17	TXD9_A/SDA9_A/MOSI9_A/ RSPCKB_A/CRX0/OM_0_SIO4	GTOWLO/GTIOC2B/AGTO0	—	—
P6	P6	M6	M6	—	P801	—	IRQ12	TXD2_A/SDA2_A/MOSI2_A/ OM_0_DQS/GPTP1_PPS	GTIV/GTIOC11B/AGTOB0	—	—
P7	P7	M7	M7	—	P803	—	IRQ19	SCK2_A/DE2/OM_0_SIO1	GTIOC12B	—	—
P8	P8	—	—	—	P812	—	IRQ23	CTS_RTS7_B/SS7_B/DE7/ SD1DAT4/PDMCLK2	GTIOC11A	AN022	—
P9	P9	—	—	—	P012	—	IRQ15	—	—	AN012	—
P10	P10	—	—	—	P010	—	IRQ14	—	—	AN010	—
P11	P11	M8	M8	—	P009	—	IRQ13-DS	—	—	AN009/ IVREF1	—
P12	P12	—	—	—	P805	—	IRQ30	TXD8_A/SDA8_A/MOSI8_A/ ET1_MDIO	—	AN017/ IVCMP0_0	VIO_D15
P13	P13	P13	P13	—	P512	—	IRQ14	CTS8_A/SCL1_A/CTX1/ET1_INT	GTIOC0A	—	—

Table 1.17 Pin list (7 of 8)

BGA289	BGA289 without MIPI	BGA224	BGA224 without MIPI	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/ USBHS/OSPI/SSIE/SDHI/MMC/ ESWM(GMII,RGMII,MII,RMII)/ PDMIF	GPT/AGT/ULPT/RTC	ADC16/ DAC12/ ACMPHS	MIPI/ GLCDC/ CEU
P14	P14	—	—	—	P413	A22	IRQ18	ET_TAS_STA3	GTOUUP/GTCPPO7/ ULPTEE1	—	—
P15	P15	—	—	—	P515	—	IRQ12	CTS_RTS4_C/SS4_C/DE4/SCL2_B/ ET_TAS_STA0	GTIOC13A	—	—
P16	P16	M13	M13	—	P709	CS4#	IRQ10	CTS_RTS4_B/SS4_B/DE4/SCL2_A/ MISOB_B/ET0_MDIO	GTCPPO5	—	VIO_D13
P17	P17	N15	N15	—	P400	—	IRQ0	TXD1_A/SDA1_A/MOSI1_A/ I3C_SCL0/AUDIO_CLK/SD1CLK	GTIOC6A/AGTIO1	—	VIO_D0
R1	R1	—	P4	VCC2_13	—	—	—	—	—	—	—
R2	—	N2	—	VCC18_MIPI	—	—	—	—	—	—	—
R3	—	N3	—	VSS_MIPI	—	—	—	—	—	—	—
—	R2	—	N2	—	P315	—	IRQ29	SCK3_C/DE3/SSLA3_A	—	—	—
—	R3	—	—	—	P900	—	IRQ30	CTS3_C	GTADSM0	—	—
R4	R4	N4	N4	—	P103	—	IRQ16	CTS_RTS9_A/SS9_A/DE9/ SSLB0_A/CTX0/OM_0_SIO2/ GPTP0_PPS	GTOWUP/GTIOC2A	—	—
R5	R5	N5	N5	—	P101	—	IRQ1	RXD9_A/SCL9_A/MISO9_A/ MOSIB_A/OM_0_SIO3/ GPTP1_CAPTURE	GTIOC8A/AGTEE0	—	—
R6	R6	N6	N6	—	P802	—	IRQ18	RXD2_A/SCL2_A/MISO2_A/ OM_0_SIO6	GTIW/GTIOC12A	—	—
R7	R7	N7	N7	—	P804	—	IRQ14	CTS_RTS2_A/SS2_A/DE2/ OM_0_SIO7	GTIOC13A	—	DSI_TE
R8	R8	—	—	—	P501	—	IRQ25	TXD8_B/SDA8_B/MOSI8_B/ SD1DAT6/PDMDAT1	GTIOC12A	AN020	—
R9	R9	N8	N8	AVCC0	—	—	—	—	—	—	—
R10	R10	N9	N9	AVSS0	—	—	—	—	—	—	—
R11	R11	N10	N10	—	P005	—	IRQ10-DS	—	—	AN005/ IVCMP3_ 2	—
R12	R12	P12	P12	—	P003	—	IRQ29	—	—	AN003/ IVCMP3_ 1	—
R13	R13	—	—	—	P513	—	IRQ31	SCK8_A/DE8/ET0_INT	GTIOC13B	AN016/ IVCMP0_ 1	VIO_FLD
R14	R14	—	—	—	P514	—	IRQ13	SCK4_C/DE4/SDA2_B/ ET_TAS_STA1	GTIOC13B	—	—
R15	R15	L13	L13	—	P415	WAIT	IRQ8	TXD4_B/SDA4_B/MOSI4_B/ RSPCKB_B/CTX1/ET1_MDC	GTIOC0A	—	VIO_HD
R16	R16	L10	L10	—	P409	A18	IRQ6	TXD3_A/SDA3_A/MOSI3_A/ SDA0_A/GPTP0_CAPTURE	GTOWUP/ULPTOA0	—	—
R17	R17	K12	K12	—	P407	CS6#	IRQ22	SCK1_C/DE1/SDA0_B/ GPTP_PTPOUT3	GTIOC10B/AGTIO0/ RTCOUT	—	—
T1	—	P1	—	MIPI_DL0_P	—	—	—	—	—	—	—
T2	—	P2	—	MIPI_CL_P	—	—	—	—	—	—	—
T3	—	P3	—	MIPI_DL1_P	—	—	—	—	—	—	—
T4	—	P4	—	AVCC_MIPI	—	—	—	—	—	—	—
—	T1	—	P1	—	P205	—	IRQ1-DS	TXD4_A/SDA4_A/MOSI4_A/ SCL1_B/SSLA1_A/SD1CD	GTIV/GTIOC4A/AGTO1	—	—
—	T2	—	P2	—	P203	—	IRQ2-DS	RXD4_A/SCL4_A/MISO4_A/ RSPCKA_A/CTX0/SD1CLK	GTIOC5A/ULPTOA1	—	—
—	T3	—	P3	—	P313	—	IRQ27	TXD3_C/SDA3_C/MOSI3_C/ MISOA_A/SD1DAT0	—	—	—
—	T4	—	—	—	P901	—	IRQ31	CTS_RTS3_C/SS3_C/DE3	GTADSM1/AGTIO1	—	—
T5	T5	P5	P5	—	P809	—	IRQ20	TXD7_B/SDA7_B/MOSI7_B/ OM_0_SCLKN	—	—	—
T6	T6	P6	P6	—	P800	—	IRQ11	CTS2_A/OM_0_SIO5	GTIU/GTIOC11A/AGTOA0	—	—
T7	T7	—	—	—	P502	—	IRQ26	SCK8_B/DE8/SD1DAT7/PDMDAT2	GTIOC12B	AN019	—
T8	T8	R7	R7	—	P014	—	IRQ27	—	—	AN014/D A0/ IVCMP0_ 3	—
T9	T9	P8	P8	VREFL	—	—	—	—	—	—	—

Table 1.17 Pin list (8 of 8)

BGA289	BGA289 without MIPI	BGA224	BGA224 without MIPI	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/ USBHS/OSPI/SSIE/SDHI/MMC/ ESWM(GMII,RGMII,MII,RMII)/ PDMIF	GPT/AGT/ULPT/RTC	ADC16/ DAC12/ ACMPHS	MIPI/ GLCDC/ CEU
T10	T10	P9	P9	VREFL0	—	—	—	—	—	—	—
T11	T11	R11	R11	—	P004	—	IRQ9-DS	—	—	AN004/ IVCMP2_ 2	—
T12	T12	M9	M9	—	P007	—	IRQ28	—	—	AN007/ IVCMP3_ 3	—
T13	T13	N11	N11	—	P001	—	IRQ7-DS	—	—	AN001/ IVCMP3_ 0	—
T14	T14	—	—	—	P806	—	IRQ0	RXD8_A/SCL8_A/MISO8_A/ ET1_MDC	—	AN018	VIO_D14
T15	T15	—	—	—	P715	—	IRQ12	RXD4_C/SCL4_C/MISO4_C/ ET_TAS_STA2	GTIOC12A	—	—
T16	T16	P14	P14	—	P815	—	IRQ15	CTX0	GTIOC8A	—	—
T17	T17	P15	P15	VSS_USB	—	—	—	—	—	—	—
U1	—	R1	—	MIPI_DL0_N	—	—	—	—	—	—	—
U2	—	R2	—	MIPI_CL_N	—	—	—	—	—	—	—
U3	—	R3	—	MIPI_DL1_N	—	—	—	—	—	—	—
—	U1	—	R1	—	P204	—	IRQ26	SCK4_A/DE4/SDA1_B/SSLA0_A/ SD1WP	GTIW/GTIOC4B/AGTIO1	—	—
—	U2	—	R2	—	P202	—	IRQ3-DS	CTS_RTS4_A/SS4_A/DE4/ MOSIA_A/CRX0/SD1CMD	GTIOC5B/ULPTOB1	—	—
—	U3	—	R3	—	P314	—	IRQ28	RXD3_C/SCL3_C/MISO3_C/ SSLA2_A/SD1DAT1	—	—	—
U4	U4	—	N3	VSS_13	—	—	—	—	—	—	—
U5	U5	R5	R5	—	P808	—	IRQ15	RXD7_B/SCL7_B/MISO7_B/ OM_0_SCLK	GTIOC13B	—	—
U6	U6	R6	R6	—	P100	—	IRQ2	SCK9_A/DE9/MISOB_A/ OM_0_SIO0/GPTP1_MATCH	GTIOC8B/AGTIO0	—	—
U7	U7	—	—	—	P500	—	IRQ24	RXD8_B/SCL8_B/MISO8_B/ SD1DAT5/PDMDAT0	GTIOC11B	AN021	—
U8	U8	P7	P7	—	P015	—	IRQ13	—	—	AN015/DA1/ IVCMP0_ 2	—
U9	U9	R8	R8	VREFH	—	—	—	—	—	—	—
U10	U10	R9	R9	VREFH0	—	—	—	—	—	—	—
U11	U11	R10	R10	—	P008	—	IRQ12-DS	—	—	AN008/ IVREF0	—
U12	U12	P10	P10	—	P006	—	IRQ11-DS	—	—	AN006/ IVCMP2_ 3	—
U13	U13	R12	R12	—	P000	—	IRQ6-DS	—	—	AN000/ IVCMP2_ 0	—
U14	U14	P11	P11	—	P002	—	IRQ8-DS	—	—	AN002/ IVCMP2_ 1	—
U15	U15	R13	R13	—	P511	—	IRQ15	CTS_RTS8_A/SS8_A/DE8/SDA1_A/ CRX1/ET1_LINKSTA	GTIOC0B	—	—
U16	U16	R14	R14	—	P814	—	IRQ16	CRX0	GTIOC8B	—	—
U17	U17	R15	R15	VCC_USB	—	—	—	—	—	—	—

Note: Several pin names have the added suffix of _A, _B, and _C. The suffix can be ignored when assigning functionality.

Revision History

Revision 0.80— January 25, 2024

First draft release

Revision 0.81— February 29, 2024

Second draft release

Revision 0.82— April 1, 2024

Third draft release

Revision 0.83— April 19, 2024

Fourth draft release

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.