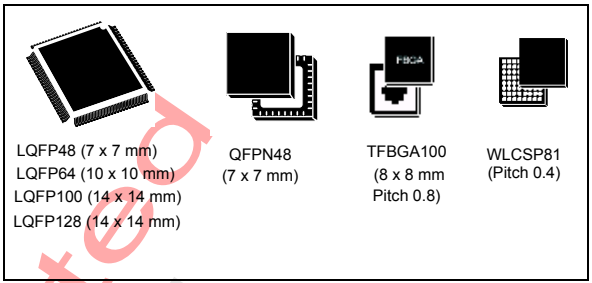
STM32G484xB STM32G484xC STM32G484xE

Arm® Cortex®-M4 32b MCU+FPU, up to 512KB Flash, 150 MHz, 128KB SRAM, Analog rich with 16b ADC, Math Co-Pro, 208 ps 12ch Hi-Res timer

Data brief

Features

- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait-state execution from Flash memory, frequency up to 150 MHz with188 DMIPS, MPU, DSP instructions
- Operating conditions:
  - VDD, VDDA voltage range: 1.71 V to 3.6 V
- Mathematical Co-Processor
  - CORDIC for Trigonometric functions acceleration
  - FMAC: Filter Mathematical Accelerator
- Memories
  - 512 Kbytes Flash, two banks read-while-write, proprietary code readout protection.
  - 96 Kbytes of SRAM, with HW parity check implemented on the first 32 Kbytes
  - Routine booster: 32 Kbytes of SRAM on instruction and data bus, with HW parity check (CCM SRAM)
  - External memory interface for static memories supporting SRAM, PSRAM, NOR and NAND memories
  - Quad-SPI memory interface
- Reset and supply management
  - Power-on/Power-down reset (POR/PDR/BOR)
  - Programmable voltage detector (PVD)
  - Low-power modes: Sleep, Stop, Standby and Shutdown
  - V_{BAT} supply for RTC and backup registers
- Clock management
  - 4 to 48 MHz crystal oscillator
  - 32 kHz oscillator with calibration
  - Internal 16 MHz RC with PLL option (± 1%)
  - Internal 32 kHz RC oscillator (± 5%)
- Up to 107 fast I/Os



  - All mappable on external interrupt vectors
  - Several I/Os with 5 V tolerant capability
- Interconnect matrix
- 16-channel DMA controller
- 5 x 12-bit ADCs 0.20 µs (5MSPS), up to 42 channels. Resolution up to 16-bit with hardware oversampling, 0 to 3.6 V conversion range
- 7 x 12-bit DAC channels
  - 3 x buffered external channels 1MSPS
  - 4 x unbuffered internal channels 15 MSPS.
- 7 x ultra-fast rail-to-rail analog comparators
- 6 x operational amplifiers that can be used in PGA mode, all terminals accessible
- 17 timers:
  - HRTIM (Hi-Resolution and complex waveform builder): 6 x16-bit counters, 208 ps resolution, 12 PWM
  - 2 x 32-bit timer and 2 x 16-bit timers with up to four IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - 3 x 16-bit 8-channel advanced motor control timers, with up to 8 x PWM channels, dead time generation and emergency stop
  - 1 x 16-bit timer with 2 x IC/OCs, one OCN/PWM, dead time generation and emergency stop
  - 2 x 16-bit timers with IC/OC/OCN/PWM, dead time generation and emergency stop
  - 2 x watchdog timers (independent, window)

  - 1 x SysTick timer: 24-bit downcounter
  - 2 x 16-bit basic timers
  - 1 x low-power timer
- Calendar RTC with Alarm, periodic wakeup from Stop/Standby
- Communication interfaces
  - 3 x CAN controller supporting Flexible data rate (CAN FD)
  - 4 x I^2C Fast mode plus (1 Mbit/s) with 20 mA current sink, SMBus/PMBus, wakeup from STOP
  - 5 x USART/UARTs (ISO 7816 interface, LIN, IrDA, modem control)
  - 1 x LPUART
  - 4 x SPIs, 4 to 16 programmable bit frames, 2 x with multiplexed half duplex I^2S interface
  - 1 x SAI (serial audio interface)
  - USB 2.0 full-speed interface with LPM and BCD support
  - IRTIM (Infrared interface)
  - USB Type-C™ /USB power delivery controller (UCPD)
- True random number generator (RNG)
- CRC calculation unit, 96-bit unique ID
- AES: 128/256-bit key encryption hardware accelerator (in STM32G441xx devices only)
- Development support: serial wire debug (SWD), JTAG, Embedded Trace Macrocell™

Table 1. Device summary

Reference	Part number
STM32G484xB	STM32G484CB, STM32G484RB, STM32G484VB, STM32G484WB
STM32G484xC	STM32G484CC, STM32G484RC, STM32G484VC, STM32G484WC
STM32G484xE	STM32G484CE, STM32G484RE, STM32G484VE, STM32G484WE

Contents

List of tables

List of figures

1 Introduction

This data brief provides the ordering information and mechanical device characteristics of the STM32G484xx microcontrollers.

This document should be read in conjunction with the reference manual (RM0440). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the Arm® Cortex®-M4 core, please refer to the Cortex®-M4 Technical Reference Manual, available from the www.arm.com website.

2 Description

The STM32G484xx devices are based on the high-performance Arm® Cortex®-M4 32-bit RISC core. They operate at a frequency of up to 150 MHz.

The Cortex-M4 core features a single-precision floating-point unit (FPU), which supports all the Arm single-precision data-processing instructions and all the data types. It also implements a full set of DSP (digital signal processing) instructions and a memory protection unit (MPU) which enhances the application's security.

These devices embed high-speed memories (512 Kbytes of Flash memory and 128 Kbytes of SRAM), a flexible external memory controller (FSMC) for static memories (for devices with packages of 100 pins and more), a Quad SPI Flash memories interface, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The devices embed as well several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, proprietary code readout protection.

The devices embed peripherals allowing mathematical/arithmetic functions acceleration (CORDIC co-processor for trigonometric functions and FMAC unit for Filter Functions).

They offer five fast 12-bit ADC (5 Msps), seven comparators, six operational amplifiers, seven DAC channels (3 external and 4 internal), an internal voltage reference buffer, a low-power RTC, general-purpose 32-bit timer, three 16-bit PWM timers dedicated to motor control, seven general-purpose 16-bit timers, and one 16-bit low-power timer, and high resolution timer with 208 ps resolution.

They also feature standard and advanced communication interfaces such as:

- Four I2Cs
- Four SPIs multiplexed with two half duplex I2Ss
- Three USARTs, two UART and one low-power UART.
- Three FDCANs
- One SAI (Serial Audio Interfaces)
- USB device
- USB PD

The devices embed an AES.

The devices operate in the -40 to +85 °C (+105 °C junction), -40 to +105 °C (+125 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Some independent power supplies are supported like an analog independent supply input for ADC, DAC, OPAMPs and comparators. A VBAT input allows to backup the RTC and backup the registers.

The STM32G484xx family offers 7 packages from 48-pin to 128-pin.

Table 2. STM32G484xx features and peripheral counts

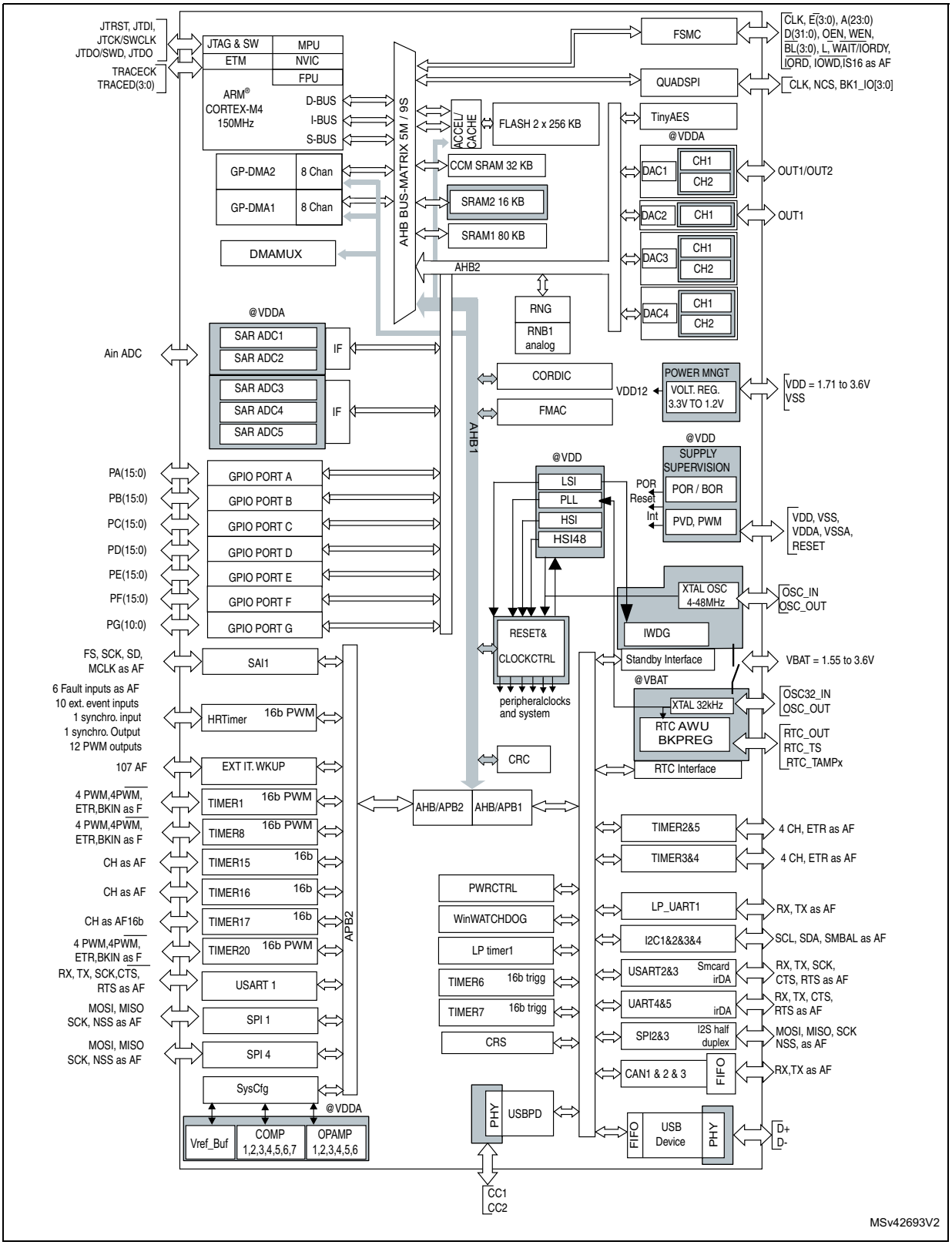
Peripheral		STM32G484Cx			STM32G484Rx			STM32G484Vx			STM32G484Wx		
Flash memory		128 KB	256 KB	512 KB	128 KB	256 KB	512 KB	128 KB	256 KB	512 KB	128 KB	256 KB	512 KB
SRAM		128 (80 + 16+ 32) KB											
External memory controller for static memories (FSMC)		No						Yes(1)			Yes		
QUADSPI		1											
Timers	Advanced motor control	3 (16-bit)											
	HRTIM	1											
	General purpose	5 (16-bit) 2 (32-bit)											
	Basic	2 (16-bit)											
	Low power	1 (16-bit)											
	SysTick timer	1											
	Watchdog timers (independent, window)	2											
	Total number of PWMs(2)	TBD			TBD			TBD			TBD		
Comm. interfaces	SPI(I2S)(3)	4 (2)											
	I^2C	4											
	USART	3											
	UART	0			2								
	LPUART	1											
	FDCANs	3											
	USB device	Yes											
	UCPD	Yes											
	SAI	Yes											
RTC		Yes											
Tamper pins		2						3					
Random number generator		Yes											
AES		Yes											
CORDIC		Yes											
FMAC		Yes											
GPIOs		38 in LQFP48 42 in QFN48			52			86			107		
Wakeup pins		3			4			5			5		

Table 2. STM32G484xx features and peripheral counts (continued)

Peripheral	STM32G484Cx	STM32G484Rx	STM32G484Vx	STM32G484Wx
12-bit ADCs Number of channels	5			
	20 in LQFP48 21 in QFN48	26	42	42
12-bit DAC Number of channels	4 7 (3 external + 4 internal)			
Internal voltage reference buffer	Yes			
Analog comparator	7			
Operational amplifiers	6			
Max. CPU frequency	150 MHz			
Operating voltage	1.71 V to 3.6 V			
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 105 °C / -40 to 125 °C			
Packages	LQFP48/QFN48	LQFP64	LQFP100/TFBGA100	LQFP128

1. For the LQFP100 package, only FMC bank1 and NAND bank are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 chip select.
2. This corresponds to the total number of TIM1/8/20/2/3/4/5/15/16/17 PWMs, that could be used in parallel. It includes the number of complementary PWMs.
3. The SPI2/3 interfaces can work in an exclusive way in either the SPI mode or the I2S audio mode.

Figure 1. STM32G484xx block diagram



Note: AF: alternate function on I/O pins.

3 Functional overview

3.1 Arm® Cortex®-M4 core with FPU

The Arm® Cortex®-M4 with FPU processor is the latest generation of Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of the MCU implementation, with a reduced pin count and with low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm® Cortex®-M4 with FPU 32-bit RISC processor features an exceptional code-efficiency, delivering the expected high-performance from an Arm core in a memory size usually associated with 8-bit and 16-bit devices.

The processor supports a set of DSP instructions which allows an efficient signal processing and a complex algorithm execution. Its single precision FPU speeds up the software development by using metalanguage development tools to avoid saturation.

With its embedded Arm core, the STM32G484xx family is compatible with all Arm tools and software.

Figure 1 shows the general block diagram of the STM32G484xx devices.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator that is optimized for the STM32 industry-standard Arm® Cortex®-M4 processors. It balances the inherent performance advantage of the Arm® Cortex®-M4 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to the memory and to prevent one task to accidentally corrupt the memory or the resources used by any other active task. This memory area is organized into up to 8 protected areas, which can be divided in up into 8 subareas each. The protection area sizes range between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Embedded Flash memory

The STM32G484xx devices feature 512 kbytes of embedded Flash memory which is available for storing programs and data.

The Flash interface features:

- Single or dual bank operating modes
- Read-while-write (RWW) in dual bank mode

This feature allows to perform a read operation from one bank while an erase or program operation is performed to the other bank. The dual bank boot is also supported.

Flexible protections can be configured thanks to the option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels of protection are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection; the Flash memory cannot be read from or written to if either the debug features are connected or the boot in RAM or bootloader are selected
  - Level 2: chip readout protection; the debug features (Cortex-M4 JTAG and serial wire), the boot in RAM and the bootloader selection are disabled (JTAG fuse). This selection is irreversible.
- Write protection (WRP): the protected area is protected against erasing and programming.
- Proprietary code readout protection (PCROP): a part of the Flash memory can be protected against read and write from third parties. The protected area is execute-only and it can only be reached by the STM32 CPU as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited. An additional option bit (PCROP_RDP) allows to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

The Flash memory embeds the error correction code (ECC) feature supporting:

- Single error detection and correction
- Double error detection
- The address of the ECC fail can be read in the ECC register

3.5 Embedded SRAM

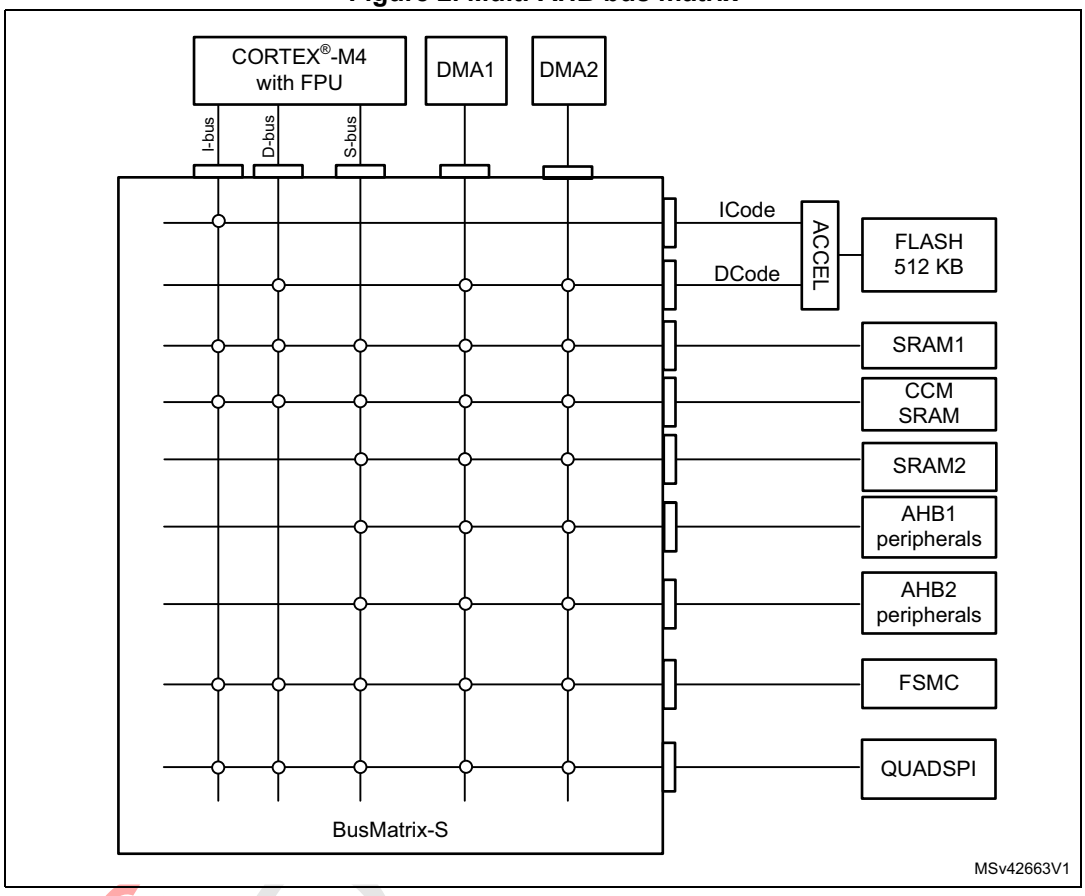
STM32G484xx devices feature 128 Kbyte of embedded SRAM. This SRAM is split into three blocks:

- 80 Kbyte mapped at address 0x2000 0000 (SRAM1). The CM4 can access the SRAM1 through the System Bus or through the I-Code/D-Code bus. The first 32 Kbyte of SRAM1 support hardware parity check.
- 16 Kbyte mapped at address 0x2001 4000 (SRAM2). The CM4 can access the SRAM2 through the System Bus or through the I-Code/D-Code bus. SRAM2 can be retained in standby modes.
- 32 Kbyte mapped at address 0x1000 0000 (CCM SRAM). It is accessed by the CPU through ICODE/DCODE bus for maximum performance.
  It is also aliased at 0x2001 8000 address to be accessed by all masters (CPU, DMA1, DMA2) through SBUS contiguously to SRAM1 and SRAM2. The CCM SRAM supports hardware parity check and can be write-protected with 1 Kbyte granularity.
- The memory can be accessed in read/write at max CPU clock speed with 0 wait states.

3.6 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs) and the slaves (Flash memory, RAM, FSMC, QUADSPI, AHB and APB peripherals). It also ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 2. Multi-AHB bus matrix



3.7 Boot modes

At startup, a BOOT0 pin and an nBOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The BOOT0 value may come from the PB8-BOOT0 pin or from an option bit depending on the value of a user option bit to free the GPIO pad if needed.

The boot loader is located in the system memory. It is used to reprogram the Flash memory by using USART, I2C, SPI, CAN and USB through the DFU (device firmware upgrade).

3.8 CORDIC co-processor (CORDIC)

The CORDIC co-processor provides hardware acceleration of certain mathematical functions, notably trigonometric, commonly used in motor control, metering, signal processing and many other applications.

It speeds up the calculation of these functions compared to a software implementation, allowing a lower operating frequency, or freeing up processor cycles in order to perform other tasks.

Cordic features

- 24-bit CORDIC rotation engine
- Circular and Hyperbolic modes
- Rotation and Vectoring modes
- Functions: Sine, Cosine, Sinh, Cosh, Atan, Atan2, Atanh, Modulus, Square root, Natural logarithm
- Programmable precision up to 20-bit
- Fast convergence: 4 bits per clock cycle
- Supports 16-bit and 32-bit fixed point input and output formats
- Low latency AHB slave interface
- Results can be read as soon as ready without polling or interrupt
- DMA read and write channels

3.9 Filter Mathematical ACcelerator(FMAC)

The filter math accelerator unit performs arithmetic operations on vectors. It comprises a multiplier/accumulator (MAC) unit, together with address generation logic, which allows it to index vector elements held in local memory.

The unit includes support for circular buffers on input and output, which allows digital filters to be implemented. Both finite and infinite impulse response filters can be realized.

The unit allows frequent or lengthy filtering operations to be offloaded from the CPU, freeing up the processor for other tasks. In many cases it can accelerate such calculations compared to a software implementation, resulting in a speed-up of time critical tasks.

FMAC features

- 16 x 16-bit multiplier
- 24+2-bit accumulator with addition and subtraction
- 16-bit input and output data
- 256 x 16-bit local memory
- Up to three areas can be defined in memory for data buffers (two input, one output), defined by programmable base address pointers and associated size registers
- Input and output sample buffers can be circular
- Buffer “watermark” feature reduces overhead in interrupt mode
- Filter functions: FIR, IIR (direct form 1)
- AHB slave interface
- DMA read and write data channels

3.10 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator with polynomial value and size.

Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a mean to verify the Flash memory integrity.

The CRC calculation unit helps to compute a signature of the software during runtime, which can be ulteriorly compared with a reference signature generated at link-time and which can be stored at a given memory location.

3.11 Power supply management

3.11.1 Power supply schemes

The STM32G484xx devices require a 1.71 V to 3.6 V V_{DD} operating voltage supply. Several independent supplies, can be provided for specific peripherals:

- V_{DD} = 1.71 V to 3.6 V
  V_{DD} is the external power supply for the I/Os, the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through the VDD pins.
- V_{DDA} = 1.62 V (ADC) / 1.8 V (DAC 1MSPS/OPAMP)/ TBD (DAC 15MSPS) / TBD (COMP) / 2.4 V (VREFBUF) to 3.6 V.
  V_{DDA} is the external analog power supply for A/D converters, D/A converters, voltage reference buffer, operational amplifiers and comparators. The V_{DDA} voltage level is

independent from the V_{DD} voltage and should preferably be connected to V_{DD} when these peripherals are not used.

- V_{BAT} = 1.55 V to 3.6 V

  V_{BAT} is the power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

- V_{REF-}, V_{REF+}

  V_{REF+} is the input reference voltage for ADCs and DACs. It is also the output of the internal voltage reference buffer when enabled.

  When V_{DDA} < 2 V V_{REF+} must be equal to V_{DDA}.

  When V_{DDA} ≥ 2 V V_{REF+} must be between 2 V and V_{DDA}.

  The internal voltage reference buffer supports three output voltages, which are configured with VRS bit in the VREFBUF_CSR register:

  – V_{REF+} = 2.048V
  – V_{REF+} = 2.5V
  – V_{REF+} = 2.95V

  V_{REF-} is double bonded with V_{SSA}.

3.11.2 Power supply supervisor

The device has an integrated ultra-low-power brown-out reset (BOR) active in all modes (except for Shutdown mode). The BOR ensures proper operation of the devices after power-on and during power down. The devices remain in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71 V at power on, and other higher thresholds can be selected through option bytes.The devices feature an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold. An interrupt can be generated when V_{DD} drops below the VPVD threshold and/or when V_{DD} is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the devices embed a peripheral voltage monitor which compares the independent supply voltages V_{DDA}, with a fixed threshold in order to ensure that the peripheral is in its functional supply range.

3.11.3 Voltage regulator

Two embedded linear voltage regulators, main regulator (MR) and low-power regulator (LPR), supply most of digital circuitry in the device. The MR is used in Run and Sleep modes. The LPR is used in Low-power run, Low-power sleep and Stop modes. In Standby and Shutdown modes, both regulators are powered down and their outputs set in high-impedance state, such as to bring their current consumption close to zero.

3.11.4 Low-power modes

By default, the microcontroller is in Run mode after system or power Reset. It is up to the user to select one of the low-power modes described below:

- **Sleep mode**: In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Low-power run mode:** This mode is achieved with VCORE supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or from Flash, and the CPU frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16.
- **Low-power sleep mode:** This mode is entered from the low-power run mode. Only the CPU clock is stopped. When wakeup is triggered by an event or an interrupt, the system reverts to the Low power run mode.
- **Stop mode:** In Stop mode, the device achieves the lowest power consumption while retaining the SRAM and register contents. All clocks in the VCORE domain are stopped. The PLL, as well as the HSI16 RC oscillator and the HSE crystal oscillator are disabled. The LSE or LSI keep running. The RTC can remain active (Stop mode with RTC, Stop mode without RTC). Some peripherals with wakeup capability can enable the HSI16 RC during Stop mode, so as to get clock for processing the wakeup event.
- **Standby mode:** The Standby mode is used to achieve the lowest power consumption with brown-out reset, BOR. The internal regulator is switched off to power down the VCORE domain. The PLL, as well as the HSI16 RC oscillator and the HSE crystal oscillator are also powered down. The RTC can remain active (Standby mode with RTC, Standby mode without RTC). The BOR always remains active in Standby mode. For each I/O, the software can determine whether a pull-up, a pull-down or no resistor shall be applied to that I/O during Standby mode. Upon entering Standby mode, SRAM and register contents are lost except for registers in the RTC domain and standby circuitry. The device exits Standby mode upon external reset event (NRST pin), IWDG reset event, wakeup event (WKUP pin, configurable rising or falling edge) or RTC event (alarm, periodic wakeup, timestamp, tamper), or when a failure is detected on LSE (CSS on LSE).
- **Shutdown mode:** The Shutdown mode allows to achieve the lowest power consumption. The internal regulator is switched off to power down the VCORE domain. The PLL, as well as the HSI16 and LSI RC-oscillators and HSE crystal oscillator are also powered down. The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC). The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode. Therefore, switching to RTC domain is not supported. SRAM and register contents are lost except for registers in the RTC domain. The device exits Shutdown mode upon external reset event (NRST pin), IWDG reset event, wakeup event (WKUP pin, configurable rising or falling edge) or RTC event (alarm, periodic wakeup, timestamp, tamper).

3.11.5 Reset mode

In order to improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O schmitt trigger is disabled). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.11.6 VBAT operation

The VBAT pin allows to power the device VBAT domain from an external battery, an external supercapacitor, or from V_{DD} when there is no external battery and when an external supercapacitor is present. The VBAT pin supplies the RTC with LSE and the backup registers. Three anti-tamper detection pins are available in VBAT mode.

The VBAT operation is automatically activated when V_{DD} is not present. An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from VBAT, neither external interrupts nor RTC alarm/events exit the microcontroller from the VBAT operation.

3.12 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep and Stop modes.

Table 3. STM32G484xx peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
TIMx	TIMx	Timers synchronization or chaining	Y	Y	Y	Y	-
	ADCx DACx	Conversion triggers	Y	Y	Y	Y	-
	DMA	Memory to memory transfer trigger	Y	Y	Y	Y	-
	COMPx	Comparator output blanking	Y	Y	Y	Y	-
TIM16/TIM17	IRTIM	Infrared interface output generation	Y	Y	Y	Y	-
COMPx	TIM1, 8, 20 TIM2, 3, 4, 5	Timer input channel, trigger, break from analog signals comparison	Y	Y	Y	Y	-
	LPTIMER1	Low-power timer triggered by analog signals comparison	Y	Y	Y	Y	Y
	HRTIM	COMPx Output is an input event or a fault input for HRTIM	Y	Y	Y	Y	-
ADCx	TIM1, 8, 20	Timer triggered by analog watchdog	Y	Y	Y	Y	-
	HRTIM	HRTIM external event source can be ADCx analog watchdog	Y	Y	Y	Y	-

Table 3. STM32G484xx peripherals interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
RTC	TIM16	Timer input channel from RTC events	Y	Y	Y	Y	-
	LPTIMER1	Low-power timer triggered by RTC alarms or tampers	Y	Y	Y	Y	Y
All clocks sources (internal and external)	TIM5, TIM15, 16, 17	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-
USB	TIM2	Timer triggered by USB SOF	Y	Y	-	-	-
CSS RAM (parity error) Flash memory (ECC error) COMPx PVD	TIM1,8, 20 TIM15,16,17 HRTIM	Timer break HRTIM SYSFLT	Y	Y	Y	Y	-
CPU (hard fault)	TIM1,8,20 TIM15/16/17 HRTIM	Timer break HRTIM SYSFLT	Y	Y	Y	Y	-
GPIO	TIMx	External trigger	Y	Y	Y	Y	-
	LPTIMER1	External trigger	Y	Y	Y	Y	Y
	HRTIM	External fault/event/Synchro inputs for HRTIM	Y	Y	Y	Y	-
	ADCx DACx	Conversion external trigger	Y	Y	Y	Y	-
HRTIM	DACx/ADCx	Conversion trigger	Y	Y	Y	Y	-
	GPIO	Synchro output for HRTIM	Y	Y	Y	Y	-

3.13 Clocks and startup

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** three different sources can deliver SYSCLK system clock:
  - 4 - 48 MHz high-speed oscillator with external crystal or ceramic resonator (HSE). It can supply clock to system PLL. The HSE can also be configured in bypass mode for an external clock.
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software. It can supply clock to system PLL.
  - System PLL with maximum output frequency of 150 MHz. It can be fed with HSE or HSI16 clocks.
- **Auxiliary clock source:** two ultra-low-power clock sources for the real-time clock (RTC):
  - 32.768 kHz low-speed oscillator with external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for using an external clock.
  - 32 kHz low-speed internal RC oscillator (LSI) with ±5% accuracy, also used to clock an independent watchdog.
- **Peripheral clock sources:** several peripherals (I2S, USART, I2C, LPTimer, ADC, SAI, RNG) have their own clock independent of the system clock.
- **Clock security system (CSS):** in the event of HSE clock failure, the system clock is automatically switched to HSI16 and, if enabled, a software interrupt is generated. LSE clock failure can also be detected and generate an interrupt.
- Clock-out capability:
  - **MCO:** microcontroller clock output: it outputs one of the internal clocks for external use by the application
  - **LSCO: low speed clock output:** it outputs LSI or LSE in all low-power modes.

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 150 MHz.

3.14 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB2 bus.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.15 Direct memory access controller (DMA)

The device embeds 2 DMAs. Refer to *Table 4: DMA implementation* for the features implementation.

Direct memory access (DMA) is used in order to provide a high-speed data transfer between peripherals and memory as well as from memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps the CPU resources free for other operations.

The two DMA controllers have 16 channels in total, each one dedicated to manage memory access requests from one or more peripherals. Each controller has an arbiter for handling the priority between DMA requests.

The DMA supports:

- 16 independently configurable channels (requests)
  - Each channel is connected to a dedicated hardware DMA request, a software trigger is also supported on each channel. This configuration is done by software.
- Priorities between requests from channels of one DMA are both software programmable (4 levels: very high, high, medium, low) or hardware programmable in case of equality (request 1 has priority over request 2, etc.)
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size.
- Support for circular buffer management
- 3 event flags (DMA half transfer, DMA transfer complete and DMA transfer error) logically ORed together in a single interrupt request for each channel
- Memory-to-memory transfer
- Peripheral-to-memory, memory-to-peripheral, and peripheral-to-peripheral transfers
- Access to Flash, SRAM, APB and AHB peripherals as source and destination
- Programmable number of data to be transferred: up to 65536.

Table 4. DMA implementation

DMA features	DMA1	DMA2
Number of regular channels	8	8

3.16 DMA request router (DMAMux)

When a peripheral indicates a request for DMA transfer by setting its DMA request line, the DMA request is pending until it is served and the corresponding DMA request line is reset. The DMA request router allows to route the DMA control lines between the peripherals and the DMA controllers of the product.

An embedded multi-channel DMA request generator can be considered as one of such peripherals. The routing function is ensured by a multi-channel DMA request line

multiplexer. Each channel selects a unique set of DMA control lines, unconditionally or synchronously with events on synchronization inputs.

For simplicity, the functional description is limited to DMA request lines. The other DMA control lines are not shown in figures or described in the text. The DMA request generator produces DMA requests following events on DMA request trigger inputs.

3.17 Interrupts and events

3.17.1 Nested vectored interrupt controller (NVIC)

The STM32G484xx devices embed a nested vectored interrupt controller which is able to manage 16 priority levels, and to handle up to 102 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.17.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 44 edge detector lines used to generate interrupt/event requests and to wake-up the system from the Stop mode. Each external line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently.

A pending register maintains the status of the interrupt requests. The internal lines are connected to peripherals with wakeup from Stop mode capability. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 107 GPIOs can be connected to the 16 external interrupt lines.

3.18 Analog-to-digital converter (ADC)

The device embeds a successive approximation analog-to-digital converters with the following features:

- 12-bit native resolution, with built-in calibration
- 5 Msps maximum conversion rate with full resolution
  - Down to 18.75 ns sampling time
  - Increased conversion rate for lower resolution (up to 8.88 Msps for 6-bit resolution)
- One external reference pin is available on all packages, allowing the input voltage range to be independent from the power supply
- Single-ended and differential mode inputs
- Low-power design
  - Capable of low-current operation at low conversion rate (consumption decreases linearly with speed)
  - Dual clock domain architecture: ADC speed independent from CPU frequency
- Highly versatile digital interface
  - Single-shot or continuous/discontinuous sequencer-based scan mode: 2 groups of analog signals conversions can be programmed to differentiate background and high-priority real-time conversions
  - Each ADC support multiple trigger inputs for synchronization with on-chip timers and external signals
  - Results stored into a data register or in RAM with DMA controller support
  - Data pre-processing: left/right alignment and per channel offset compensation
  - Built-in oversampling unit for enhanced SNR
  - Channel-wise programmable sampling time
  - Analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers
  - Hardware assistant to prepare the context of the injected channels to allow fast context switching
  - Flexible sample time control
  - Hardware gain and offset compensation

3.18.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature. The temperature sensor is internally connected to the ADCs input channels which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

3.18.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (VREFINT) provides a stable (bandgap) voltage output for the ADC and the comparators. The VREFINT is internally connected to the ADCx_IN18, x = 1,3,4,5 input channel. The precise voltage of VREFINT is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

3.18.3 V_{BAT} battery voltage monitoring

This embedded hardware enables the application to measure the V_{BAT} battery voltage using the internal ADC channel. As the V_{BAT} voltage may be higher than the VDDA, and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by 3. As a consequence, the converted digital value is one third of the V_{BAT} voltage.

3.18.4 Operational amplifier internal output (OPAMPxINT):

The OPAMPx (x = 1...6) output OPAMPxINT can be sampled using an ADCx (x = 1...5) internal input channel. In this case, the I/O on which the OPAMPx output is mapped can be used as GPIO.

3.19 Digital to analog converter (DAC)

Seven 12 bit DAC channels (3 external buffered and 4 internal unbuffered) can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- Up to two DAC output channels
- 8-bit or 12-bit output mode
- Buffer offset calibration (factory and user trimming)
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Saw tooth wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor
- Up to 1 Msps for external output and 15 Msps for internal output

The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.20 Voltage reference buffer (V_{REFBUF})

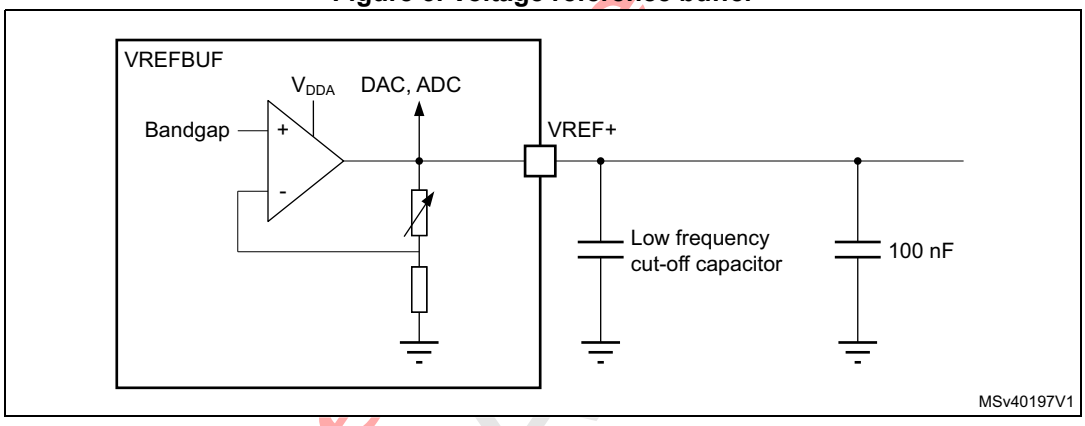
The STM32G484xx devices embed a voltage reference buffer which can be used as voltage reference for ADC, DACs and also as voltage reference for external components through the VREF+ pin.

The internal voltage reference buffer supports three voltages:

- 2.048 V
- 2.5 V
- 2.95 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

Figure 3. Voltage reference buffer



3.21 Comparators (COMP)

The STM32G484xx devices embed seven rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis.

The reference voltage can be one of the following:

- External I/O
- DAC output channels
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers.

3.22 Operational amplifier (OPAMP)

The STM32G484xx devices embed six operational amplifiers with external or internal follower routing and PGA capability.

The operational amplifier features:

- 15 MHz bandwidth
- Rail-to-rail input/output
- PGA with a non-inverting gain ranging of 2, 4, 8, 16, 32 or 64 or inverting gain ranging of -1, -3, -7, or -15

3.23 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.24 Advanced encryption standard hardware accelerator (AES)

The devices embed an AES hardware accelerator that can be used both to encipher and to decipher data using an AES algorithm.

The AES peripheral supports:

- Encryption/decryption using AES Rijndael block cipher algorithm
- NIST FIPS 197 compliant implementation of AES encryption/decryption algorithm
- 128-bit and 256-bit register for storing the encryption, decryption or derivation key (4x 32-bit registers)
- Electronic codebook (ECB), cipher block chaining (CBC), Counter mode (CTR), Galois Counter Mode (GCM), Galois Message Authentication Code mode (GMAC) and Cipher Message Authentication Code mode (CMAC) supported
- Key scheduler
- Key derivation for decryption
- 128-bit data block processing
- 128-bit, 256-bit key length
- 1x32-bit INPUT buffer and 1x32-bit OUTPUT buffer
- Register access supporting 32-bit data width only
- One 128-bit Register for the initialization vector when AES is configured in CBC mode or for the 32-bit counter initialization when CTR mode is selected, GCM mode or CMAC mode
- Automatic data flow control with support of direct memory access (DMA) using 2 channels, one for incoming data, and one for outcoming data
- Suspend a message if another message with a higher priority needs to be processed.

3.25 Timers and watchdogs

The STM32G484xx devices include One High Resolution time, two advanced motor control timers, up to nine general-purpose timers, two basic timers, one low-power timer, two watchdog timers and a SysTick timer. The table below compares the features of the advanced motor control, general purpose and basic timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
High resolution timer	HRTIM	16-bit	Up	/1 /2 /4 (x2 x4 x8 x16 x32, with DLL)	Yes	12	Yes
Advanced motor control	TIM1, TIM8, TIM20	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	4
General-purpose	TIM2, TIM5	32-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3, TIM4	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.25.1 High-resolution timer (HRTIM)

The high-resolution timer (HRTIM) allows generating digital signals with high-accuracy timings, such as PWM or phase-shifted pulses.

It consists of 7 timers, 1 master and 6 slaves, totaling 12 high-resolution outputs, which can be coupled by pairs for deadtime insertion. It also features 6 fault inputs for protection purposes and 10 inputs to handle external events such as current limitation, zero voltage or zero current switching.

HRTIM timer is made of a digital kernel clocked at 150 MHz followed by delay lines. Delay lines with closed loop control guarantee a 208 ps resolution whatever the voltage, temperature or chip-to-chip manufacturing process deviation. The high-resolution is available on the 12 outputs in all operating modes: variable duty cycle, variable frequency, and constant ON time.

The slave timers can be combined to control multiswitch complex converters or operate independently to manage multiple independent converters.

The waveforms are defined by a combination of user-defined timings and external events such as analog or digital feedbacks signals.

HRTIM timer includes options for blanking and filtering out spurious events or faults. It also offers specific modes and features to offload the CPU: DMA requests, burst mode controller, push-pull and resonant mode.

It supports many topologies including LLC, Full bridge phase shifted, buck or boost converters, either in voltage or current mode, as well as lighting application (fluorescent or LED). It can also be used as a general purpose timer, for instance to achieve high-resolution PWM-emulated DAC.

In debug mode, the HRTIM counters can be frozen and the PWM outputs enter safe state.

3.25.2 Advanced motor control timer (TIM1, TIM8, TIM20)

The advanced motor control timers can each be seen as a four-phase PWM multiplexed on 8 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers.

The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced motor control timer counter can be frozen and the PWM outputs disabled in order to turn off any power switches driven by these outputs.

Many features are shared with the general-purpose TIMx timers (described in *Section 3.25.3*) using the same architecture, so the advanced motor control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.25.3 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM15, TIM16, TIM17)

There are up to seven synchronizable general-purpose timers embedded in the STM32G484xx devices (see *Table 5* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, TIM3, TIM4 and TIM5

  They are full-featured general-purpose timers:

  – TIM2 and TIM5 have a 32-bit auto-reload up/downcounter and 32-bit prescaler

  – TIM3 and TIM4 have 16-bit auto-reload up/downcounter and 16-bit prescaler.

  These timers feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.

- TIM15, 16 and 17

  They are general-purpose timers with mid-range features:

  They have 16-bit auto-reload upcounters and 16-bit prescalers.

  – TIM15 has 2 channels and 1 complementary channel

  – TIM16 and TIM17 have 1 channel and 1 complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

3.25.4 Basic timers (TIM6 and TIM7)

The basic timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit timebases.

3.25.5 Low-power timer (LPTIM1)

The devices embed a low-power timer. This timer has an independent clock and are running in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the system from Stop mode.

LPTIM1 is active in Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
  - Internal clock sources: LSE, LSI, HSI16 or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by pulse counter application).
- Programmable digital glitch filter
- Encoder mode

3.25.6 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and an 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.25.7 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.25.8 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.26 Real-time clock (RTC) and backup registers

The RTC supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC is supplied through a switch that takes power either from the V_{DD} supply when present or from the VBAT pin.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32.

The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in VBAT mode, but is functional in all low-power modes except Shutdown mode.

All RTC events (Alarm, WakeUp Timer, Timestamp) can generate an interrupt and wakeup the device from the low-power modes.

3.27 Tamper and backup registers (TAMP)

- 32 32-bit backup registers, retained in all low-power modes and also in VBAT mode. They can be used to store sensitive data as their content is protected by an tamper detection circuit. They are not reset by a system or power reset, or when the device wakes up from Standby or Shutdown mode.
- Up to three tamper pins for external tamper detection events. The external tamper pins can be configured for edge detection, edge and level, level detection with filtering.
- Five internal tampers events.
- Any tamper detection can generate a RTC timestamp event.
- Any tamper detection erases the backup registers.
- Any tamper detection can generate an interrupt and wake-up the device from all low-power modes.

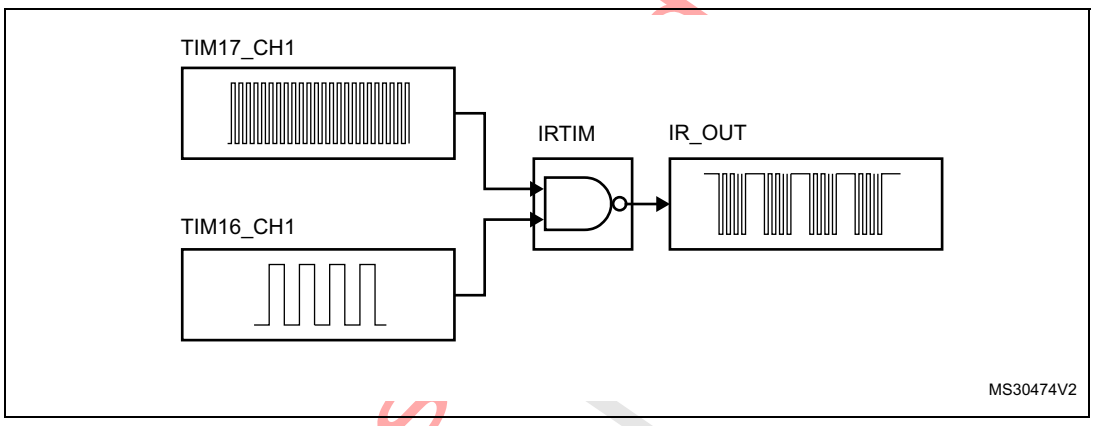
3.28 Infrared transmitter

The STM32G484xx devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below.

TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming the two timers output compare channels.

Figure 4. Infrared transmitter



3.29 Inter-integrated circuit interface (I^2C)

The device embeds four I2C. Refer to *Table 6: I2C implementation* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming.
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 6. I2C implementation

I2C features(1)	I2C1	I2C2	I2C3	I2C4
Standard-mode (up to 100 kbit/s)	X	X	X	X
Fast-mode (up to 400 kbit/s)	X	X	X	X
Fast-mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X	X	X
Programmable analog and digital noise filters	X	X	X	X
SMBus/PMBus hardware support	X	X	X	X
Independent clock	X	X	X	X
Wakeup from Stop mode on address match	X	X	X	X

1. X: supported

3.30 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32G484xx devices have three embedded universal synchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4, USART5).

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN master/slave capability. They provide hardware management of the CTS and RTS signals, and RS485 driver enable.

The USART1, USART2 and USART3 also provide a Smartcard mode (ISO 7816 compliant) and an SPI-like communication capability.

The USART comes with a Transmit FIFO (TXFIFO) and a Receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default.

All USART have a clock domain independent from the CPU clock, allowing the U(S)ARTx (x=1,2,3,4,5) to wake up the MCU from Stop mode. The wakeup from Stop mode can be done on:

- Start bit detection
- Any received data frame
- A specific programmed data frame
- Some specific TXFIFO/RXFIFO status interrupts when FIFO mode is enabled

All USART interfaces can be served by the DMA controller.

Table 7. USART/UART/LPUART features

USART modes/features(1)	USART1	USART2	USART3	UART4	UART5	LPUART1
Hardware flow control for modem	X	X	X	X	X	X
Continuous communication using DMA	X	X	X	X	X	X
Multiprocessor communication	X	X	X	X	X	X
Synchronous mode	X	X	X	-	-	-
Smartcard mode	X	X	X	-	-	-
Single-wire half-duplex communication	X	X	X	X	X	X
IrDA SIR ENDEC block	X	X	X	X	X	-
LIN mode	X	X	X	X	X	-
Dual clock domain	X	X	X	X	X	X
Wakeup from Stop mode	X	X	X	X	X	X
Receiver timeout interrupt	X	X	X	X	X	-
Modbus communication	X	X	X	X	X	-
Auto baud rate detection	X (4 modes)					-
Driver Enable	X	X	X	X	X	X
LPUART/USART data length	7, 8 and 9 bits					

Table 7. USART/UART/LPUART features (continued)

USART modes/features(1)	USART1	USART2	USART3	UART4	UART5	LPUART1
Tx/Rx FIFO	X					
Tx/Rx FIFO size	8					

1. X = supported.

3.31 Low-power universal asynchronous receiver transmitter (LPUART)

The STM32G484xx devices embed one Low-Power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half-duplex single-wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART comes with a Transmit FIFO (TXFIFO) and a Receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default. It has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode. The wake up from Stop mode can be done on:

- Start bit detection
- Any received data frame
- A specific programmed data frame
- Some specific TXFIFO/RXFIFO status interrupts when FIFO mode is enabled

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

The LPUART interface can be served by the DMA controller.

3.32 Serial peripheral interface (SPI)

Three SPI interfaces allow communication up to TBD Mbits/s in master and up to TBD Mbits/s in slave, half-duplex, full-duplex and simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits. The SPI interfaces support NSS pulse mode, TI mode and hardware CRC calculation.

Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) supporting four different audio standards can operate as master or slave at half-duplex communication modes. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by 8-bit programmable linear prescaler. When operating in master mode it can output a clock for an external audio component at 256 times the sampling frequency.

All SPI interfaces can be served by the DMA controller.

3.33 Serial audio interfaces (SAI)

The device embeds 1 SAI. The SAI bus interface handles communications between the microcontroller and the serial audio protocol.

SAI peripheral supports:

- Two independent audio sub-blocks which can be transmitters or receivers with their respective FIFO.
- 8-word integrated FIFOs for each audio sub-block.
- Synchronous or asynchronous mode between the audio sub-blocks.
- Master or slave configuration independent for both audio sub-blocks.
- Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode.
- Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit.
- Peripheral with large configurability and flexibility allowing to target as example the following audio protocol: I2S, LSB or MSB-justified, PCM/DSP, TDM, AC’97 and SPDIF out.
- Up to 16 slots available with configurable size and with the possibility to select which ones are active in the audio frame.
- Number of bits by frame may be configurable.
- Frame synchronization active level configurable (offset, bit length, level).
- First active bit position in the slot is configurable.
- LSB first or MSB first for data transfer.
- Mute mode.
- Stereo/Mono audio frame capability.
- Communication clock strobing edge configurable (SCK).
- Error flags with associated interrupts if enabled respectively. – Overrun and underrun detection. – Anticipated frame synchronization signal detection in slave mode. – Late frame synchronization signal detection in slave mode. – Codec not ready for the AC’97 mode in reception.
- Interruption sources when enabled: – Errors. – FIFO requests.
- DMA interface with 2 dedicated channels to handle access to the dedicated integrated FIFO of each SAI audio sub-block.

Table 8. SAI implementation for the features implementation

SAI features	Support[1]
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC’97	X
Mute mode	X
Stereo/Mono audio frame capability	X
16 slots	X
Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit	X
FIFO size	X (8 word)
SPDIF	X

1. X: supported.

3.34 Controller area network (FDCAN1, FDCAN2, FDCAN3)

The controller area network (CAN) subsystem consists of three CAN modules and a shared message RAM memory.

The three CAN modules (FDCAN1, FDCAN2 and FDCAN3) compliant with ISO 11898-1 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

A 3 Kbytes message RAM memory implements filters, receive FIFOs, receive buffers, transmit event FIFOs, transmit buffers. This message RAM is shared between the three FDCAN modules.

3.35 Universal serial bus (USB)

The STM32G484xx devices embed a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 KB and suspend/resume support. It requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use a HSE crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) which allows crystal less operation.

3.36 USB Type-C™ / USB Power Delivery controller (UCPD)

The device embeds one controller (UCPD) compliant with USB Type-C Rev. 1.2 and USB Power Delivery Rev. 3.0 specifications.

The controller uses specific I/Os supporting the USB Type-C and USB Power Delivery requirements, featuring:

- USB Type-C pull-up (Rp, all values) and pull-down (Rd) resistors
- “Dead battery” support
- USB Power Delivery message transmission and reception
- FRS (fast role swap) support

The digital controller handles notably:

- USB Type-C level detection with de-bounce, generating interrupts
- FRS detection, generating an interrupt
- Byte-level interface for USB Power Delivery payload, generating interrupts (DMA compatible)
- USB Power Delivery timing dividers (including a clock pre-scaler)
- CRC generation/checking
- 4b5b encode/decode
- Ordered sets (with a programmable ordered set mask at receive)
- Frequency recovery in receiver during preamble

The interface offers low-power operation compatible with Stop mode, maintaining the capacity to detect incoming USB Power Delivery messages and FRS signaling.

3.37 Clock recovery system (CRS)

The devices embed a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.38 Flexible static memory controller (FSMC)

The Flexible static memory controller (FSMC) includes two memory controllers:

- The NOR/PSRAM memory controller
- The NAND/memory controller

This memory controller is also named Flexible memory controller (FMC).

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR Flash memory/OneNAND Flash memory
  - PSRAM (4 memory banks)
  - NAND Flash memory with ECC hardware to check up to 8 Kbyte of data
  - Ferroelectric RAM (FRAM)
- 8-,16- bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- The Maximum FMC_CLK frequency for synchronous accesses is HCLK/2.

LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

3.39 Quad SPI memory interface (QUADSPI)

The Quad SPI is a specialized communication interface targeting single, dual or quad SPI flash memories. It can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the QUADSPI registers
- Status polling mode: the external flash status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external Flash is memory mapped and is seen by the system as if it were an internal memory.

Both throughput and capacity can be increased two-fold using dual-flash mode, where two quad SPI flash memories are accessed simultaneously.

The Quad SPI interface supports:

- Indirect mode: all the operations are performed using the QUADSPI registers
- Status polling mode: the external flash status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external Flash is memory mapped and is seen by the system as if it were an internal memory
- Three functional modes: indirect, status-polling, and memory-mapped
- SDR and DDR support
- Fully programmable opcode for both indirect and memory mapped mode
- Fully programmable frame format for both indirect and memory mapped mode
  - Each of the 5 following phases can be configured independently (enable, length, single/dual/quad communication)
  - Instruction phase
  - Address phase
  - Alternate bytes phase
  - Dummy cycles phase
  - Data phase
- Integrated FIFO for reception and transmission
- 8, 16, and 32-bit data accesses are allowed
- DMA channel for indirect mode operations
- Programmable masking for external flash flag management
- Timeout management
- Interrupt generation on FIFO threshold, timeout, status match, operation complete, and access error

3.40 Development support

3.40.1 Serial wire JTAG debug port (SWJ-DP)

The Arm SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with

SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.40.2 Embedded Trace Macrocell™

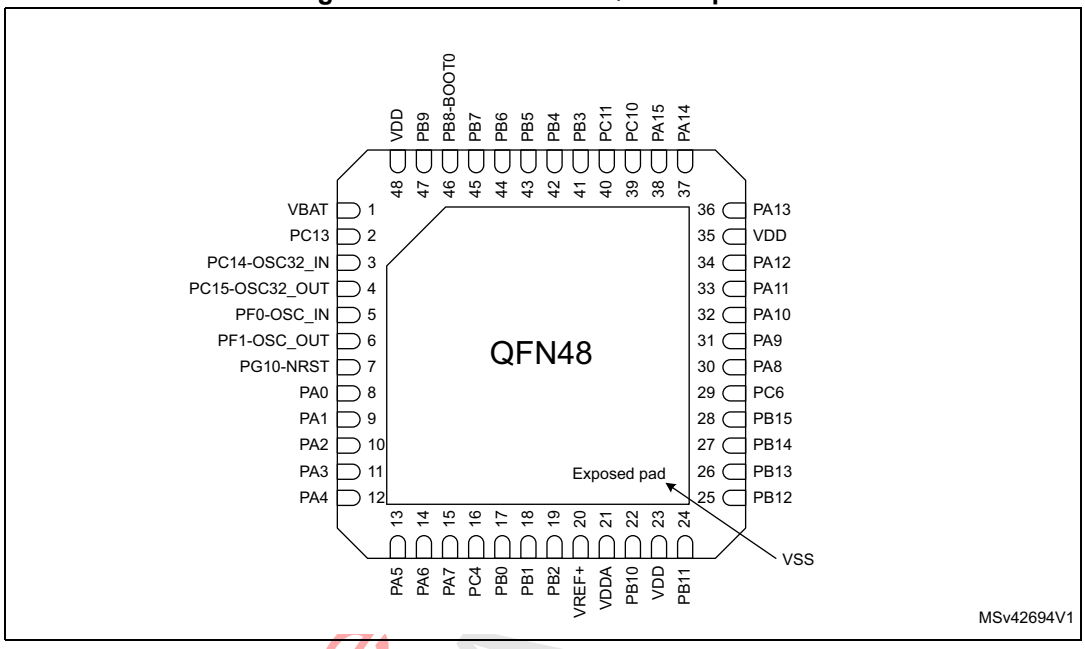
The Arm Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32G484xx devices through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

4 Pinouts and pin description

4.1 QFPN48 pinout description

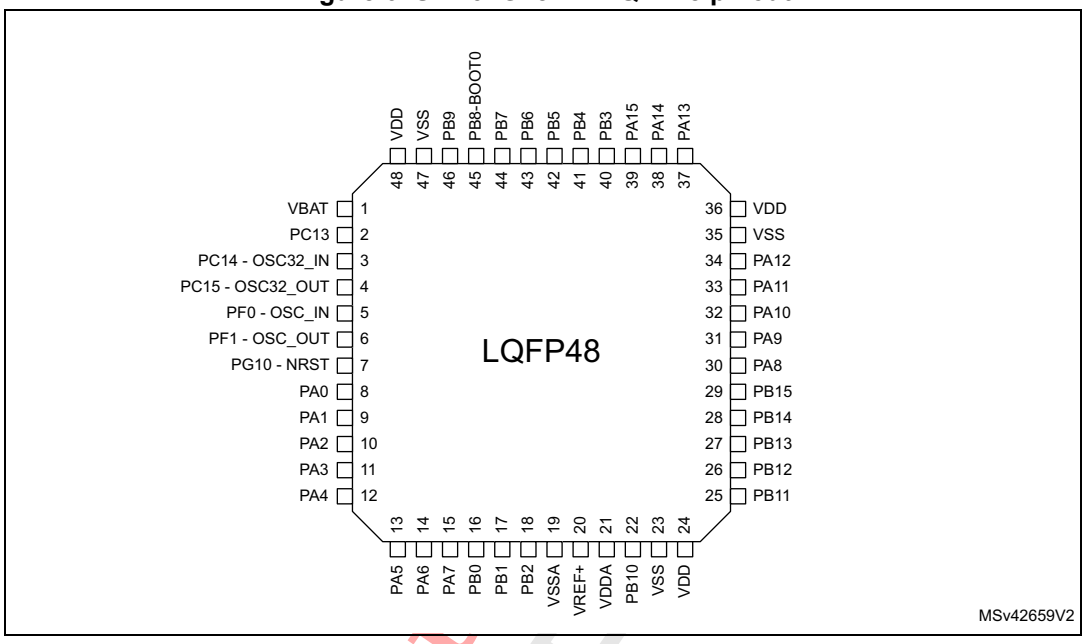
Figure 5. STM32G484xx QFPN48 pinout



1. The above figure shows the package top view
2. VSS pads are connected to the exposed pad.

4.2 LQFP48 pinout description

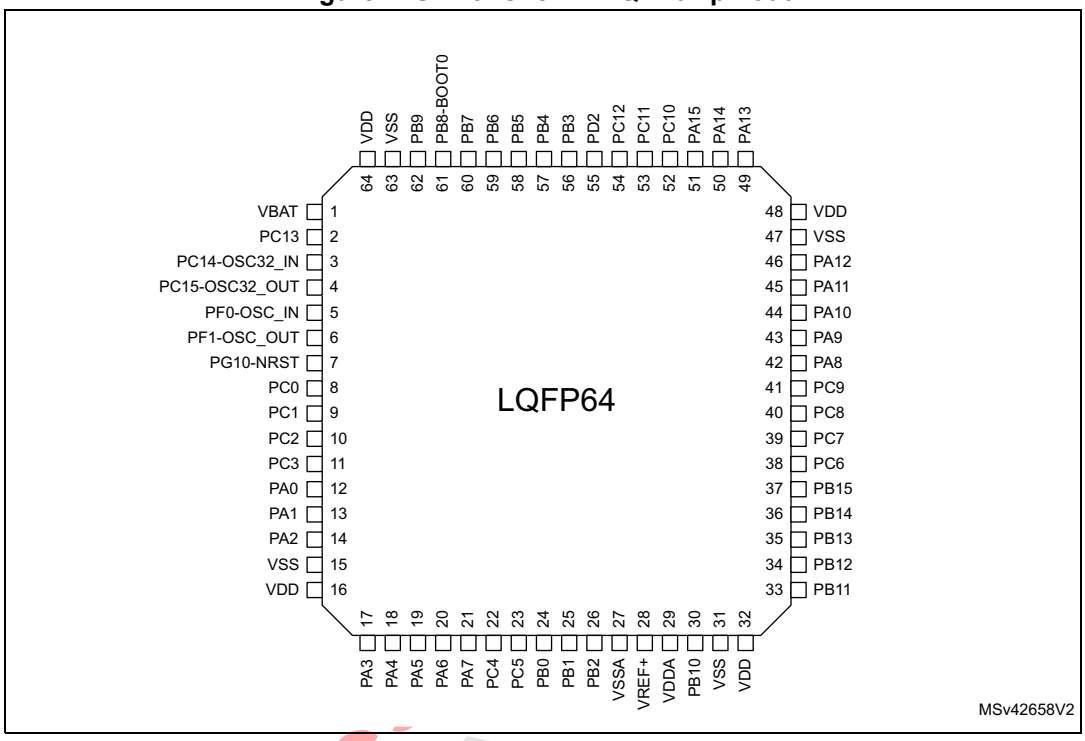
Figure 6. STM32G484xx LQFP48 pinout



1. The above figure shows the package top view

4.3 LQFP64 pinout description

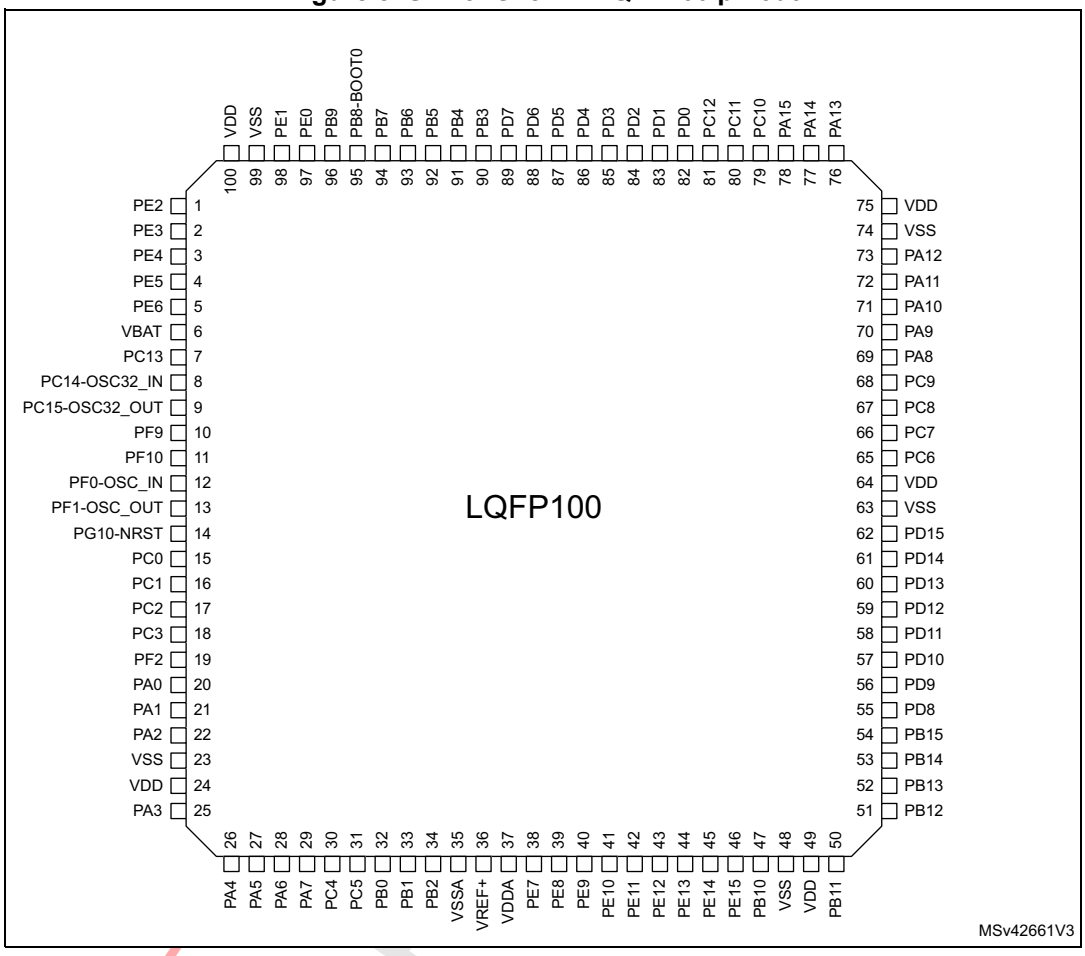
Figure 7. STM32G484xx LQFP64 pinout



1. The above figure shows the package top view.

4.4 LQFP100 pinout description

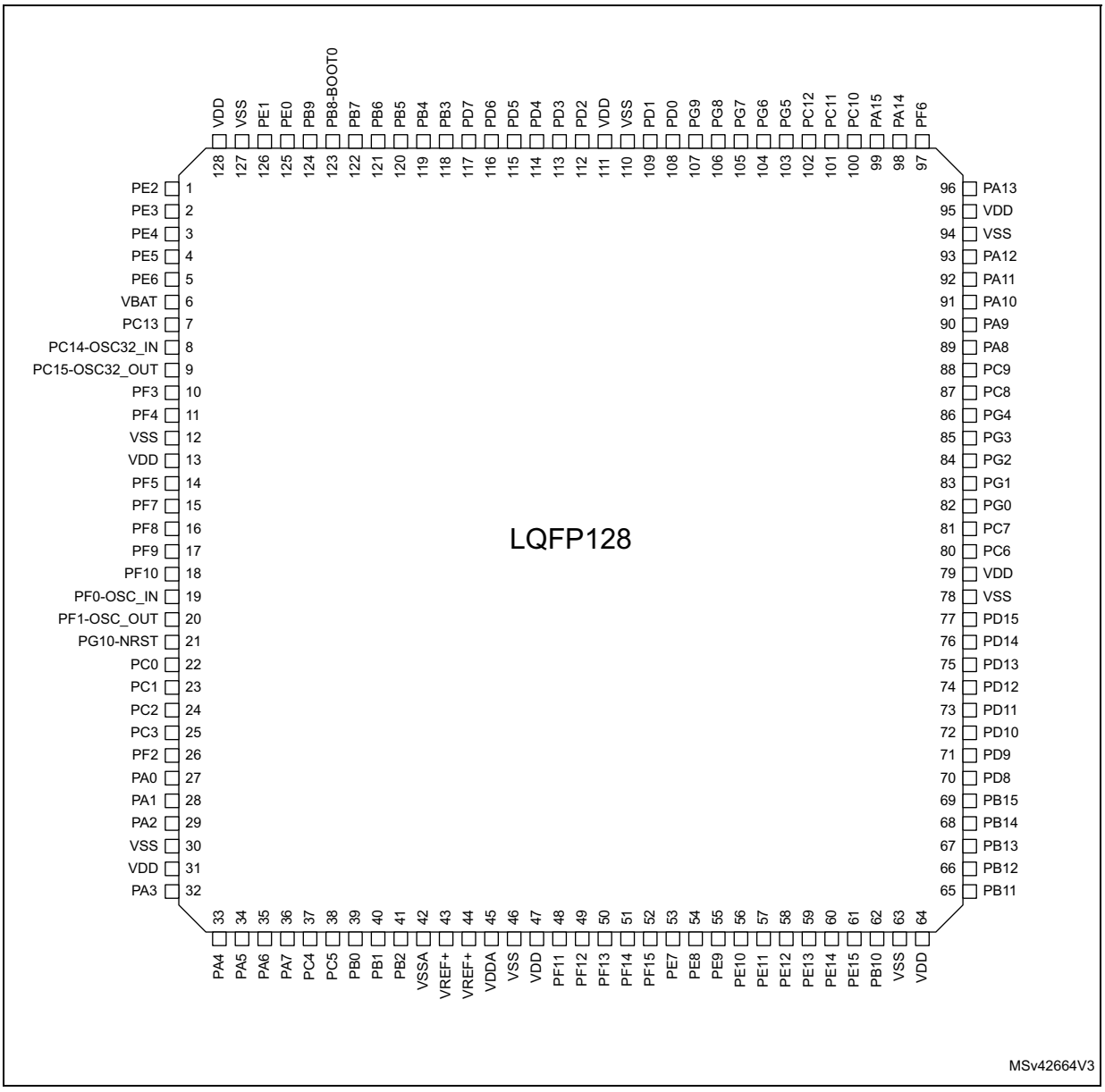
Figure 8. STM32G484xx LQFP100 pinout



1. The above figure shows the package top view.

4.5 LQFP128 pinout description

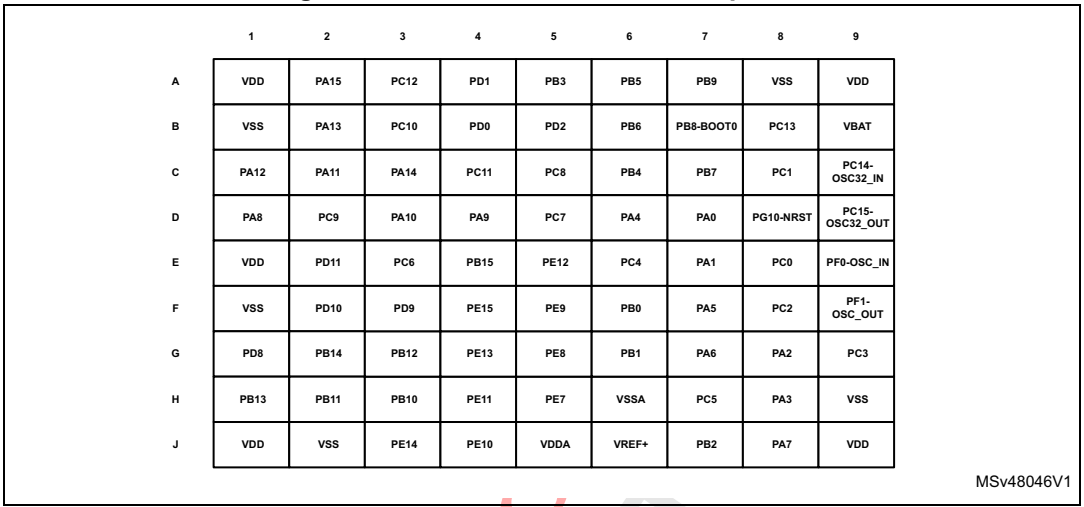
Figure 9. STM32G484xx LQFP128 pinout



1. The above figure shows the package top view.

4.6 WLCSP81 pinout description

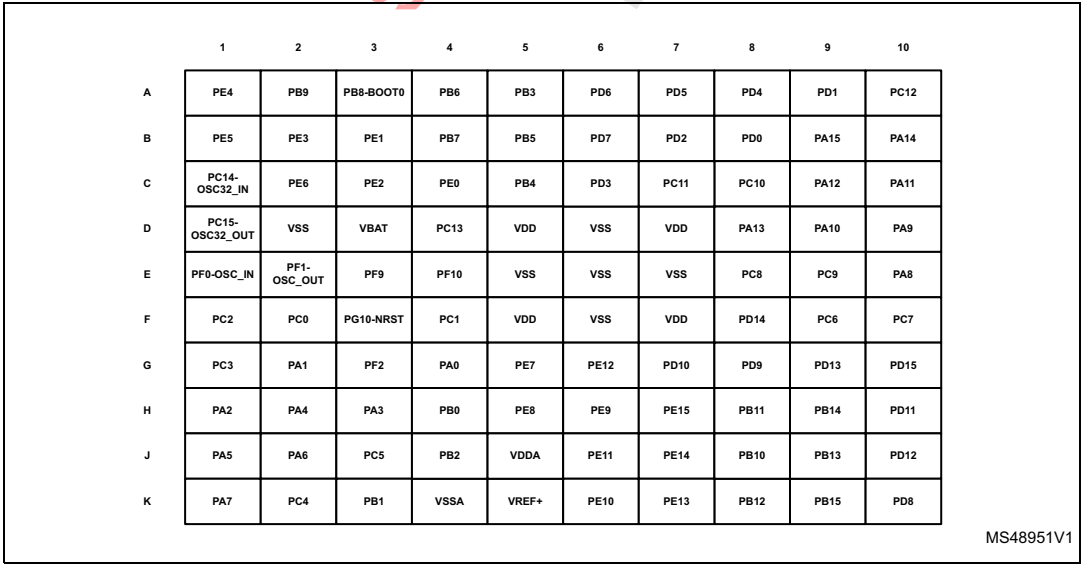
Figure 10. STM32G484xx WLCSP81 pinout



1. The above figure shows the package top view.

4.7 TFBGA100 pinout description

Figure 11. STM32G484xx TFBGA100 pinout



1. The above figure shows the package top view.

4.8 Pin definition

Table 9. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TT	3.6 V tolerant I/O
	B	Dedicated BOOT0 pin
	NRST	Bidirectional reset pin with embedded weak pull-up resistor
	Option for TT or FT I/Os	
	_f(1)	I/O, Fm+ capable
	_a (2)	I/O, with Analog switch function supplied by V_{DDA}
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers
	Additional functions	Functions directly selected/enabled through peripheral registers

1. The related I/O structures in *Table 10* are: FT_f, FT_fa.
2. The related I/O structures in *Table 10* are: FT_a, FT_fa, TT_a.

Table 10. STM32G484xx pin definition

Pin Number							Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LPQF100	LPQF128						
-	-	-	-	C3	1	1	PE2	I/O	FT	-	TRACECK, TIM3_CH1, SAI_CK1, SPI4_SCK, TIM20_CH1, FMC_A23, SAI_MCLK_A, EVENTOUT	-
-	-	-	-	B2	2	2	PE3	I/O	FT	-	TRACED0, TIM3_CH2, SPI4_NSS, TIM20_CH2, FMC_A19, SAI_SD_B, EVENTOUT	-
-	-	-	-	A1	3	3	PE4	I/O	FT	-	TRACED1, TIM3_CH3, SAI_D2, SPI4_NSS, TIM20_CH1N, FMC_A20, SAI_FS_A, EVENTOUT	-
-	-	-	-	B1	4	4	PE5	I/O	FT	-	TRACED2, TIM3_CH4, SAI_CK2, SPI4_MISO, TIM20_CH2N, FMC_A21, SAI_SCK_A, EVENTOUT	-
-	-	-	-	C2	5	5	PE6	I/O	FT	-	TRACED3, SAI_D1, SPI4_MOSI, TIM20_CH3N, FMC_A22, SAI_SD_A, EVENTOUT	WKUP3, RTC_TAMP3
B9	1	1	1	D3	6	6	VBAT	S	-	-	-	-
B8	2	2	2	D4	7	7	PC13	I/O	FT	-	TIM1_BKIN, TIM1_CH1N, TIM8_CH4N, EVENTOUT	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT1
C9	3	3	3	C1	8	8	PC14-OSC32_IN	I/O	FT	-	EVENTOUT	OSC32_IN
D9	4	4	4	D1	9	9	PC15-OSC32_OUT	I/O	FT	-	EVENTOUT	OSC32_OUT
-	-	-	-	-	-	10	PF3	I/O	FT_f	-	TIM20_CH4, I2C3_SCL, FMC_A3, EVENTOUT	-
-	-	-	-	-	-	11	PF4	I/O	FT_f	-	COMP1_OUT, TIM20_CH1N, I2C3_SDA, FMC_A4, EVENTOUT	-
F1	-	-	-	-	-	12	VSS	S	-	-	-	-
A9	-	-	-	-	-	13	VDD	S	-	-	-	-

Table 10. STM32G484xx pin definition (continued)

Pin Number							Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LPQF100	LPQF128						
-	-	-	-	-	-	14	PF5	I/O	FT	-	TIM20_CH2N, FMC_A5, EVENTOUT	-
-	-	-	-	-	-	15	PF7	I/O	FT	-	TIM20_BKIN, TIM5_CH2, QUADSPI_BK1_IO2, FMC_A1, SAI_MCLK_B, EVENTOUT	-
-	-	-	-	-	-	16	PF8	I/O	FT	-	TIM20_BKIN2, TIM5_CH3, QUADSPI_BK1_IO0, FMC_A24, SAI_SCK_B, EVENTOUT	-
-	-	-	-	E3	10	17	PF9	I/O	FT	-	TIM20_BKIN, TIM15_CH1, SPI2_SCK, TIM5_CH4, QUADSPI_BK1_IO1, FMC_A25, SAI_FS_B, EVENTOUT	-
-	-	-	-	E4	11	18	PF10	I/O	FT	-	TIM20_BKIN2, TIM15_CH2, SPI2_SCK, QUADSPI_CLK, FMC_A0, SAI_D3, EVENTOUT	-
E9	5	5	5	E1	12	19	PF0-OSC_IN	I	FT_fa	-	I2C2_SDA, SPI2_NSS/I2S2_WS, TIM1_CH3N, EVENTOUT	ADC1_IN10, OSC_IN
F9	6	6	6	E2	13	20	PF1-OSC_OUT	O	FT_a	-	SPI2_SCK/I2S2_CK, EVENTOUT	ADC2_IN10, COMP3_INM, OSC_OUT
D8	7	7	7	F3	14	21	PG10-NRST	I/O	FT	-	MCO, EVENTOUT	NRST
E8	-	-	8	F2	15	22	PC0	I/O	FT_a	-	LPTIM1_IN1, TIM1_CH1, LPUART1_RX, EVENTOUT	ADC12_IN6, COMP3_INM
C8	-	-	9	F4	16	23	PC1	I/O	TT_a	-	LPTIM1_OUT, TIM1_CH2, LPUART1_TX, QUADSPI_BK2_IO0, SAI_SD_A, EVENTOUT	ADC12_IN7, COMP3_INP

Table 10. STM32G484xx pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LPQF100	LPQF128						
F8	-	-	10	F1	17	24	PC2	I/O	FT_a	-	LPTIM1_IN2, TIM1_CH3, COMP3_OUT, TIM20_CH2, QUADSPI_BK2_IO1, EVENTOUT	ADC12_IN8
G9	-	-	11	G1	18	25	PC3	I/O	TT_a	-	LPTIM1_ETR, TIM1_CH4, SAI_D1, TIM1_BKIN2, QUADSPI_BK2_IO2, SAI_SD_A, EVENTOUT	ADC12_IN9, OPAMP5_VINP
-	-	-	-	G3	19	26	PF2	I/O	FT	-	TIM20_CH3, I2C2_SMBA, FMC_A2, EVENTOUT	-
D7	8	8	12	G4	20	27	PA0	I/O	TT_a	-	TIM2_CH1, TIM5_CH1, USART2_CTS, COMP1_OUT, TIM8_BKIN, TIM8_ETR, TIM2_ETR, EVENTOUT	ADC12_IN1, COMP1_INM, COMP3_INP, RTC_TAMP2,WKUP1
E7	9	9	13	G2	21	28	PA1	I/O	TT_a	-	RTC_REFIN, TIM2_CH2, TIM5_CH2, USART2_RTS_DE, TIM15_CH1N, EVENTOUT	ADC12_IN2, COMP1_INP, OPAMP1_VINP, OPAMP3_VINP, OPAMP6_VINM
G8	10	10	14	H1	22	29	PA2	I/O	FT_a	-	TIM2_CH3, TIM5_CH3, USART2_TX, COMP2_OUT, TIM15_CH1, QUADSPI_BK1_NCS, LPUART1_TX, USBPD_FRSTX, EVENTOUT	ADC1_IN3, COMP2_INM, OPAMP1_VOUT, WKUP4/LSCO
H9	-	-	15	D2	23	30	VSS	S	-	-	-	-
J9	-	-	16	D5	24	31	VDD	S	-	-	-	-
H8	11	11	17	H3	25	32	PA3	I/O	TT_a	-	TIM2_CH4, TIM5_CH4, SAI_CK1, USART2_RX, TIM15_CH2, QUADSPI_CLK, LPUART1_RX, SAI_MCLK_A, EVENTOUT	ADC1_IN4, COMP2_INP, OPAMP1_VINM/OPAMP 1_VINP, OPAMP5_VINM

Table 10. STM32G484xx pin definition (continued)

Pin Number							Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LPQF100	LPQF128						
D6	12	12	18	H2	26	33	PA4	I/O	TT_a	-	TIM3_CH2, SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_CK, SAI_FS_B, EVENTOUT	ADC2_IN17, DAC1_OUT1, COMP1_INM
F7	13	13	19	J1	27	34	PA5	I/O	TT_a	-	TIM2_CH1, TIM2_ETR, SPI1_SCK, USBPD_FRSTX, EVENTOUT	ADC2_IN13, DAC1_OUT2, COMP2_INM, OPAMP2_VINM
G7	14	14	20	J2	28	35	PA6	I/O	TT_a	-	TIM16_CH1, TIM3_CH1, TIM8_BKIN, SPI1_MISO, TIM1_BKIN, COMP1_OUT, QUADSPI_BK1_IO3, LPUART1_CTS, EVENTOUT	ADC2_IN3, DAC2_OUT1, OPAMP2_VOUT
J8	15	15	21	K1	29	36	PA7	I/O	TT_a	-	TIM17_CH1, TIM3_CH2, TIM8_CH1N, SPI1_MOSI, TIM1_CH1N, COMP2_OUT, QUADSPI_BK1_IO2, USBPD_FRSTX, EVENTOUT	ADC2_IN4, COMP2_INP, OPAMP1_VINP, OPAMP2_VINP
E6	16	-	22	K2	30	37	PC4	I/O	FT_fa	-	TIM1_ETR, I2C2_SCL, USART1_TX, QUADSPI_BK2_IO3, EVENTOUT	ADC2_IN5
H7	-	-	23	J3	31	38	PC5	I/O	TT_a	-	TIM15_BKIN, SAI_D3, TIM1_CH4N, USART1_RX, HRTIM_EEV10, EVENTOUT	ADC2_IN11, OPAMP1_VINM, OPAMP2_VINM, WKUP5
F6	17	16	24	H4	32	39	PB0	I/O	TT_a	-	TIM3_CH3, TIM8_CH2N, TIM1_CH2N, QUADSPI_BK1_IO1, HRTIM_FLT5, USBPD_FRSTX, EVENTOUT	ADC3_IN12/ADC1_IN15, COMP4_INP, OPAMP2_VINP, OPAMP3_VINP

Table 10. STM32G484xx pin definition (continued)

Pin Number							Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LPQF100	LPQF128						
G6	18	17	25	K3	33	40	PB1	I/O	TT_a	-	TIM3_CH4, TIM8_CH3N, TIM1_CH3N, COMP4_OUT, QUADSPI_BK1_IO0, LPUART1_RTS_DE, HRTIM_SCOUT, EVENTOUT	ADC3_IN1/ADC1_IN12, COMP1_INP, OPAMP3_VOUT, OPAMP6_VINM
J7	19	18	26	J4	34	41	PB2	I/O	TT_a	-	RTC_OUT2, LPTIM1_OUT, TIM5_CH1, TIM20_CH1, I2C3_SMBA, QUADSPI_BK2_IO1, HRTIM_SCIN, EVENTOUT	ADC2_IN12, COMP4_INM, OPAMP3_VINM
H6	-	19	27	K4	35	42	VSSA	S	-	-	-	-
J6	20	20	28	K5	36	43	VREF+	S	-	-	-	VREF_OUT
-	-	-	-	-	-	44	VREF+	S	-	-	-	-
J5	21	21	29	J5	37	45	VDDA	S	-	-	-	-
H9	-	-	-		-	46	VSS	S	-	-	-	-
J1	-	-	-		-	47	VDD	S	-	-	-	-
-	-	-	-	-	-	48	PF11	I/O	FT	-	TIM20_ETR, FMC_NE4, EVENTOUT	-
-	-	-	-	-	-	49	PF12	I/O	FT	-	TIM20_CH1, FMC_A6, EVENTOUT	-
-	-	-	-	-	-	50	PF13	I/O	FT	-	TIM20_CH2, I2C4_SMBA, FMC_A7, EVENTOUT	-
-	-	-	-	-	-	51	PF14	I/O	FT_f	-	TIM20_CH3, I2C4_SCL, FMC_A8, EVENTOUT	-
-	-	-	-	-	-	52	PF15	I/O	FT_f	-	TIM20_CH4, I2C4_SDA, FMC_A9, EVENTOUT	-
H5	-	-	-	G5	38	53	PE7	I/O	TT_a	-	TIM1_ETR, FMC_D4, SAI_SD_B, EVENTOUT	ADC3_IN4, COMP4_INP
G5	-	-	-	H5	39	54	PE8	I/O	FT_a	-	TIM5_CH3, TIM1_CH1N, FMC_D5, SAI_SCK_B, EVENTOUT	ADC345_IN6, COMP4_INM
F5	-	-	-	H6	40	55	PE9	I/O	FT_a	-	TIM5_CH4, TIM1_CH1, FMC_D6, SAI_FS_B, EVENTOUT	ADC3_IN2

Table 10. STM32G484xx pin definition (continued)

Pin Number							Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LPQF100	LPQF128						
J4	-	-	-	K6	41	56	PE10	I/O	FT_a	-	TIM1_CH2N, QUADSPI_CLK, FMC_D7, SAI_MCLK_B, EVENTOUT	ADC345_IN14
H4	-	-	-	J6	42	57	PE11	I/O	FT_a	-	TIM1_CH2, SPI4_NSS, QUADSPI_BK1_NCS, FMC_D8, EVENTOUT	ADC345_IN15
E5	-	-	-	G6	43	58	PE12	I/O	FT_a	-	TIM1_CH3N, SPI4_SCK, QUADSPI_BK1_IO0, FMC_D9, EVENTOUT	ADC345_IN16
G4	-	-	-	K7	44	59	PE13	I/O	FT_a	-	TIM1_CH3, SPI4_MISO, QUADSPI_BK1_IO1, FMC_D10, EVENTOUT	ADC3_IN3
J3	-	-	-	J7	45	60	PE14	I/O	FT_a	-	TIM1_CH4, SPI4_MOSI, TIM1_BKIN2, QUADSPI_BK1_IO2, FMC_D11, EVENTOUT	ADC4_IN1
F4	-	-	-	H7	46	61	PE15	I/O	FT_a	-	TIM1_BKIN, TIM1_CH4N, USART3_RX, QUADSPI_BK1_IO3, FMC_D12, EVENTOUT	ADC4_IN2
H3	22	22	30	J8	47	62	PB10	I/O	TT_a	-	TIM2_CH3, USART3_TX, LPUART1_RX, QUADSPI_CLK, CAN3_TXFD, TIM1_BKIN, HRTIM_FLT3, SAI_SCK_A, EVENTOUT	COMP5_INM, OPAMP3_VINM, OPAMP4_VINM
J2	-	23	31	D6	48	63	VSS	S	-	-	-	-
J1	23	24	32	D7	49	64	VDD	S	-	-	-	-
H2	24	25	33	H8	50	65	PB11	I/O	TT_a	-	TIM2_CH4, USART3_RX, LPUART1_TX, QUADSPI_BK1_NCS, CAN3_RXFD, HRTIM_FLT4, EVENTOUT	ADC12_IN14, COMP6_INP, OPAMP4_VINP, OPAMP6_VOUT

Table 10. STM32G484xx pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LPQF100	LPQF128						
G3	25	26	34	K8	51	66	PB12	I/O	TT_a	-	TIM5_ETR, I2C2_SMBA, SPI2_NSS/I2S2_WS, TIM1_BKIN, USART3_CK, LPUART1_RTS_DE, CAN2_RX, HRTIM_CHC1, EVENTOUT	ADC4_IN3/ADC1_IN11, COMP7_INM, OPAMP4_VOUT, OPAMP6_VINP
H1	26	27	35	J9	52	67	PB13	I/O	TT_a	-	SPI2_SCK/I2S2_CK, TIM1_CH1N, USART3_CTS, LPUART1_CTS, CAN2_TX, HRTIM_CHC2, EVENTOUT	ADC3_IN5, COMP5_INP, OPAMP3_VINP, OPAMP4_VINP, OPAMP6_VINP
G2	27	28	36	H9	53	68	PB14	I/O	TT_a	-	TIM15_CH1, SPI2_MISO, TIM1_CH2N, USART3_RTS_DE, COMP4_OUT, HRTIM_CHD1, EVENTOUT	ADC4_IN4/ADC1_IN5, COMP7_INP, OPAMP2_VINP, OPAMP5_VINP
E4	28	29	37	K9	54	69	PB15	I/O	TT_a	-	RTC_REFIN, TIM15_CH2, TIM15_CH1N, COMP3_OUT, TIM1_CH3N, SPI2_MOSI/I2S2_SD, HRTIM_CHD2, EVENTOUT	ADC4_IN5/ADC2_IN15, COMP6_INM, OPAMP5_VINM
G1	-	-	-	K10	55	70	PD8	I/O	TT_a	-	USART3_TX, FMC_D13, EVENTOUT	ADC4_IN12/ADC5_IN12, OPAMP4_VINM
F3	-	-	-	G8	56	71	PD9	I/O	TT_a	-	USART3_RX, CAN2_RXFD, FMC_D14, EVENTOUT	ADC4_IN13/ADC5_IN13, OPAMP6_VINP
F2	-	-	-	G7	57	72	PD10	I/O	FT_a	-	USART3_CK, CAN2_TXFD, FMC_D15, EVENTOUT	ADC345_IN7, COMP6_INM
E2	-	-	-	H10	58	73	PD11	I/O	TT_a	-	TIM5_ETR, I2C4_SMBA, USART3_CTS, FMC_A16, EVENTOUT	ADC345_IN8, COMP6_INP, OPAMP4_VINP

Table 10. STM32G484xx pin definition (continued)

Pin Number							Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LPQF100	LPQF128						
-	-	-	-	J10	59	74	PD12	I/O	TT_a	-	TIM4_CH1, USART3_RTS_DE, FMC_A17, EVENTOUT	ADC345_IN9, COMP5_INP, OPAMP5_VINP
-	-	-	-	G9	60	75	PD13	I/O	FT_a	-	TIM4_CH2, FMC_A18, EVENTOUT	ADC345_IN10, COMP5_INM
-	-	-	-	F8	61	76	PD14	I/O	TT_a	-	TIM4_CH3, FMC_D0, EVENTOUT	ADC345_IN11, COMP7_INP, OPAMP2_VINP
-	-	-	-	G10	62	77	PD15	I/O	FT_a	-	TIM4_CH4, SPI2_NSS, FMC_D1, EVENTOUT	COMP7_INM
B1	-	-	-		63	78	VSS	S	-	-	-	-
E1	-	-	-		64	79	VDD	S	-	-	-	-
E3	29	-	38	E5	65	80	PC6	I/O	FT_f	-	TIM3_CH1, HRTIM_EEV10, TIM8_CH1, I2S2_MCK, COMP6_OUT, I2C4_SCL, HRTIM_CHF1, EVENTOUT	-
D5	-	-	39	F5	66	81	PC7	I/O	FT_f	-	TIM3_CH2, HRTIM_FLT5, TIM8_CH2, I2S3_MCK, COMP5_OUT, I2C4_SDA, HRTIM_CHF2, EVENTOUT	-
-	-	-	-	F9	-	82	PG0	I/O	FT	-	TIM20_CH1N, FMC_A10, EVENTOUT	-
-	-	-	-	F10	-	83	PG1	I/O	FT	-	TIM20_CH2N, FMC_A11, EVENTOUT	-
-	-	-	-	-	-	84	PG2	I/O	FT	-	TIM20_CH3N, SPI1_SCK, FMC_A12, EVENTOUT	-
-	-	-	-	-	-	85	PG3	I/O	FT_f	-	TIM20_BKIN, I2C4_SCL, SPI1_MISO, TIM20_CH4N, FMC_A13, EVENTOUT	-
-	-	-	-	-	-	86	PG4	I/O	FT_f	-	TIM20_BKIN2, I2C4_SDA, SPI1_MOSI, FMC_A14, EVENTOUT	-

Table 10. STM32G484xx pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LPQF100	LPQF128						
C5	-	-	40	E8	67	87	PC8	I/O	FT_f	-	TIM3_CH3, HRTIM_CHE1, TIM8_CH3, TIM20_CH3, COMP7_OUT, I2C3_SCL, EVENTOUT	-
D2	-	-	41	E9	68	88	PC9	I/O	FT_f	-	TIM3_CH4, RTIM1_CHE2, TIM8_CH4, I2SCKIN, TIM8_BKIN2, I2C3_SDA, EVENTOUT	-
D1	30	30	42	E10	69	89	PA8	I/O	FT_a	-	MCO, I2C3_SCL, I2C2_SDA, I2S2_MCK, TIM1_CH1, USART1_CK, COMP7_OUT, TIM4_ETR, CAN3_RX, SAI_CK2, HRTIM_CHA1, SAI_SCK_A, EVENTOUT	ADC5_IN1, OPAMP5_VOUT
D4	31	31	43	D10	70	90	PA9	I/O	FT_fa	-	I2C3_SMBA, I2C2_SCL, I2S3_MCK, TIM1_CH2, USART1_TX, OMP5_OUT, TIM15_BKIN, TIM2_CH3, CAN1_RXFD, HRTIM_CHA2, SAI_FS_A, EVENTOUT	ADC5_IN2, USBPD_DBCC1
D3	32	32	44	D9	71	91	PA10	I/O	FT_fa	-	TIM17_BKIN, USB_CRS_SYNC, I2C2_SMBA, SPI2_MISO, TIM1_CH3, USART1_RX, COMP6_OUT, CAN1_TXFD, TIM2_CH4, TIM8_BKIN, SAI_D1, HRTIM_CHB1, SAI_SD_A, EVENTOUT	USBPD_DBCC2

Table 10. STM32G484xx pin definition (continued)

Pin Number							Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LPQF100	LPQF128						
C2	33	33	45	C10	72	92	PA11	I/O	FT	-	SPI2_MOSI/I2S2_SD, TIM1_CH1N, USART1_CTS, COMP1_OUT, CAN1_RX, TIM4_CH1, TIM1_CH4, TIM1_BKIN2, HRTIM_CHB2, EVENTOUT	USB_DM
C1	34	34	46	C9	73	93	PA12	I/O	FT	-	TIM16_CH1, I2SCKIN, TIM1_CH2N, USART1_RTS_DE, COMP2_OUT, CAN1_TX, TIM4_CH2, TIM1_ETR, HRTIM_FLT1, EVENTOUT	USB_DP
A8	-	35	47	E6	74	94	VSS	S	-	-	-	-
A1	35	36	48	F7	75	95	VDD	S	-	-	-	-
B2	36	37	49	D8	76	96	PA13	I/O	FT_f	-	SWDIO-JTMS, TIM16_CH1N, I2C4_SCL, I2C1_SCL, IR_OUT, USART3_CTS, TIM4_CH3, SAI_SD_B, EVENTOUT	-
-	-	-	-	-	-	97	PF6	I/O	FT_f	-	TIM5_ETR, TIM4_CH4, SAI_SD_B, I2C2_SCL, TIM5_CH1, USART3_RTS, QUADSPI_BK1_IO3, EVENTOUT	-
C3	37	38	50	B10	77	98	PA14	I/O	FT_f	-	SWCLK-JTCK, LPTIM1_OUT, I2C4_SMBA, I2C1_SDA, TIM8_CH2, TIM1_BKIN, USART2_TX, CAN3_TXFD, SAI_FS_B, EVENTOUT	-

Table 10. STM32G484xx pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LPQF100	LPQF128						
A2	38	39	51	B9	78	99	PA15	I/O	FT_f	-	JTDI, TIM2_CH1, TIM8_CH1, I2C1_SCL, SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_RX, UART4_RTS_DE, TIM1_BKIN, CAN3_TX, HRTIM_FLT2, TIM2_ETR, EVENTOUT	-
B3	39	-	52	C8	79	100	PC10	I/O	FT	-	TIM8_CH1N, UART4_TX, SPI3_SCK/I2S3_CK, USART3_TX, HRTIM_FLT6, EVENTOUT	-
C4	40	-	53	C7	80	101	PC11	I/O	FT_f	-	HRTIM_EEV2, TIM8_CH2N, UART4_RX, SPI3_MISO, USART3_RX, I2C3_SDA, EVENTOUT	-
A3	-	-	54	A10	81	102	PC12	I/O	FT	-	TIM5_CH2, HRTIM_EEV1, TIM8_CH3N, UART5_TX, SPI3_MOSI/I2S3_SD, USART3_CK, USBPD_FRSTX, EVENTOUT	-
-	-	-	-	-	-	103	PG5	I/O	FT	-	TIM20_ETR, SPI1_NSS, LPUART1_CTS, FMC_A15, EVENTOUT	-
-	-	-	-	-	-	104	PG6	I/O	FT	-	TIM20_BKIN, I2C3_SMBA, LPUART1_RTS_DE, FMC_INT, EVENTOUT	-
-	-	-	-	-	-	105	PG7	I/O	FT_f	-	SAI_CK1, I2C3_SCL, LPUART1_TX, FMC_INT, SAI_MCLK_A, EVENTOUT	-
-	-	-	-	-	-	106	PG8	I/O	FT_f	-	I2C3_SDA, LPUART1_RX, FMC_NE3, EVENTOUT	-

Table 10. STM32G484xx pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LPQF100	LPQF128						
-	-	-	-	-	-	107	PG9	I/O	FT	-	SPI3_SCK, USART1_TX, FMC_NCE/FMC_NE2, TIM15_CH1N, EVENTOUT	-
B4	-	-	-	B8	82	108	PD0	I/O	FT	-	TIM8_CH4N, CAN1_RX, FMC_D2, EVENTOUT	-
A4	-	-	-	A9	83	109	PD1	I/O	FT	-	TIM8_CH4, TIM8_BKIN2, CAN1_TX, FMC_D3, EVENTOUT	-
-	-	-	-	E7	-	110	VSS	S	-	-	-	-
A1	-	-	-	-	-	111	VDD	S	-	-	-	-
B5	-	-	55	B7	84	112	PD2	I/O	FT	-	TIM3_ETR, TIM8_BKIN, UART5_RX, EVENTOUT	-
-	-	-	-	C6	85	113	PD3	I/O	FT	-	TIM2_CH1/ TIM2_ETR, USART2_CTS, QUADSPI_BK2_NCS, FMC_CLK, EVENTOUT	-
-	-	-	-	A8	86	114	PD4	I/O	FT	-	TIM2_CH2, USART2_RTS_DE, CAN1_RXFD, QUADSPI_BK2_IO0, FMC_NOE, EVENTOUT	-
-	-	-	-	A7	87	115	PD5	I/O	FT	-	USART2_TX, CAN1_TXFD, QUADSPI_BK2_IO1, FMC_NWE, EVENTOUT	-
-	-	-	-	A6	88	116	PD6	I/O	FT	-	TIM2_CH4, SAI_D1, USART2_RX, CAN2_RXFD, QUADSPI_BK2_IO2, FMC_NWAIT, SAI_SD_A, EVENTOUT	-
-	-	-	-	B6	89	117	PD7	I/O	FT	-	TIM2_CH3, USART2_CK, QUADSPI_BK2_IO3, FMC_NCE/FMC_NE1, EVENTOUT	-

Table 10. STM32G484xx pin definition (continued)

Pin Number							Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LPQF100	LPQF128						
A5	41	40	56	A5	90	118	PB3	I/O	FT	-	JTDO-TRACESWO, TIM2_CH2, TIM4_ETR, USB_CRS_SYNC, TIM8_CH1N, SPI1_SCK, SPI3_SCK/I2S3_CK, USART2_TX, TIM3_ETR, CAN3_RX, HRTIM_SCOUT, HRTIM_EEV9, SAI_SCK_B, EVENTOUT	-
C6	42	41	57	C5	91	119	PB4	I/O	FT	-	JTRST, TIM16_CH1, TIM3_CH1, TIM8_CH2N, SPI1_MISO, SPI3_MISO, USART2_RX, UART5_RTS_DE, TIM17_BKIN, CAN3_TX, HRTIM_EEV7, SAI_MCLK_B, EVENTOUT	USBPD_CC2
A6	43	42	58	B5	92	120	PB5	I/O	FT_f	-	TIM16_BKIN, TIM3_CH2, TIM8_CH3N, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI/I2S3_SD, USART2_CK, I2C3_SDA, CAN2_RX, TIM17_CH1, LPTIM1_IN1, SAI_SD_B, HRTIM_EEV6, UART5_CTS, EVENTOUT	-
B6	44	43	59	A4	93	121	PB6	I/O	FT	-	TIM16_CH1N, TIM4_CH1, TIM8_CH1, TIM8_ETR, USART1_TX, COMP4_OUT, CAN2_TX, TIM8_BKIN2, LPTIM1_ETR, HRTIM_SCIN, HRTIM_EEV4, SAI_FS_B, EVENTOUT	USBPD_CC1

Table 10. STM32G484xx pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	QFPN48	LQFP48	LQFP64	TFBGA100	LPQF100	LPQF128						
C7	45	44	60	B4	94	122	PB7	I/O	FT_f	-	TIM17_CH1N, TIM4_CH2, I2C4_SDA, I2C1_SDA, TIM8_BKIN, USART1_RX, COMP3_OUT, CAN2_TXFD, TIM3_CH4, LPTIM1_IN2, FMC_NL, HRTIM_EEV3, UART4_CTS, EVENTOUT	PVD_IN
B7	46	45	61	A3	95	123	PB8-BOOT0	I/O	FT_f	-	TIM16_CH1, TIM4_CH3, SAI_CK1, I2C1_SCL, USART3_RX, COMP1_OUT, CAN1_RX, TIM8_CH2, TIM1_BKIN, HRTIM_EEV8, SAI_MCLK_A, EVENTOUT	-
A7	47	46	62	A2	96	124	PB9	I/O	FT_f	-	TIM17_CH1, TIM4_CH4, SAI_D2, I2C1_SDA, IR_OUT, USART3_TX, COMP2_OUT, CAN1_TX, TIM8_CH3, TIM1_CH3N, HRTIM_EEV5, SAI_FS_A, EVENTOUT	-
-	-	-	-	C4	97	125	PE0	I/O	FT	-	TIM4_ETR, TIM20_CH4N, TIM16_CH1, TIM20_ETR, USART1_TX, CAN1_RXFD, FMC_NBL0, EVENTOUT	-
-	-	-	-	B3	98	126	PE1	I/O	FT	-	TIM17_CH1, TIM20_CH4, USART1_RX, CAN1_TXFD, FMC_NBL1, EVENTOUT	-
-	-	47	63	F6	99	127	VSS	S	-	-	-	-
A9	48	48	64	-	100	128	VDD	S	-	-	-	-

1. Function availability depends on the chosen device.

Table 11. Alternate function

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ TIM2/5/ 15/16/17	I2C3/ TIM1/2/3/4/5/8/15/20/ GPCOMP1	QUADSPI/ I2C3/4/SAI/ USB/ HRTIM/ TIM8/15/20/GPCOMP3/ TSC	I2C1/2/3/4/ TIM1/8/16/17	QUADSPI/SPI1/2/3/4/I2S2/3/ I2C4/ UART4/5/TIM8/ Infrared	QUADSPI/SPI2/3/ I2S2/3/ TIM1/5/8/20/ Infrared	USART1/2/3/CAN/ GPCOMP5/6/7	I2C3/4/ UART4/5/LPUART1/GPCOMP1/2/3/4/5/6/7	CAN/ TIM1/8/15/CAN1/2	QUADSPI/TIM2/3/4/8/17	LPTIM1/ TIM1/8/CAN1/3	SDIO/FMC/ LPUART1/ SAI/ HRTIM/TIM1	SAI/HRTIM/OPAMP2	UART4/5/ SAI/ TIM2/15/ UCPD	EVENT
Port A	PA0	-	TIM2_CH1	TIM5_CH1	-	-	-	-	USART2_CTS	COMP1_OUT	TIM8_BKIN	TIM8_ETR	-	-	-	TIM2_ETR	EVENTOUT
	PA1	RTC_REFIN	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS_DE	-	TIM15_CH1N	-	-	-	-	-	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	-	-	-	-	USART2_TX	COMP2_OUT	TIM15_CH1	QUADSPI_BK1_NCS	-	LPUART1_TX	-	UCPD_FRSTX	EVENTOUT
	PA3	-	TIM2_CH4	TIM5_CH4	SAI_CK1	-	-	-	USART2_RX	-	TIM15_CH2	QUADSPI_CLK	-	LPUART1_RX	SAI_MCLK_A	-	EVENTOUT
	PA4	-	-	TIM3_CH2	-	-	SPI1_NSS	SPI3_NSS/I2S3_WS	USART2_CK	-	-	-	-	-	SAI_FS_B	-	EVENTOUT
	PA5	-	TIM2_CH1	TIM2_ETR	-	-	SPI1_SCK	-	-	-	-	-	-	-	-	UCPD_FRSTX	EVENTOUT
	PA6	-	TIM16_CH1	TIM3_CH1	-	TIM8_BKIN	SPI1_MISO	TIM1_BKIN	-	COMP1_OUT	-	QUADSPI_BK1_IO3	-	LPUART1_CTS	-	-	EVENTOUT
	PA7	-	TIM17_CH1	TIM3_CH2	-	TIM8_CH1N	SPI1_MOSI	TIM1_CH1N	-	COMP2_OUT	-	QUADSPI_BK1_IO2	-	-	-	UCPD_FRSTX	EVENTOUT
	PA8	MCO	-	-	-	I2C2_SMBA	I2S2_MCK	TIM1_CH1	USART1_CK	COMP7_OUT	-	TIM4_ETR	CAN3_RX	SAI_CK2	HRTIM_CHA1	SAI_SCK_A	EVENTOUT
	PA9	-	-	I2C3_SMBA	-	I2C2_SCL	I2S3_MCK	TIM1_CH2	USART1_TX	COMP5_OUT	TIM15_BKIN	TIM2_CH3	CAN1_RXFD	-	HRTIM_CHA2	SAI_FS_A	EVENTOUT
	PA10	-	TIM17_BKIN	I2C3_SCL	USB_CRS_SYNC	I2C2_SDA	SPI2_MISO	TIM1_CH3	USART1_RX	COMP6_OUT	CAN1_TXFD	TIM2_CH4	TIM8_BKIN	SAI_D1	HRTIM_CHB1	SAI_SD_A	EVENTOUT
	PA11	-	-	-	-	-	SPI2_MOSI/I2S2_SD	TIM1_CH1N	USART1_CTS	COMP1_OUT	CAN1_RX	TIM4_CH1	TIM1_CH4	TIM1_BKIN2	HRTIM_CHB2	-	EVENTOUT
	PA12	-	TIM16_CH1	-	-	-	I2SCKIN	TIM1_CH2N	USART1_RTS_DE	COMP2_OUT	CAN1_TX	TIM4_CH2	TIM1_ETR	-	HRTIM_FLT1	-	EVENTOUT
	PA13	SWDIO-JTMS	TIM16_CH1N	-	-	-	IR_OUT	-	USART3_CTS	-	-	TIM4_CH3	-	-	SAI_SD_B	-	EVENTOUT
	PA14	SWCLK-JTCK	LPTIM1_OUT	-	I2C4_SMBA	I2C1_SDA	TIM8_CH2	TIM1_BKIN	USART2_TX	-	-	-	CAN3_TXFD	-	SAI_FS_B	-	EVENTOUT
	PA15	JTDI	TIM2_CH1	TIM8_CH1	-	I2C1_SCL	SPI1_NSS	SPI3_NSS/I2S3_WS	USART2_RX	UART4_RTS_DE	TIM1_BKIN	-	CAN3_TX	-	HRTIM_FLT2	TIM2_ETR	EVENTOUT

Table 11. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ TIM2/5/ 15/16/17	I2C3/ TIM1/2/3/4/5/8/15/20/ GPCOMP1	QUADSPI/ I2C3/4/SAI/ USB/ HRTIM/ TIM8/15/20/GPCOMP3/ TSC	I2C1/2/3/4/ TIM1/8/16/17	QUADSPI/SPI1/2/3/4/I2S2/3/ I2C4/ UART4/5/TIM8/ Infrared	QUADSPI/SPI2/3/ I2S2/3/ TIM1/5/8/20/ Infrared	USART1/2/3/CAN/ GPCOMP5/6/7	I2C3/4/ UART4/5/LPUART1/GPCOMP1/2/3/4/5/6/7	CAN/ TIM1/8/15/CAN1/2	QUADSPI/TIM2/3/4/8/17	LPTIM1/ TIM1/8/CAN1/3	SDIO/FMC/ LPUART1/ SAI/ HRTIM/TIM1	SAI/HRTIM/OPAMP2	UART4/5/ SAI/ TIM2/15/ UCPD	EVENT
Port B	PB0	-	-	TIM3_CH3	-	TIM8_CH2N	-	TIM1_CH2N	-	-	-	QUADSPI_BK1_IO1	-	-	HRTIM_FLT5	UCPD_FRSTX	EVENT OUT
	PB1	-	-	TIM3_CH4	-	TIM8_CH3N	-	TIM1_CH3N	-	COMP4_OUT	-	QUADSPI_BK1_IO0	-	LPUART1_RTS_DE	HRTIM_SCOUT	-	EVENT OUT
	PB2	-	LPTIM1_OUT	TIM5_CH1	TIM20_CH1	I2C3_SMBA	-	-	-	-	-	QUADSPI_BK2_IO1	-	-	HRTIM_SCIN	-	EVENT OUT
	PB3	JTDO-TRACESWO	TIM2_CH2	TIM4_ETR	USB_CRS_SYNC	TIM8_CH1N	SPI1_SCK	SPI3_SCK/I2S3_CK	USART2_TX	-	-	TIM3_ETR	CAN3_RX	HRTIM_SCOUT	HRTIM_EEV9	SAI_SCK_B	EVENT OUT
	PB4	JTRST	TIM16_CH1	TIM3_CH1	-	TIM8_CH2N	SPI1_MISO	SPI3_MISO	USART2_RX	UART5_RTS_DE	-	TIM17_BKIN	CAN3_TX	-	HRTIM_EEV7	SAI_MCLK_B	EVENT OUT
	PB5	-	TIM16_BKIN	TIM3_CH2	TIM8_CH3N	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI/I2S3_SD	USART2_CK	I2C3_SDA	CAN2_RX	TIM17_CH1	LPTIM1_IN1	SAI_SD_B	HRTIM_EEV6	UART5_CTS	EVENT OUT
	PB6	-	TIM16_CH1N	TIM4_CH1	I2C4_SCL	I2C1_SCL	TIM8_CH1	TIM8_ETR	USART1_TX	COMP4_OUT	CAN2_TX	TIM8_BKIN2	LPTIM1_ETR	HRTIM_SCIN	HRTIM_EEV4	SAI_FS_B	EVENT OUT
	PB7	-	TIM17_CH1N	TIM4_CH2	I2C4_SDA	I2C1_SDA	TIM8_BKIN	-	USART1_RX	COMP3_OUT	CAN2_TXFD	TIM3_CH4	LPTIM1_IN2	FMC_NL	HRTIM_EEV3	UART4_CTS	EVENT OUT
	PB8	-	TIM16_CH1	TIM4_CH3	SAI_CK1	I2C1_SCL	-	-	USART3_RX	COMP1_OUT	CAN1_RX	TIM8_CH2	-	TIM1_BKIN	HRTIM_EEV8	SAI_MCLK_A	EVENT OUT
	PB9	-	TIM17_CH1	TIM4_CH4	SAI_D2	I2C1_SDA	-	IR_OUT	USART3_TX	COMP2_OUT	CAN1_TX	TIM8_CH3	-	TIM1_CH3N	HRTIM_EEV5	SAI_FS_A	EVENT OUT
	PB10	-	TIM2_CH3	-	-	-	-	-	USART3_TX	LPUART1_RX	-	QUADSPI_CLK	CAN3_TXFD	TIM1_BKIN	HRTIM_FLT3	SAI_SCK_A	EVENT OUT
	PB11	-	TIM2_CH4	-	-	-	-	-	USART3_RX	LPUART1_TX	-	QUADSPI_BK1_NCS	CAN3_RXFD	-	HRTIM_FLT4	-	EVENT OUT
	PB12	-	-	TIM5_ETR	-	I2C2_SMBA	SPI2_NSS/I2S2_WS	TIM1_BKIN	USART3_CK	LPUART1_RTS_DE	CAN2_RX	-	-	-	HRTIM_CHC1	-	EVENT OUT
	PB13	-	-	-	-	-	SPI2_SCK/I2S2_CK	TIM1_CH1N	USART3_CTS	LPUART1_CTS	CAN2_TX	-	-	-	HRTIM_CHC2	-	EVENT OUT
	PB14	-	TIM15_CH1	-	-	-	SPI2_MISO	TIM1_CH2N	USART3_RTS_DE	COMP4_OUT	-	-	-	-	HRTIM_CHD1	-	EVENT OUT
	PB15	RTC_REFIN	TIM15_CH2	TIM15_CH1N	COMP3_OUT	TIM1_CH3N	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-	-	HRTIM_CHD2	-	EVENT OUT

Table 11. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ TIM2/5/ 15/16/17	I2C3/ TIM1/2/3/4/5/8/15/20/ GPCOMP1	QUADSPI/ I2C3/4/SAI/ USB/ HRTIM/ TIM8/15/20/GPCOMP3/ TSC	I2C1/2/3/4/ TIM1/8/16/17	QUADSPI/SPI1/2/3/4/I2S2/3/ I2C4/ UART4/5/TIM8/ Infrared	QUADSPI/SPI2/3/ I2S2/3/ TIM1/5/8/20/ Infrared	USART1/2/3/CAN/ GPCOMP5/6/7	I2C3/4/ UART4/5/LPUART1/GPCOMP1/2/3/4/5/6/7	CAN/ TIM1/8/15/CAN1/2	QUADSPI/TIM2/3/4/8/17	LPTIM1/ TIM1/8/CAN1/3	SDIO/FMC/ LPUART1/ SAI/ HRTIM/TIM1	SAI/HRTIM/OPAMP2	UART4/5/ SAI/ TIM2/15/ UCPD	EVENT
Port C	PC0	-	LPTIM1_IN1	TIM1_CH1	-	-	-	-	-	LPUART1_RX	-	-	-	-	-	-	EVENT OUT
	PC1	-	LPTIM1_OUT	TIM1_CH2	-	-	-	-	-	LPUART1_TX	-	QUADSPI_BK2_IO0	-	-	SAI_SD_A	-	EVENT OUT
	PC2	-	LPTIM1_IN2	TIM1_CH3	COMP3_OUT	-	-	TIM20_CH2	-	-	-	QUADSPI_BK2_IO1	-	-	-	-	EVENT OUT
	PC3	-	LPTIM1_ETR	TIM1_CH4	SAI_D1	-	-	TIM1_BKIN2	-	-	-	QUADSPI_BK2_IO2	-	-	SAI_SD_A	-	EVENT OUT
	PC4	-	-	TIM1_ETR	-	I2C2_SCL	-	-	USART1_TX	-	-	QUADSPI_BK2_IO3	-	-	-	-	EVENT OUT
	PC5	-	-	TIM15_BKIN	SAI_D3	-	-	TIM1_CH4N	USART1_RX	-	-	-	-	-	HRTIM_EEV10	-	EVENT OUT
	PC6	-	-	TIM3_CH1	HRTIM_EEV10	TIM8_CH1	-	I2S2_MCK	COMP6_OUT	I2C4_SCL	-	-	-	-	HRTIM_CHF1	-	EVENT OUT
	PC7	-	-	TIM3_CH2	HRTIM_FLT5	TIM8_CH2	-	I2S3_MCK	COMP5_OUT	I2C4_SDA	-	-	-	-	HRTIM_CHF2	-	EVENT OUT
	PC8	-	-	TIM3_CH3	HRTIM_CHE1	TIM8_CH3	-	TIM20_CH3	COMP7_OUT	I2C3_SCL	-	-	-	-	-	-	EVENT OUT
	PC9	-	-	TIM3_CH4	HRTIM_CHE2	TIM8_CH4	I2SCKIN	TIM8_BKIN2	-	I2C3_SDA	-	-	-	-	-	-	EVENT OUT
	PC10	-	-	-	-	TIM8_CH1N	UART4_TX	SPI3_SCK/I2S3_CK	USART3_TX	-	-	-	-	-	HRTIM_FLT6	-	EVENT OUT
	PC11	-	-	-	HRTIM_EEV2	TIM8_CH2N	UART4_RX	SPI3_MISO	USART3_RX	I2C3_SDA	-	-	-	-	-	-	EVENT OUT
	PC12	-	TIM5_CH2	-	HRTIM_EEV1	TIM8_CH3N	UART5_TX	SPI3_MOSI/I2S3_SD	USART3_CK	-	-	-	-	-	-	UCPD_FRSTX	EVENT OUT
	PC13	-	-	TIM1_BKIN	-	TIM1_CH1N	-	TIM8_CH4N	-	-	-	-	-	-	-	-	EVENT OUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT

Table 11. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ TIM2/5/ 15/16/17	I2C3/ TIM1/2/3/4/5/8/15/20/ GPCOMP1	QUADSPI/ I2C3/4/SAI/ USB/ HRTIM/ TIM8/15/20/GPCOMP3/ TSC	I2C1/2/3/4/ TIM1/8/16/17	QUADSPI/SPI1/2/3/4/I2S2/3/ I2C4/ UART4/5/TIM8/ Infrared	QUADSPI/SPI2/3/ I2S2/3/ TIM1/5/8/20/ Infrared	USART1/2/3/CAN/ GPCOMP5/6/7	I2C3/4/ UART4/5/LPUART1/GPCOMP1/2/3/4/5/6/7	CAN/ TIM1/8/15/CAN1/2	QUADSPI/TIM2/3/4/8/17	LPTIM1/ TIM1/8/CAN1/3	SDIO/FMC/ LPUART1/ SAI/ HRTIM/TIM1	SAI/HRTIM/OPAMP2	UART4/5/ SAI/ TIM2/15/ UCPD	EVENT
Port D	PD0	-	-	-	-	-	-	TIM8_CH4N	-	-	CAN1_RX	-	-	FMC_D2	-	-	EVENT OUT
	PD1	-	-	-	-	TIM8_CH4	-	TIM8_BKIN2	-	-	CAN1_TX	-	-	FMC_D3	-	-	EVENT OUT
	PD2	-	-	TIM3_ETR	-	TIM8_BKIN	UART5_RX	-	-	-	-	-	-	-	-	-	EVENT OUT
	PD3	-	-	TIM2_CH1/TIM2_ETR	-	-	-	-	USART2_CTS	-	-	QUADSPI_BK2_NCS	-	FMC_CLK	-	-	EVENT OUT
	PD4	-	-	TIM2_CH2	-	-	-	-	USART2_RTS_DE	-	CAN1_RXFD	QUADSPI_BK2_IO0	-	FMC_NOE	-	-	EVENT OUT
	PD5	-	-	-	-	-	-	-	USART2_TX	-	CAN1_TXFD	QUADSPI_BK2_IO1	-	FMC_NWE	-	-	EVENT OUT
	PD6	-	-	TIM2_CH4	SAI_D1	-	-	-	USART2_RX	-	CAN2_RXFD	QUADSPI_BK2_IO2	-	FMC_NWAIT	SAI_SD_A	-	EVENT OUT
	PD7	-	-	TIM2_CH3	-	-	-	-	USART2_CK	-	-	QUADSPI_BK2_IO3	-	FMC_NCE/FMC_NE1	-	-	EVENT OUT
	PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	-	FMC_D13	-	-	EVENT OUT
	PD9	-	-	-	-	-	-	-	USART3_RX	-	CAN2_RXFD	-	-	FMC_D14	-	-	EVENT OUT
	PD10	-	-	-	-	-	-	-	USART3_CK	-	CAN2_TXFD	-	-	FMC_D15	-	-	EVENT OUT
	PD11	-	TIM5_ETR	-	-	I2C4_SMBA	-	-	USART3_CTS	-	-	-	-	FMC_A16	-	-	EVENT OUT
	PD12	-	-	TIM4_CH1	-	-	-	-	USART3_RTS_DE	-	-	-	-	FMC_A17	-	-	EVENT OUT
	PD13	-	-	TIM4_CH2	-	-	-	-	-	-	-	-	-	FMC_A18	-	-	EVENT OUT
	PD14	-	-	TIM4_CH3	-	-	-	-	-	-	-	-	-	FMC_D0	-	-	EVENT OUT
	PD15	-	-	TIM4_CH4	-	-	-	SPI2_NSS	-	-	-	-	-	FMC_D1	-	-	EVENT OUT

Table 11. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ TIM2/5/ 15/16/17	I2C3/ TIM1/2/3/4/5/8/15/20/ GPCOMP1	QUADSPI/ I2C3/4/SAI/ USB/ HRTIM/ TIM8/15/20/GPCOMP3/ TSC	I2C1/2/3/4/ TIM1/8/16/17	QUADSPI/SPI1/2/3/4/I2S2/3/ I2C4/ UART4/5/TIM8/ Infrared	QUADSPI/SPI2/3/ I2S2/3/ TIM1/5/8/20/ Infrared	USART1/2/3/CAN/ GPCOMP5/6/7	I2C3/4/ UART4/5/LPUART1/GPCOMP1/2/3/4/5/6/7	CAN/ TIM1/8/15/CAN1/2	QUADSPI/TIM2/3/4/8/17	LPTIM1/ TIM1/8/CAN1/3	SDIO/FMC/ LPUART1/ SAI/ HRTIM/TIM1	SAI/HRTIM/OPAMP2	UART4/5/ SAI/ TIM2/15/ UCPD	EVENT
Port E	PE0	-	-	TIM4_ETR	TIM20_CH4N	TIM16_CH1	-	TIM20_ETR	USART1_TX	-	CAN1_RXFD	-	-	FMC_NBL0	-	-	EVENT OUT
	PE1	-	-	-	-	TIM17_CH1	-	TIM20_CH4	USART1_RX	-	CAN1_TXFD	-	-	FMC_NBL1	-	-	EVENT OUT
	PE2	TRACECK	-	TIM3_CH1	SAI_CK1	-	SPI4_SCK	TIM20_CH1	-	-	-	-	-	FMC_A23	SAI_MCLK_A	-	EVENT OUT
	PE3	TRACED0	-	TIM3_CH2	-	-	SPI4_NSS	TIM20_CH2	-	-	-	-	-	FMC_A19	SAI_SD_B	-	EVENT OUT
	PE4	TRACED1	-	TIM3_CH3	SAI_D2	-	SPI4_NSS	TIM20_CH1N	-	-	-	-	-	FMC_A20	SAI_FS_A	-	EVENT OUT
	PE5	TRACED2	-	TIM3_CH4	SAI_CK2	-	SPI4_MISO	TIM20_CH2N	-	-	-	-	-	FMC_A21	SAI_SCK_A	-	EVENT OUT
	PE6	TRACED3	-	-	SAI_D1	-	SPI4_MOSI	TIM20_CH3N	-	-	-	-	-	FMC_A22	SAI_SD_A	-	EVENT OUT
	PE7	-	-	TIM1_ETR	-	-	-	-	-	-	-	-	-	FMC_D4	SAI_SD_B	-	EVENT OUT
	PE8	-	TIM5_CH3	TIM1_CH1N	-	-	-	-	-	-	-	-	-	FMC_D5	SAI_SCK_B	-	EVENT OUT
	PE9	-	TIM5_CH4	TIM1_CH1	-	-	-	-	-	-	-	-	-	FMC_D6	SAI_FS_B	-	EVENT OUT
	PE10	-	-	TIM1_CH2N	-	-	-	-	-	-	-	QUADSPI_CLK	-	FMC_D7	SAI_MCLK_B	-	EVENT OUT
	PE11	-	-	TIM1_CH2	-	-	SPI4_NSS	-	-	-	-	QUADSPI_BK1_NCS	-	FMC_D8	-	-	EVENT OUT
	PE12	-	-	TIM1_CH3N	-	-	SPI4_SCK	-	-	-	-	QUADSPI_BK1_IO0	-	FMC_D9	-	-	EVENT OUT
	PE13	-	-	TIM1_CH3	-	-	SPI4_MISO	-	-	-	-	QUADSPI_BK1_IO1	-	FMC_D10	-	-	EVENT OUT
	PE14	-	-	TIM1_CH4	-	-	SPI4_MOSI	TIM1_BKIN2	-	-	-	QUADSPI_BK1_IO2	-	FMC_D11	-	-	EVENT OUT
	PE15	-	-	TIM1_BKIN	-	-	-	TIM1_CH4N	USART3_RX	-	-	QUADSPI_BK1_IO3	-	FMC_D12	-	-	EVENT OUT

Table 11. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ TIM2/5/ 15/16/17	I2C3/ TIM1/2/3/4/5/8/15/20/ GPCOMP1	QUADSPI/ I2C3/4/SAI/ USB/ HRTIM/ TIM8/15/20/GPCOMP3/ TSC	I2C1/2/3/4/ TIM1/8/16/17	QUADSPI/SPI1/2/3/4/I2S2/3/ I2C4/ UART4/5/TIM8/ Infrared	QUADSPI/SPI2/3/ I2S2/3/ TIM1/5/8/20/ Infrared	USART1/2/3/CAN/ GPCOMP5/6/7	I2C3/4/ UART4/5/LPUART1/GPCOMP1/2/3/4/5/6/7	CAN/ TIM1/8/15/CAN1/2	QUADSPI/TIM2/3/4/8/17	LPTIM1/ TIM1/8/CAN1/3	SDIO/FMC/ LPUART1/ SAI/ HRTIM/TIM1	SAI/HRTIM/OPAMP2	UART4/5/ SAI/ TIM2/15/ UCPD	EVENT
Port F	PF0	-	-	-	-	I2C2_SDA	SPI2_NSS/I2S2_WS	TIM1_CH3N	-	-	-	-	-	-	-	-	EVENT OUT
	PF1	-	-	-	-	-	SPI2_SCK/I2S2_CK	-	-	-	-	-	-	-	-	-	EVENT OUT
	PF2	-	-	TIM20_CH3	-	I2C2_SMBA	-	-	-	-	-	-	-	FMC_A2	-	-	EVENT OUT
	PF3	-	-	TIM20_CH4	-	I2C3_SCL	-	-	-	-	-	-	-	FMC_A3	-	-	EVENT OUT
	PF4	-	-	COMP1_OUT	TIM20_CH1N	I2C3_SDA	-	-	-	-	-	-	-	FMC_A4	-	-	EVENT OUT
	PF5	-	-	TIM20_CH2N	-	-	-	-	-	-	-	-	-	FMC_A5	-	-	EVENT OUT
	PF6	-	TIM5_ETR	TIM4_CH4	SAI_SD_B	I2C2_SCL	-	TIM5_CH1	USART3_RTS	-	-	QUADSPI_BK1_IO3	-	-	-	-	EVENT OUT
	PF7	-	-	TIM20_BKIN	-	-	-	TIM5_CH2	-	-	-	QUADSPI_BK1_IO2	-	FMC_A1	SAI_MCLK_B	-	EVENT OUT
	PF8	-	-	TIM20_BKIN2	-	-	-	TIM5_CH3	-	-	-	QUADSPI_BK1_IO0	-	FMC_A24	SAI_SCK_B	-	EVENT OUT
	PF9	-	-	TIM20_BKIN	TIM15_CH1	-	SPI2_SCK	TIM5_CH4	-	-	-	QUADSPI_BK1_IO1	-	FMC_A25	SAI_FS_B	-	EVENT OUT
	PF10	-	-	TIM20_BKIN2	TIM15_CH2	-	SPI2_SCK	-	-	-	-	QUADSPI_CLK	-	FMC_A0	SAI_D3	-	EVENT OUT
	PF11	-	-	TIM20_ETR	-	-	-	-	-	-	-	-	-	FMC_NE4	-	-	EVENT OUT
	PF12	-	-	TIM20_CH1	-	-	-	-	-	-	-	-	-	FMC_A6	-	-	EVENT OUT
	PF13	-	-	TIM20_CH2	-	I2C4_SMBA	-	-	-	-	-	-	-	FMC_A7	-	-	EVENT OUT
	PF14	-	-	TIM20_CH3	-	I2C4_SCL	-	-	-	-	-	-	-	FMC_A8	-	-	EVENT OUT
	PF15	-	-	TIM20_CH4	-	I2C4_SDA	-	-	-	-	-	-	-	FMC_A9	-	-	EVENT OUT

Table 11. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ TIM2/5/ 15/16/17	I2C3/ TIM1/2/3/4/5/8/15/20/ GPCOMP1	QUADSPI/ I2C3/4/SAI/ USB/ HRTIM/ TIM8/15/20/GPCOMP3/ TSC	I2C1/2/3/4/ TIM1/8/16/17	QUADSPI/SPI1/2/3/4/I2S2/3/ I2C4/ UART4/5/TIM8/ Infrared	QUADSPI/SPI2/3/ I2S2/3/ TIM1/5/8/20/ Infrared	USART1/2/3/CAN/ GPCOMP5/6/7	I2C3/4/ UART4/5/LPUART1/GPCOMP1/2/3/4/5/6/7	CAN/ TIM1/8/15/CAN1/2	QUADSPI/TIM2/3/4/8/17	LPTIM1/ TIM1/8/CAN1/3	SDIO/FMC/ LPUART1/ SAI/ HRTIM/TIM1	SAI/HRTIM/OPAMP2	UART4/5/ SAI/ TIM2/15/ UCPD	EVENT
Port G	PG0	-	-	TIM20_CH1N	-	-	-	-	-	-	-	-	-	FMC_A10	-	-	EVENT OUT
	PG1	-	-	TIM20_CH2N	-	-	-	-	-	-	-	-	-	FMC_A11	-	-	EVENT OUT
	PG2	-	-	TIM20_CH3N	-	-	SPI1_SCK	-	-	-	-	-	-	FMC_A12	-	-	EVENT OUT
	PG3	-	-	TIM20_BKIN	-	I2C4_ SCL	SPI1_MISO	TIM20_CH4N	-	-	-	-	-	FMC_A13	-	-	EVENT OUT
	PG4	-	-	TIM20_BKIN2	-	I2C4_ SDA	SPI1_MOSI	-	-	-	-	-	-	FMC_A14	-	-	EVENT OUT
	PG5	-	-	TIM20_ETR	-	-	SPI1_NSS	-	-	LPUART1_ CTS	-	-	-	FMC_A15	-	-	EVENT OUT
	PG6	-	-	TIM20_BKIN	-	I2C3_ SMBA	-	-	-	LPUART1_ RTS_DE	-	-	-	FMC_INT	-	-	EVENT OUT
	PG7	-	-	-	SAI_CK1	I2C3_ SCL	-	-	-	LPUART1_ TX	-	-	-	FMC_INT	SAI_MCLK_A	-	EVENT OUT
	PG8	-	-	-	-	I2C3_ SDA	-	-	-	LPUART1_ RX	-	-	-	FMC_NE3	-	-	EVENT OUT
	PG9	-	-	-	-	-	-	SPI3_SCK	USART1_TX	-	-	-	-	FMC_NCE/FMC_NE2	-	TIM15_CH1N	EVENT OUT
	PG10	MCO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

5 Ordering information

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, contact the nearest ST sales office.

Table 12. Ordering information

Example: STM32 G 484 V E T 6 x

Device family

STM32 = Arm-based 32-bit microcontroller

Product type

G = General-purpose

Sub-family

484 = STM32G484xx

Pin count

C = 48 pins
R = 64 pins
V = 100 pins
W = 128 pins

Code size

B = 128 Kbyte
C = 256 Kbyte
E = 512 Kbyte

Package

H = TFBGA
T = LQFP
U = UFQFPN
Y = WLCSP

Temperature range

6 = Industrial temperature range, - 40 to 85 °C (105 °C junction)
7 = Industrial temperature range, - 40 to 105 °C (125 °C junction)
3 = Industrial temperature range, - 40 to 125 °C (130 °C junction)

Options

xxx = programmed parts
TR = tape and reel

6 Revision history

Table 13. Document revision history

Date	Revision	Changes
DD-Dec-2017	0.1	Initial release.