C17 Power Analysis and Optimization

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Problem description:

We have a C17 Benchmark circuit and we have to perform its power optimization

Given Input Parameters:

Following are the parameters already provided to us for the designing:

- Vdd = 3V
- Kp = 20u
- Vto = +/- 0.5V
- W = 1.3u & 1.1u (both)
- L= 0.13u (both)
- Probability=0.5
- Cl= 1pF
- Input Supplies:
  - Tr=Tf=10ns
  - Period= 50ns => f= 200MHz
  - Pulse Width = 25ns

1. Input assumed 00101

Part-A: Before Optimization

1. Dynamic Power

Transition Probabilities for NAND: PAPB x (1 -PAPB)

Gate1= 0.1875=> Pd=337.5uW

Gate2= 0.1875=> Pd=337.5uW

Gate3=0.085=> Pd=153.0uW

Gate4=0.085=> Pd=153.0uW

Gate5=0.0072=> Pd=12.96uW

Gate6=0.0407=> Pd=73.26uW

Total Dynamic Power=1.06722mW

As per Simulation:

Gate1 =75uW

Gate2 =-

Gate3=336.960uW

Gate4=336.960uW

Gate5= 12.96uW

Gate6=73.26uW

In simulation, found the highest and lowest peak of current and power through each gate separately

Main parameter: Current through load capacitance

Gate	Highest Peak Current (A)	Lowest Peak Current(A)	Highest Peak Power (W)	Lowest Peak Power (W)
1	1.2500m	-312.500u	3750u	-937.5u
2	30.923p	-29.104p	92.769p	-87.312p
3	1.8750m	-937.500u	5.625m	-2812.5u
4	625.000u	-312.500u	1875u	-937.5u

5	**583.949u**	**-281.266u**	1751.847u	-843.798u
6	**5.4570p**	**-5.4570p**	16.371p	-16.371p

2. Static Power

3. Here, I will increase the transition timing to for proper evaluation to 5ns each
4. Main Parameter: current through upper NMOS – current through load cap

Gate	Highest Peak Current (A)	Lowest Peak Current(A)	Highest Peak Power (W)	Lowest Peak Power (W)
1	**625.041u**	**-993.776u**	1875.123u	-2981.33u
2	**312.792u**	**-110.408p**	938.376u	-331.224p
3	**625.041u**	**-612.759u**	1875.123u	-1838.28u
4	**625.041u**	**-612.759u**	1875.123u	-1838.28u
5	**562.531u**	**-582.491u**	1687.593uu	-1747.47
6	**312.729u**	**1.5100p**	938.187u	4.53p

5.

6. Leakage Power: 36.150pW

7. Delay at Output1

Instead of calculating for all gate individually, we can directly check the output, the voltage swing will be a cumulative delay

Gate	Rise time	Fall time
5	**8.4084n**	**8.7945n**

8. Part-B: After Optimization

Optimization: I have used 'Gate Sizing' and change W to 1.1microns

1. Dynamic Power

Main Parameter: current through load capacitance

Gate	Highest Peak Current (A)	Lowest Peak Current(A)	Highest Peak Power (W)	Lowest Peak Power (W)
1	**1.0577m**	**-264.423u**	3.1731m	-793.269u
2	**3.2596n**	**-116.415p**	9.7788n	-349.245p
3	**528.847u**	**-264.423u**	1586.541u	-793.269u
4	**528.846u**	**-264.423u**	1586.538u	-793.269u
5	**491.140u**	**-238.004u**	1473.42u	-714.012u
6	**698.492p**	**-465.661p**	2095.476p	-1396.98p

2. Static Power

Here, I will increase the transition timing to for proper evaluation to 5ns each

Main Parameter: current through upper NMOS – current through load cap

Gate	Highest Peak Current (A)	Lowest Peak Current(A)	Highest Peak Power (W)	Lowest Peak Power (W)
1	**528.881u**	**-912.940u**	1586.643u	-2738.82u
2	**264.670u**	**-57.670p**	794.01u	-173.01p
3	**528.881u**	**-524.691u**	1586.643u	-1574.07u
4	**528.881u**	**-524.691u**	1586.643u	-1574.07u
5	**475.831u**	**-491.691u**	1427.493u	-1475.07u
6	**264.652u**	**1.5100p**	793.956u	4.53p

3. **Leakage Power: 36.150pW (No significant diff)**
4. **Delay at Output1**
   Instead of calculating for all gate individually, we can directly check the output, the voltage swing will be a cumulative delay

Gate	Rise time	Fall time
5	**9.790n**	**10.195n**

Comparison

Dynamic

Gate	*Highest Peak*			*Lowest Peak*		
	W=1.3u	***W=1.1u***	***%diff***	***W=1.3u***	***W=1.1u***	***%diff***
1	3750u	3.1731m	15.384	-937.5u	-793.269u	15.38464
2	92.769p	9.7788n	-5.41021	-87.312p	-349.245p	-299.997
3	5.625m	1586.541u	71.79483	-2812.5u	-793.269u	71.79488
4	1875u	1586.538u	91.53846	-937.5u	-793.269u	15.38464
5	1751.847u	1473.42u	15.89334	-843.798u	-714.012u	15.38117
6	16.371p	2095.476p	-12699.9	-937.5u	-1396.98p	0.490112

Short circuit

Gate	*Highest Peak*			*Lowest Peak*		
	W=1.3u	***W=1.1u***	***%diff***	***W=1.3u***	***W=1.1u***	***%diff***
1	1875.123u	1875.123u	0	-2981.33u	-2738.82u	18.134289

2	938.376u	-2738.82u	-191.868	-331.224p	-173.01p	14.776647
3	1875.123u	-173.01p	9.077341	-1838.28u	-1574.07u	14.37267
4	1875.123u	-1574.07u	16.05511	-1838.28u	-1574.07u	14.37267
5	1687.593uu	-1574.07u	6.726918	-1747.47	-1475.07u	15.58825
6	938.187u	-1475.07u	15.572256	4.53p	4.53p	0

DELAY

Gate	***TpLH***			***TpHL***		
	W=1.3u	***W=1.1u***	***%diff***	***W=1.3u***	***W=1.1u***	***%diff***
5	**8.4084n**	**9.790n**	13.816	**8.7945n**	**10.195n**	14.005

CONCLUSION;

- **Staying in the timing limit of 1.5 times, the power was reduced**
- **Reduction of 15% in W leads to 15% reduction in power**

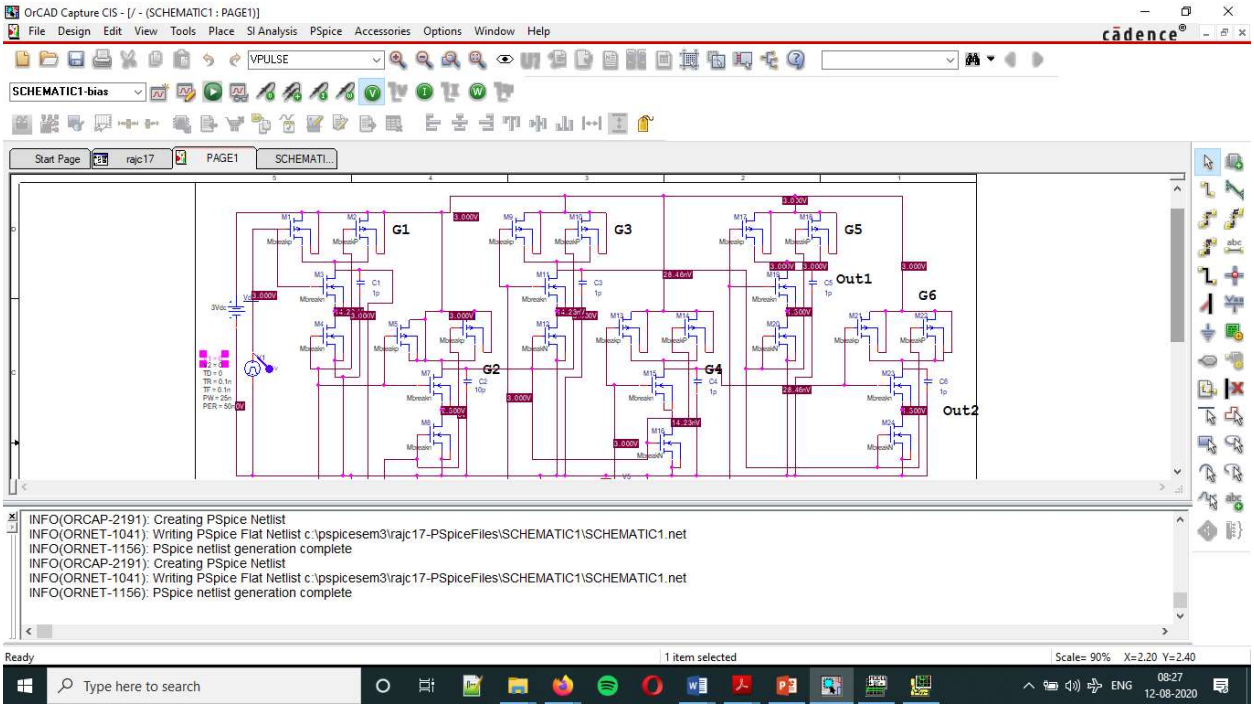

Fig1 - Schematic

Fig-2 – Delay after Optimmization