Inverter Chain Sizing and Layout

Submitted by:

Rajnish Tailor 110006068

Guidance of:

Dr. Chunhong Chen

(Professor)

and

Michael Zhan

(G.A.)

University of Windsor

DIGITAL INTEGRATED CIRCUIT DESIGN

(ELEC4330-91-R-2020S)

Faculty of Engineering University of Windsor, Canada

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Problem description:

In this project, the task is to design an inverter chain/buffer system which can drive a load capacitance of 20pF. In this the challenge will be to determine the input capacitance of the CMOS inverter and design the remaining stages accordingly. We have two have two different stage values N= 3 and N=5 for the chain. Both of then give different amount of propogation delay. Also, following this we have to find the optimal value of N. Lastly, design the 3-Sage inverter chain on the VLSI MAGIC tool.

Given Input Parameters:

Following are the parameters already provided to us for the designing:

Input gate capacitance = 10fF Load capacitance C_L = 20pF,

Intrinsic delay t_{po} = 70ps

Part-A: Two Stage Buffer (N=3 inverter chain)

Procedure:

- For the initial CMOS inverter design we have the intrinsic delay must be set to 70ps by designing a CMOS inverter circuit without any load capacitance C_L as shown in Figure-1 with NMOS transistor parameters: kp = 10u, tox = 2n, W = 1u, and L = 0.25u and PMOS transistor parameters: kp = 3u, tox = 2n, W = 3u, and L = 0.25u.

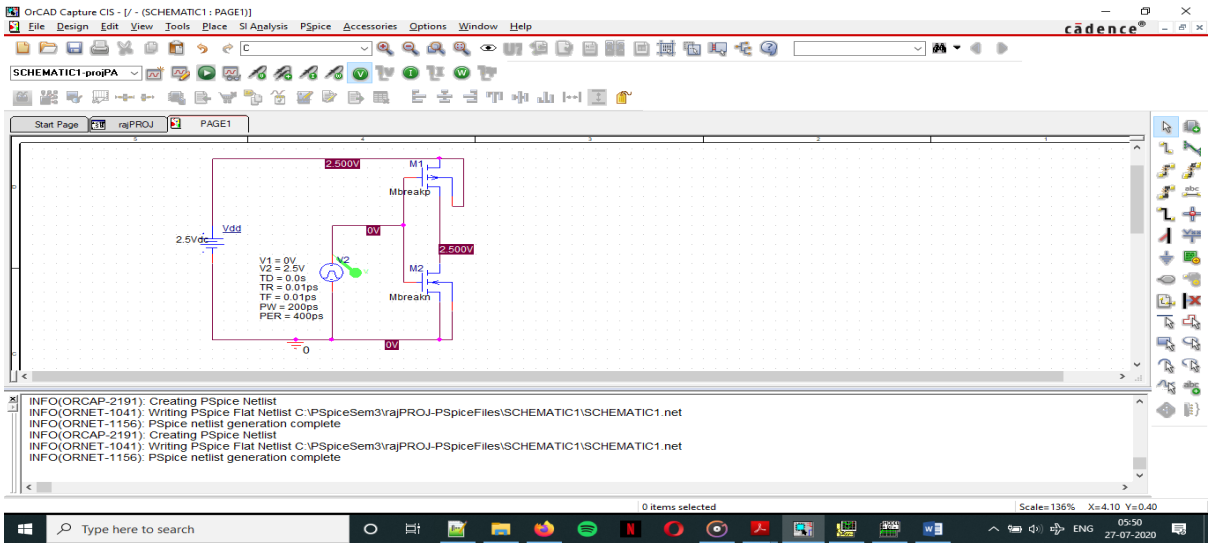


Figure – A.1a

- The input pulse has parameters like V1=0V, V2=2.5V, TR=TF=0.01ps, PW=200ps and PER=400ps. And supply voltage V_{dd} =2.5V. The circuit is set to transient analysis and simulated with run time as 400ps with a maximum step time of 1ps. The task in hand is to adjust the K_p and /or t_{ox} value to get the average t_p ps which is dame as out intrinsic delay.

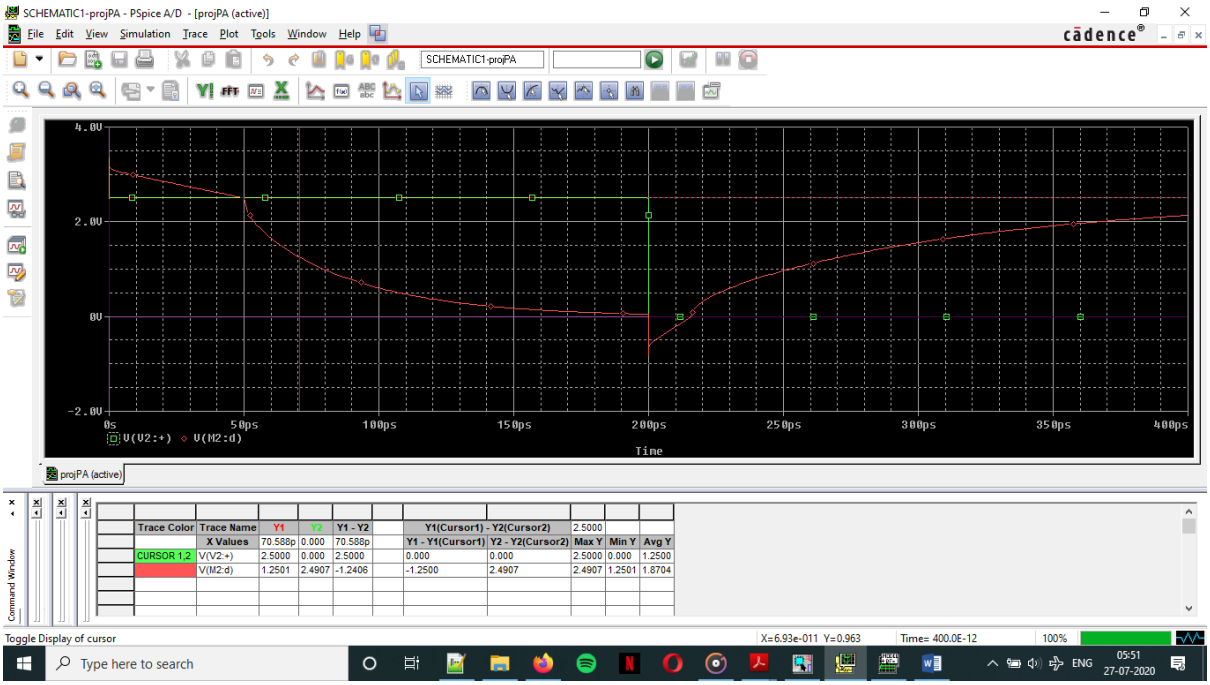


Figure – A.1b

- In the above figure I have adjusted the value of K_p (didn't need to change t_{ox})

  Average t_{p0} = 70.2615ps; t_{pLH} = 69.935ps; t_{pHL} = 70.588ps

  For PMOS: kp = 2.86µ and tox = 2n

  For NMOS: kp = 8µ and tox = 2n

- Now we need to make 2 different irrcuits,
  - The one we have already prepared with propagation delay 70ps, we simply add a load capacitance of 10fF to it.
  - One more circuit with additional inverter to it (2 inverter cascaded).

  Now we compare the output in of the single inverter circuit (mentioned a) and the intermediate voltage between the 2 inverter circuit (mentioned b)

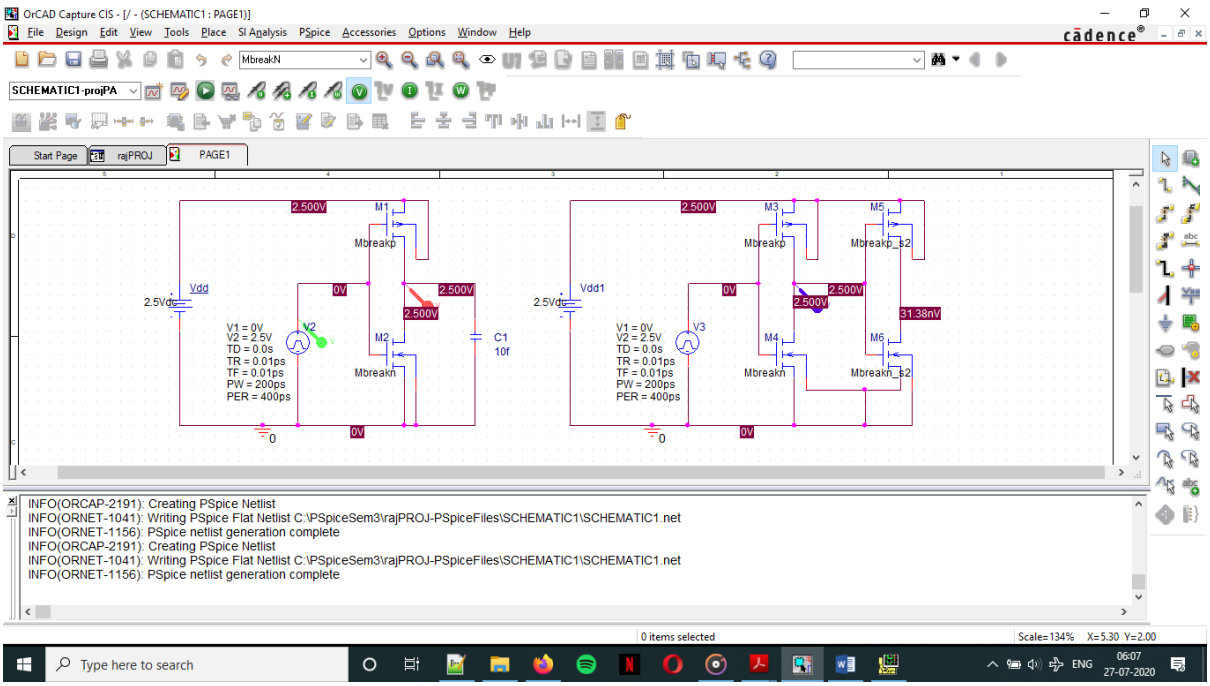


Figure – A.2a

- Below is the graph plot of the vout1, vout2 and the difference between the two

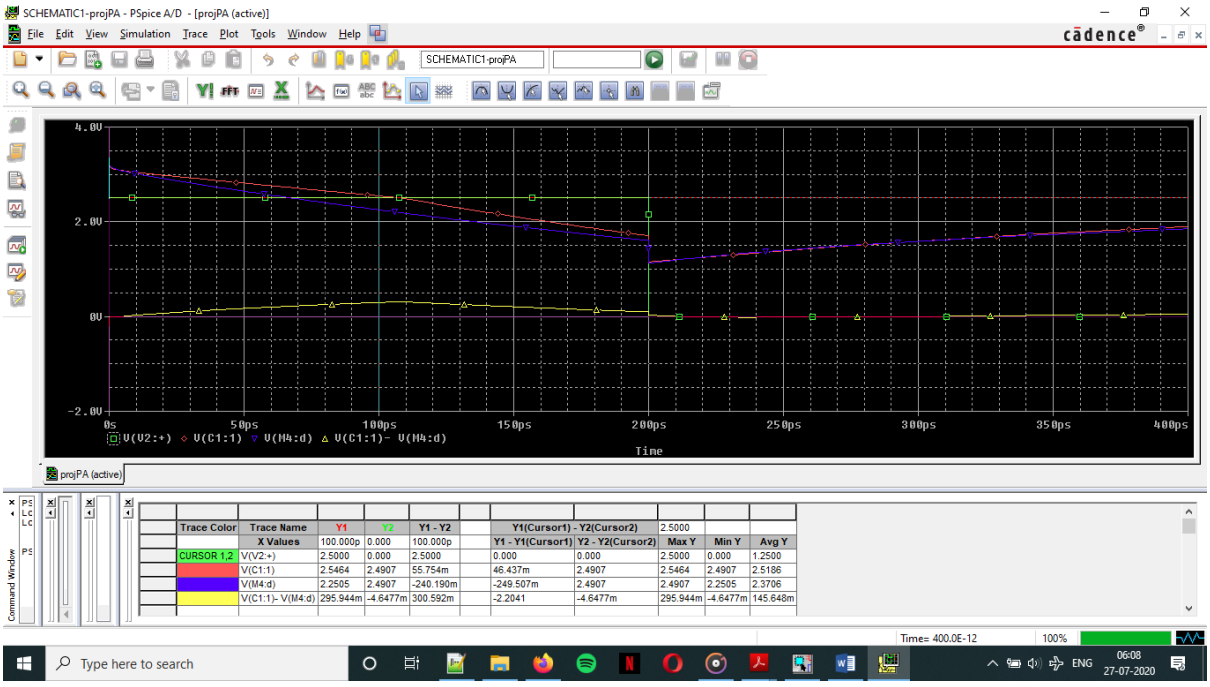


Figure – A.2b

- Furthermore, we are asked to adjust value of W in transistor M3 and M4 in order to get least to no difference, but keeping the sizing factor same

- V_{out1} = 0.28ns
- V_{out2} = 0.3ns

As the values are close by I do not need to adjust my W values and the sizing factor for me is S = 1.

- This what we have obtained are the final sizes of the transistor. Ahead of this we need to design a 3 inverter chain circuit and attach a load capacitance of 20pF to it and check on its output. Along with this we also need to theoretically find out the output delay of a 3 stage inverter chain,

  As per the calculations and given ; f=12.599, L=0.25 µm

  For stage 1(unit size inverter):

  PMOS, W = 3µm

  NMOS, W = 1µm

  For stage 2:

  PMOS, W = 3µ*12.599 = 37.797µm

  NMOS, W = 1µ*12.599 = 12.599µm

  For stage 3:

  PMOS, W = $3\mu*12.599^2$= 476.204µm

  NMOS, W = $1\mu*12.599^2$ = 158.73µm

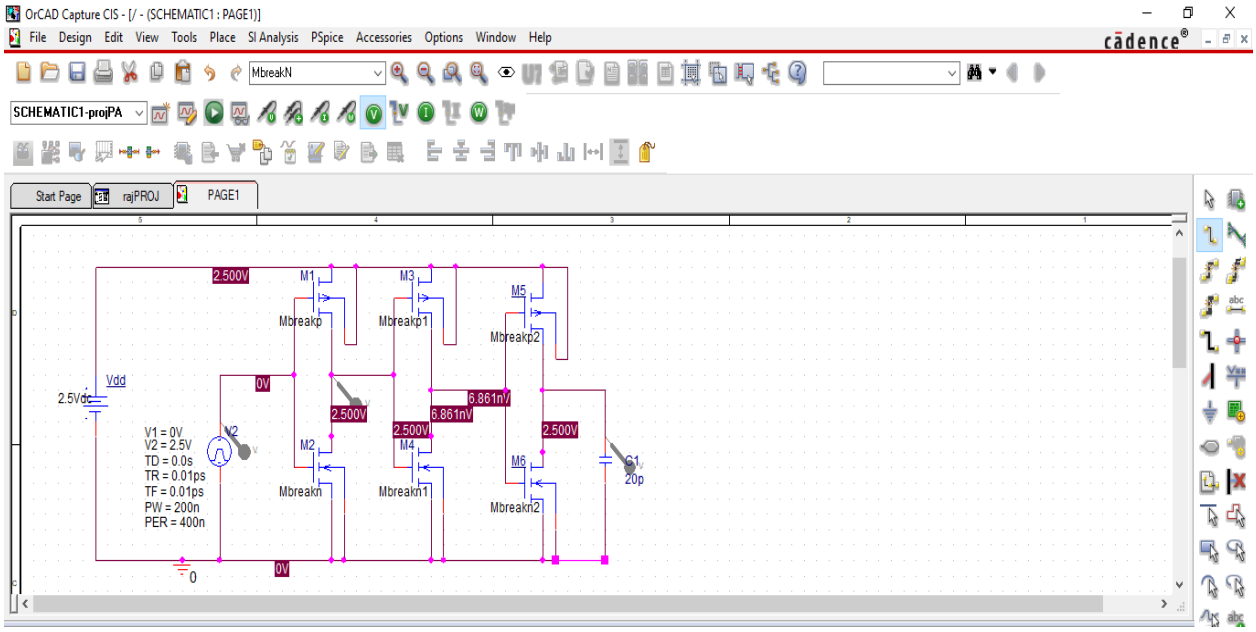


Figure-A.3a

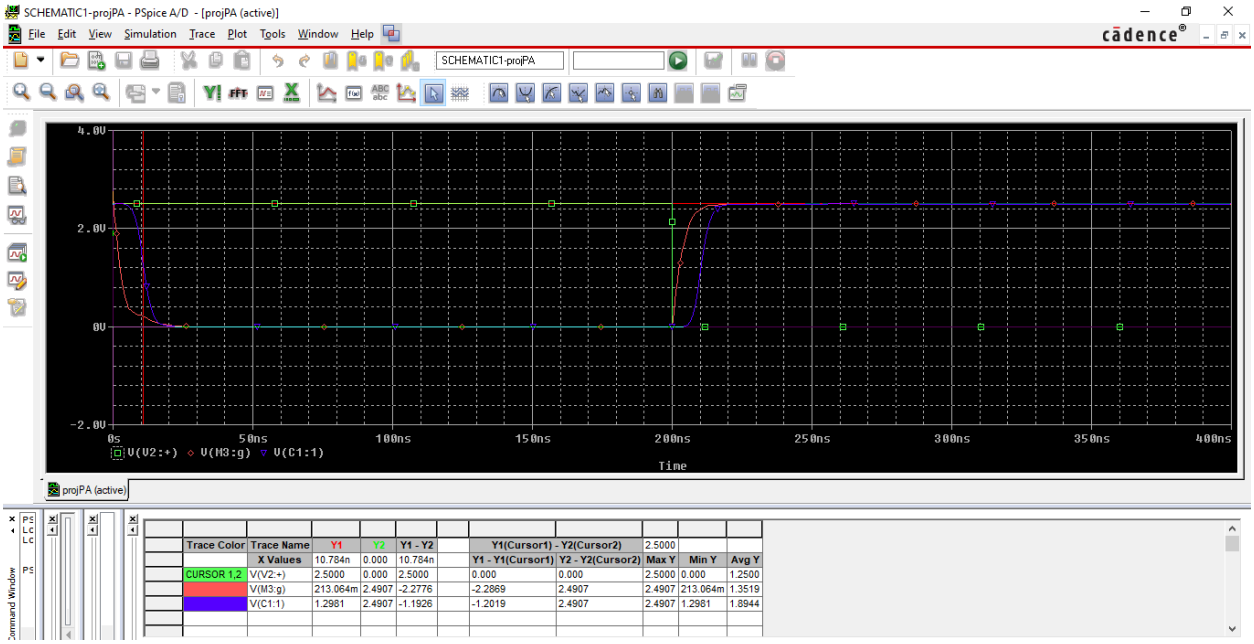


Figure-A.3b

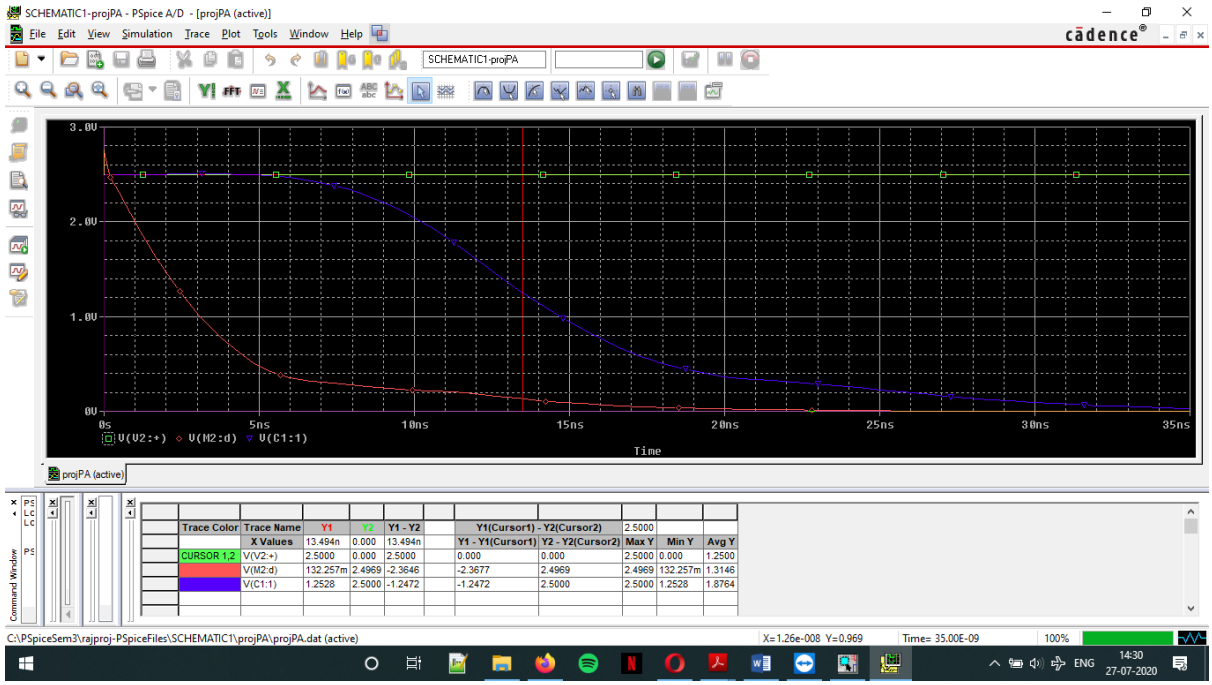


Figure – A.3c

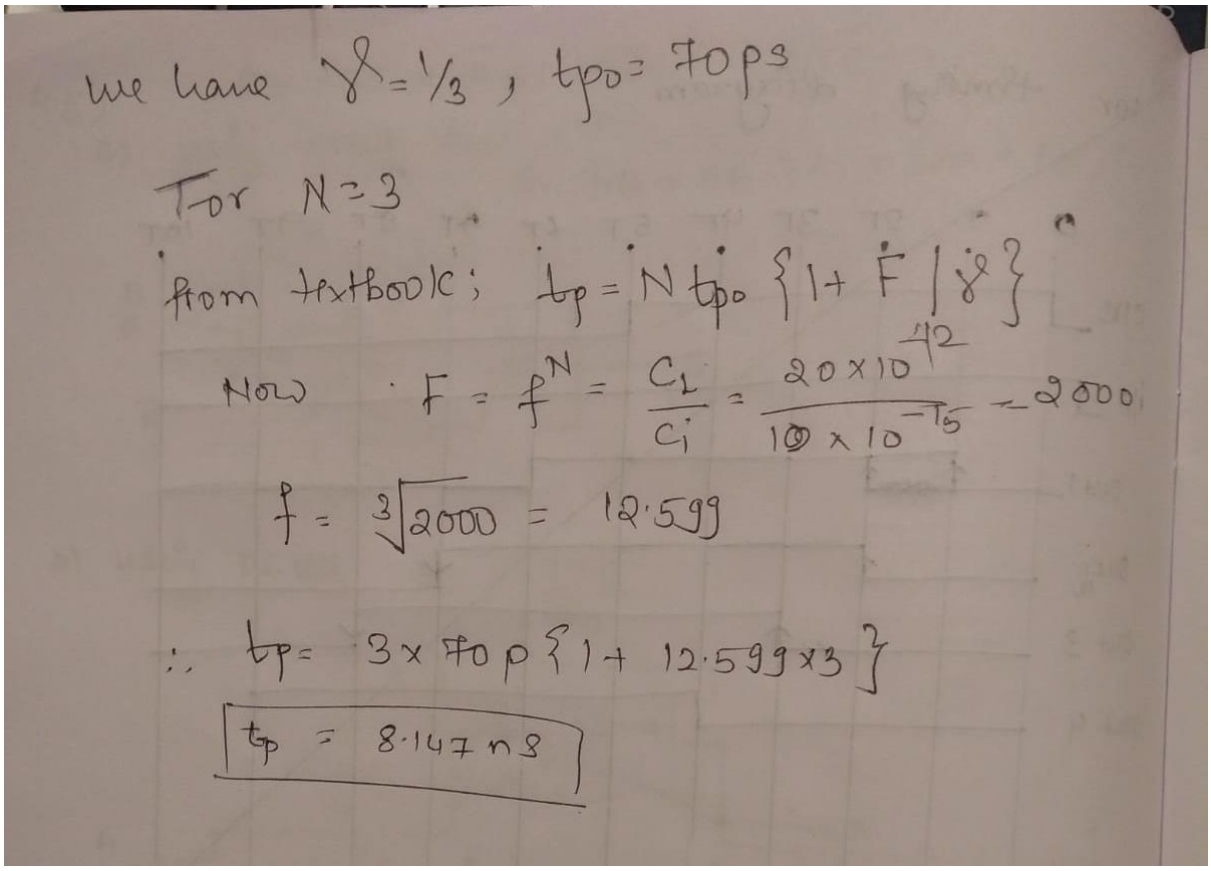


Figure – A.3d

- In the above images we can see that the for N=3
  - Experimental Delay; Tp = 10.835ns
  - Theoretical Delay; Tp= 8.147ns

Part-B: 4 Stage Buffer (N=5 inverter chain)

Procedure:

- Similar to Part a, we perform similar steps to find the theoretical delay and experimental delay of a 5 stage inverter chain.

As per the calculations and given ; f=4.573, L=0.25 µm

For stage 1(unit size inverter):

PMOS, W = 3µm

NMOS, W = 1µm

For stage 2:

PMOS, W = 3µ*4.573 =13.719µm

NMOS, W = 1µ*4.573 = 4.573µm

For stage 3:

PMOS, W = $3\mu*4.57^2$ = 62.737µm

NMOS, W = $1\mu*4.57^2$= 20.912µm

For stage 4:

PMOS, W = $3\mu*(4.57)^3$ = 286.896µm

NMOS, W = $1\mu*(4.57)^3$ = 95.632µm

For stage 5:

PMOS, W = $3\mu*(4.57)^4$ = 1311.977µm

NMOS, W = $1\mu*(4.57)^4$ = 437.326µm

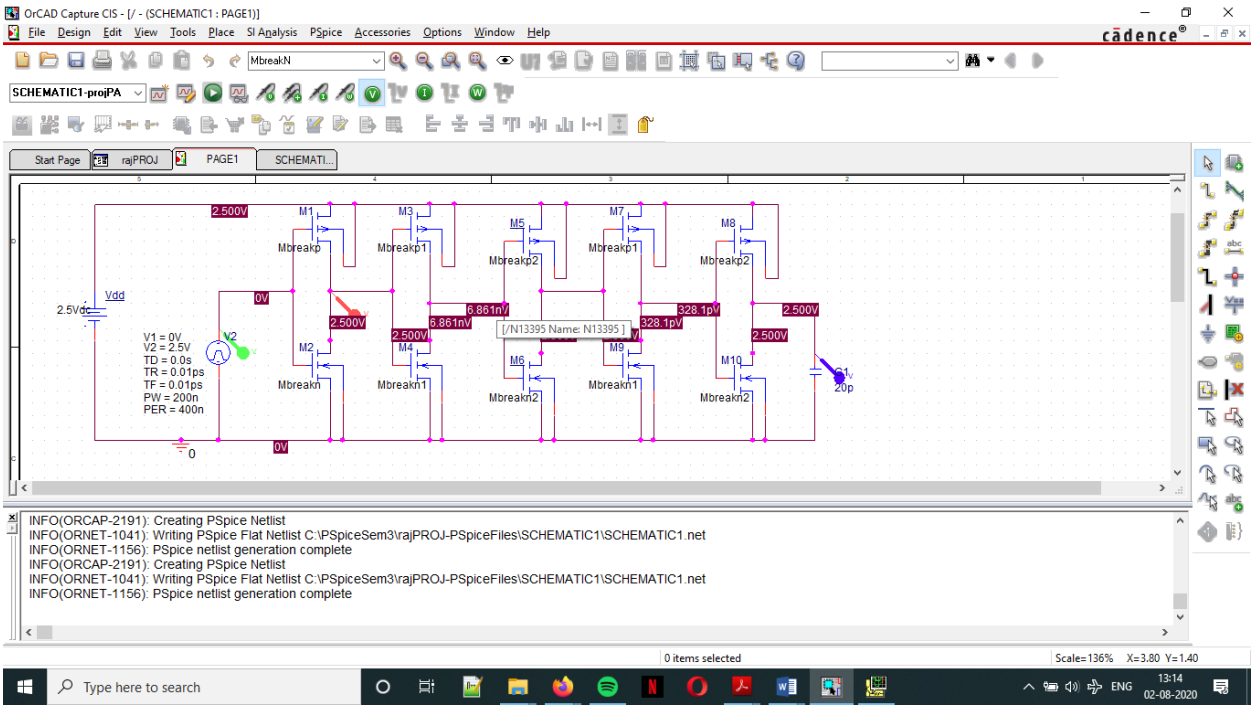


Figure-B.1a

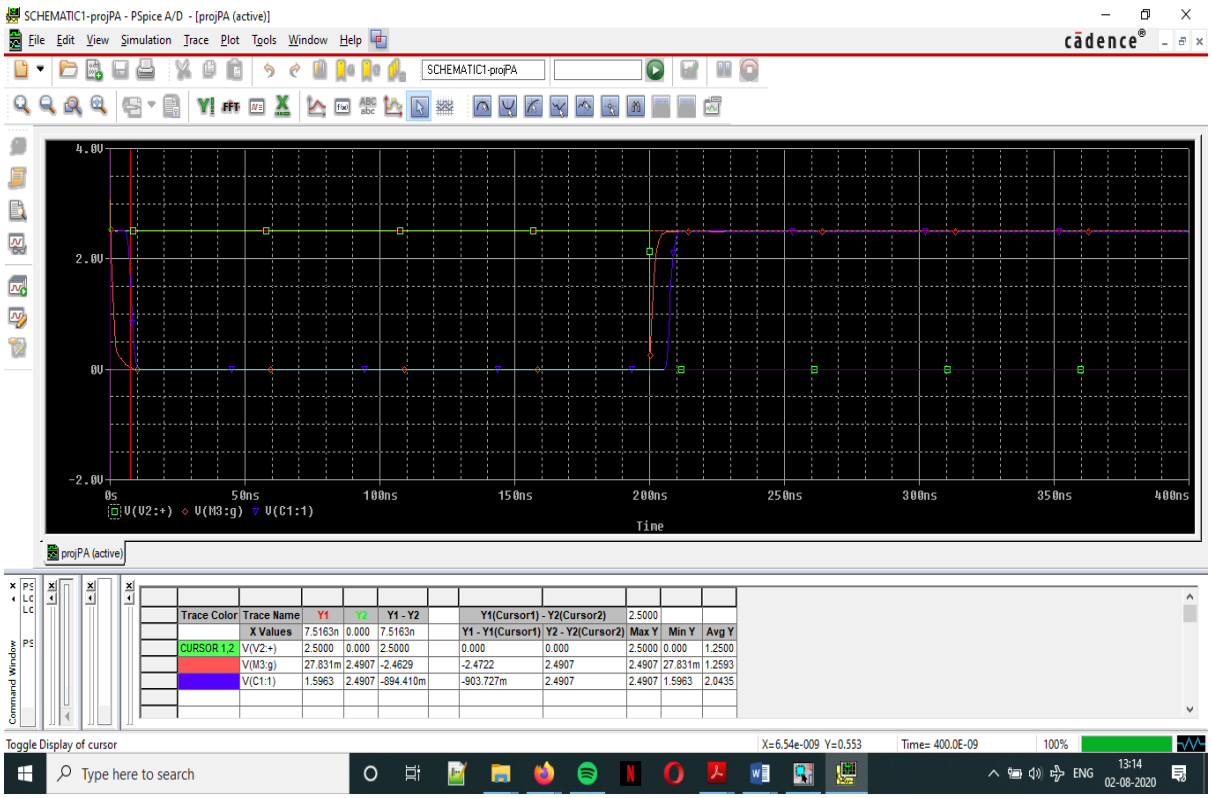


Figure-B.1b

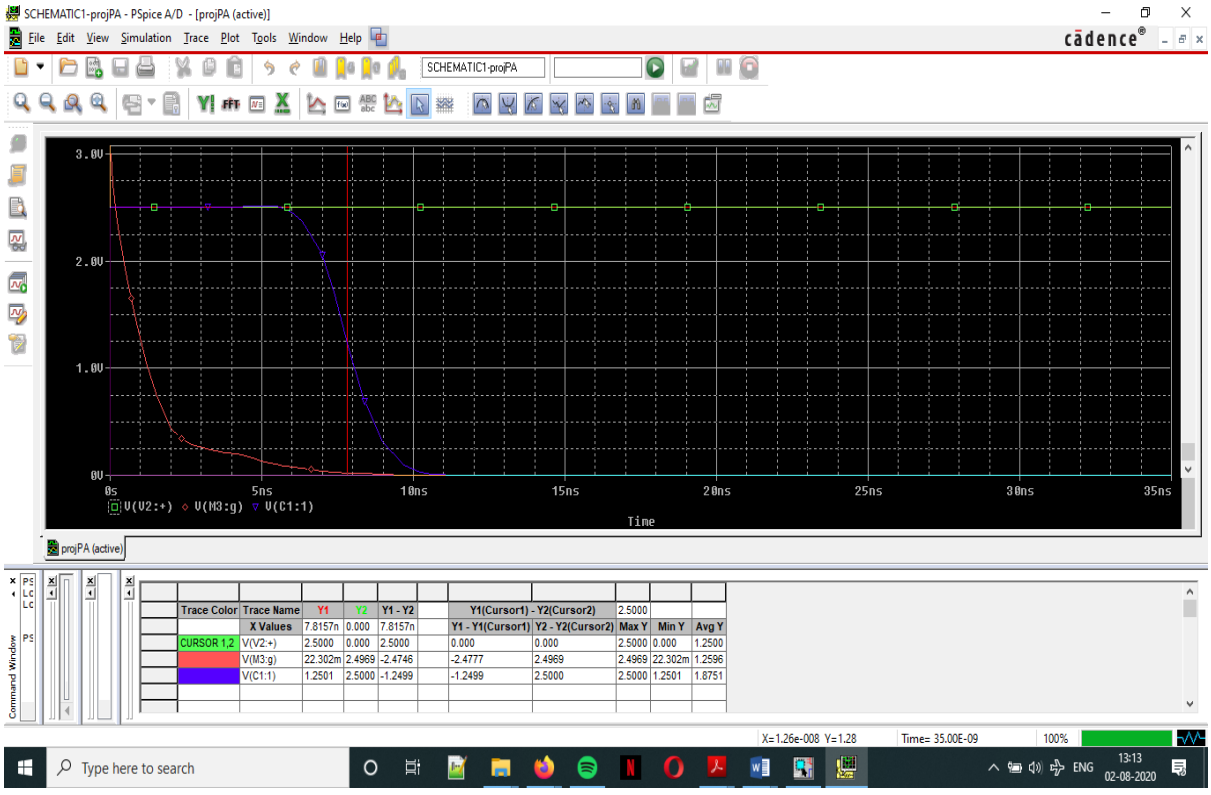


Figure-B.1c

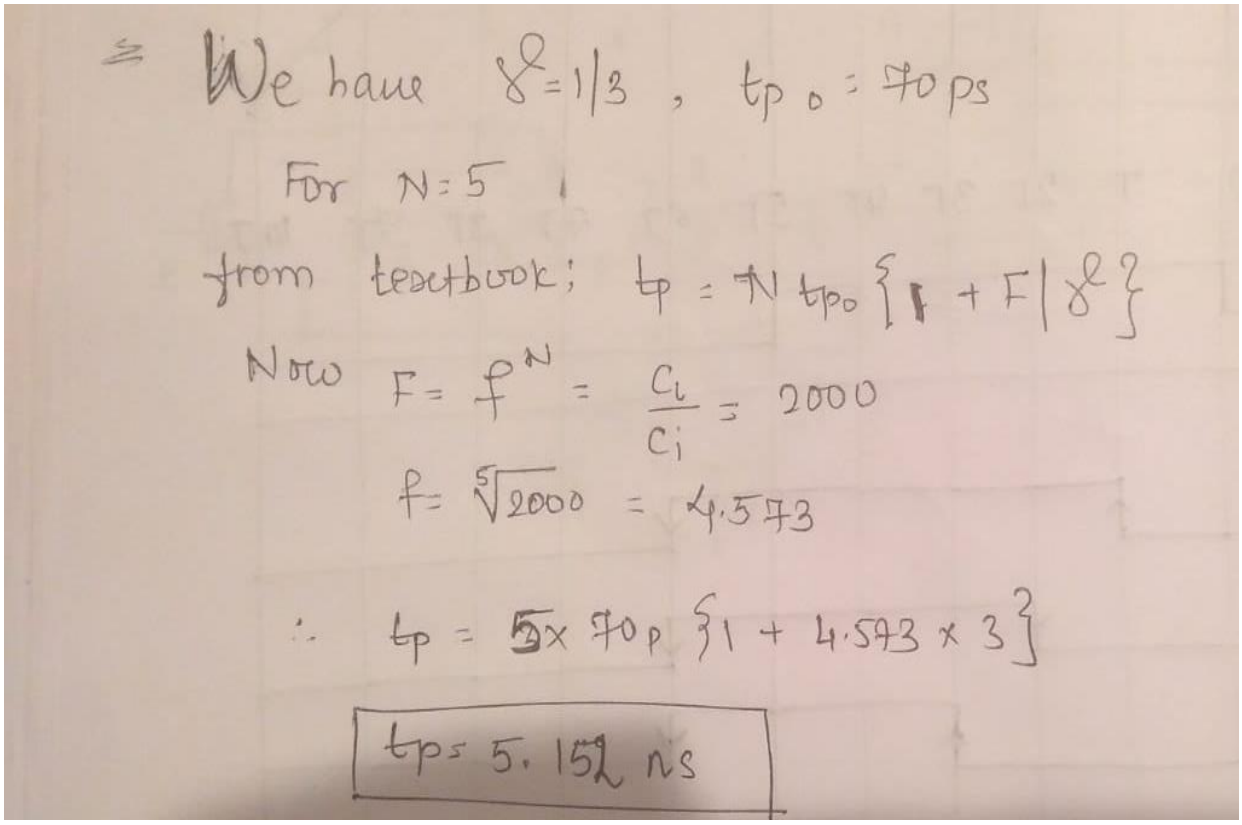


Figure-B.1d

- In the above images we can see that the for N=5
  - Experimental Delay; Tp = 7.8157ns
  - Theoretical Delay; Tp= 5.152ns

Optimum Number of stages

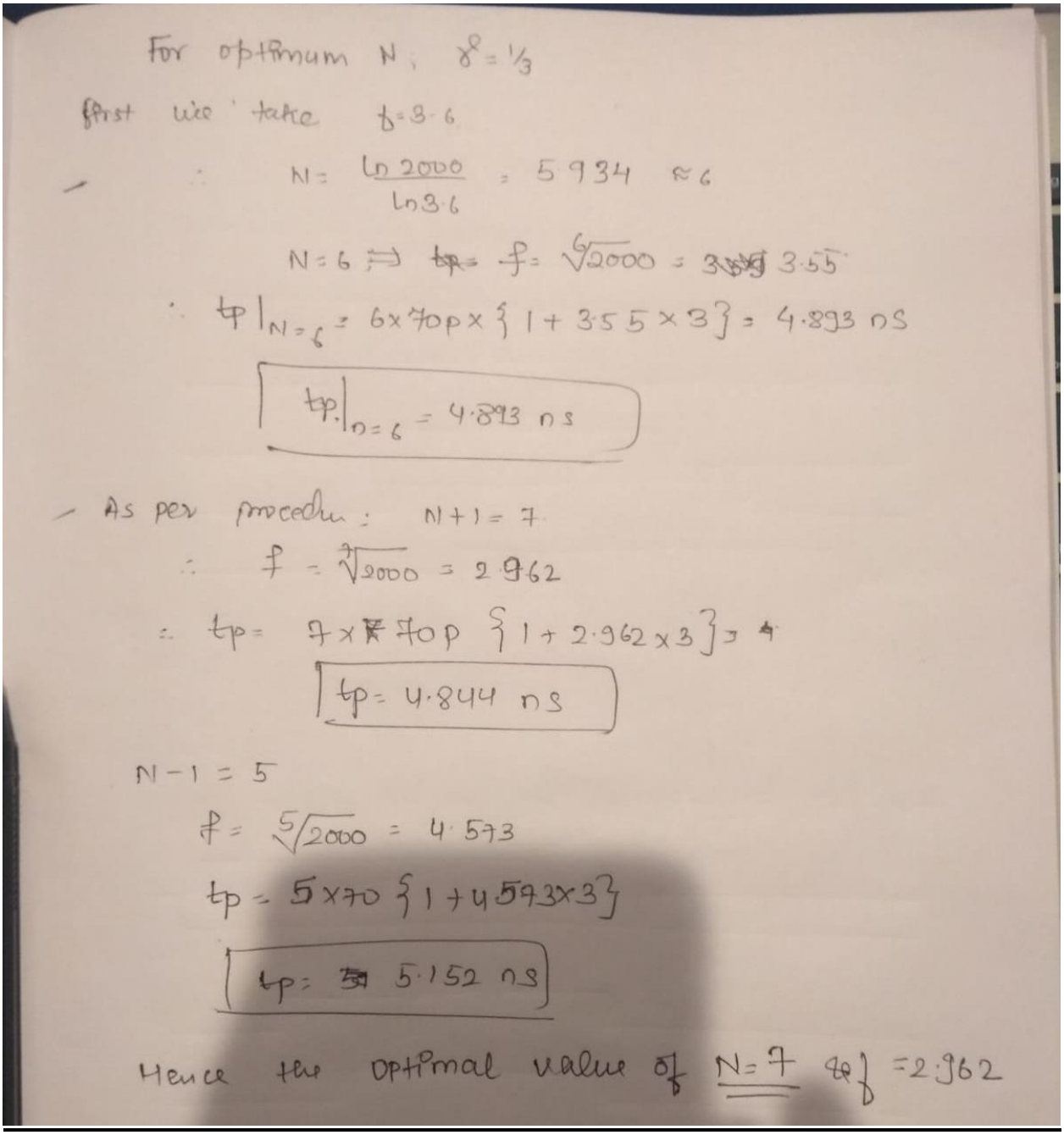


Figure-B.2a

- As the final N and f are 7 and 2.962 respectively, we form a seven stage inverter chain to minimize our delay

  As per the calculations and given ; f=42.962, L=0.25 µm

For stage 1(unit size inverter):

PMOS, W = 3μm

NMOS, W = 1μm

For stage 2:

PMOS, W = 3μ*2.962 = 8.886μm

NMOS, W = 1μ*2.962 = 2.962μm

For stage 3:

PMOS, W = $3\mu*2.962^2$ = 26.320μm

NMOS, W = $1\mu*2.962^2$ = 8.773μm

For stage 4:

PMOS, W = $3\mu*(2.962)^3$ = 77.961μm

NMOS, W = $1\mu*(2.962)^3$ = 25.987μm

For stage 5:

PMOS, W = $3\mu*(2.962)^4$ = 230.92μm

NMOS, W = $1\mu*(2.962)^4$ = 76.973μm

For stage 6:

PMOS, W = $3\mu*(2.962)^5$ = 683.985μm

NMOS, W = $1\mu*(2.962)^5$ = 227.995μm

For stage 7:

PMOS, W = $3\mu*(2.962)^6$ = 2025.963μm

NMOS, W = $1\mu*(2.962)^6$ = 675.321μm

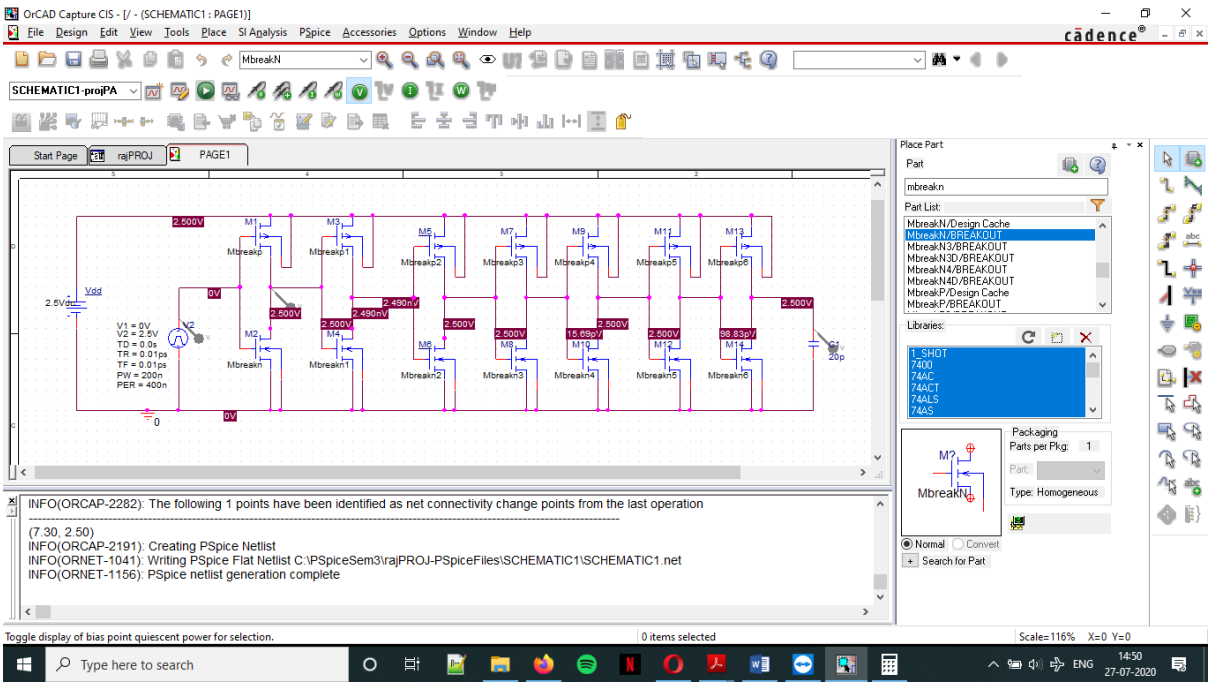


Figure-B.2b

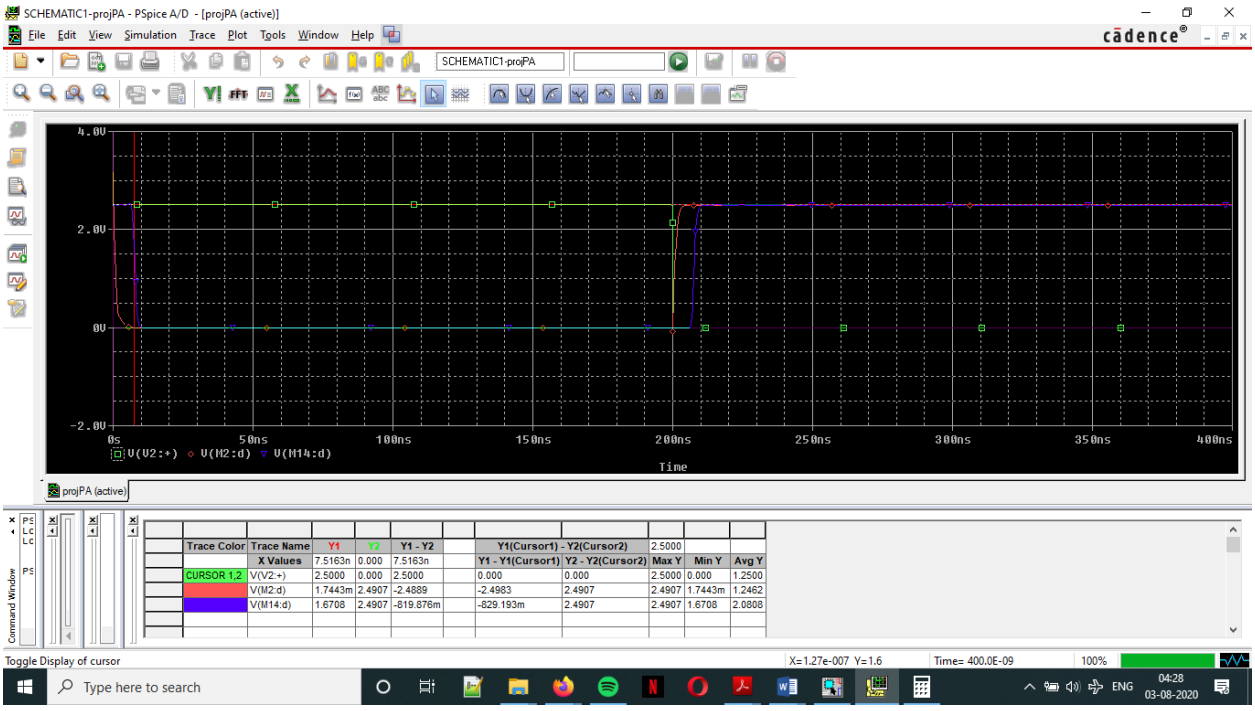


Figure- B.2c

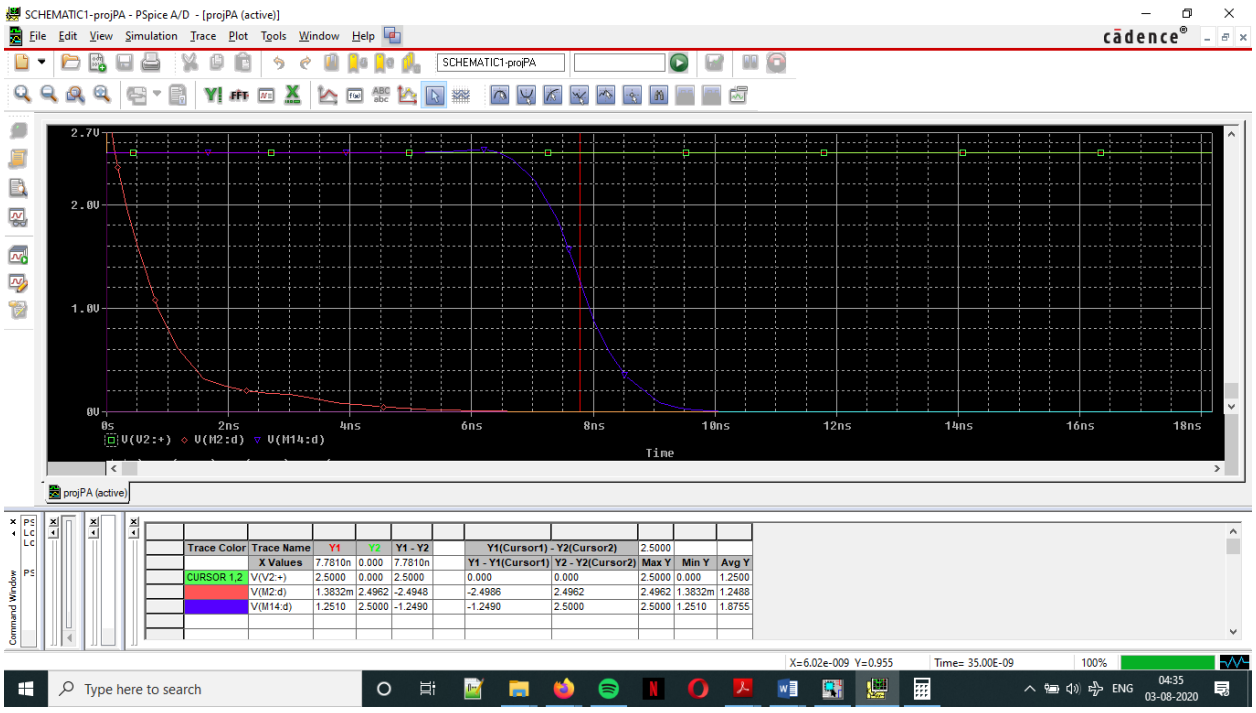


Figure -B.2d

- In the above images we can see that the for N=5
  - Experimental Delay; Tp = 7.7810ns
  - Theoretical Delay; Tp= 4.844ns

Part-C: MAGIC Layout Design (N=3 inverter chain)

Here we have to draw a 3 stage inverter chain corresponding to our values optained in the PSpice. We will be using a tool called MAGIC for this.

For the demonstration purposes the transistor sizes are scaled down to few number of grid boxed, but the below image shows you the actual number of boxes required by on PMOS and NMOS transistor.

Technology: scmos

L=0.25um => Lambda=0.125um

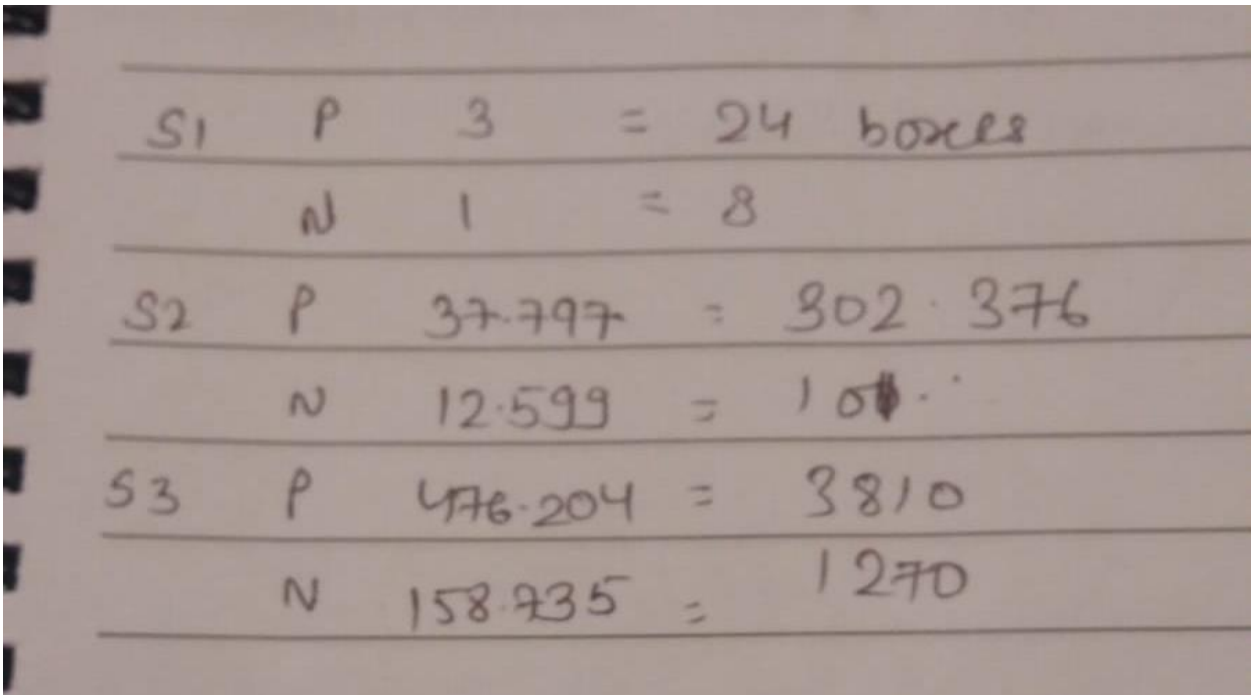
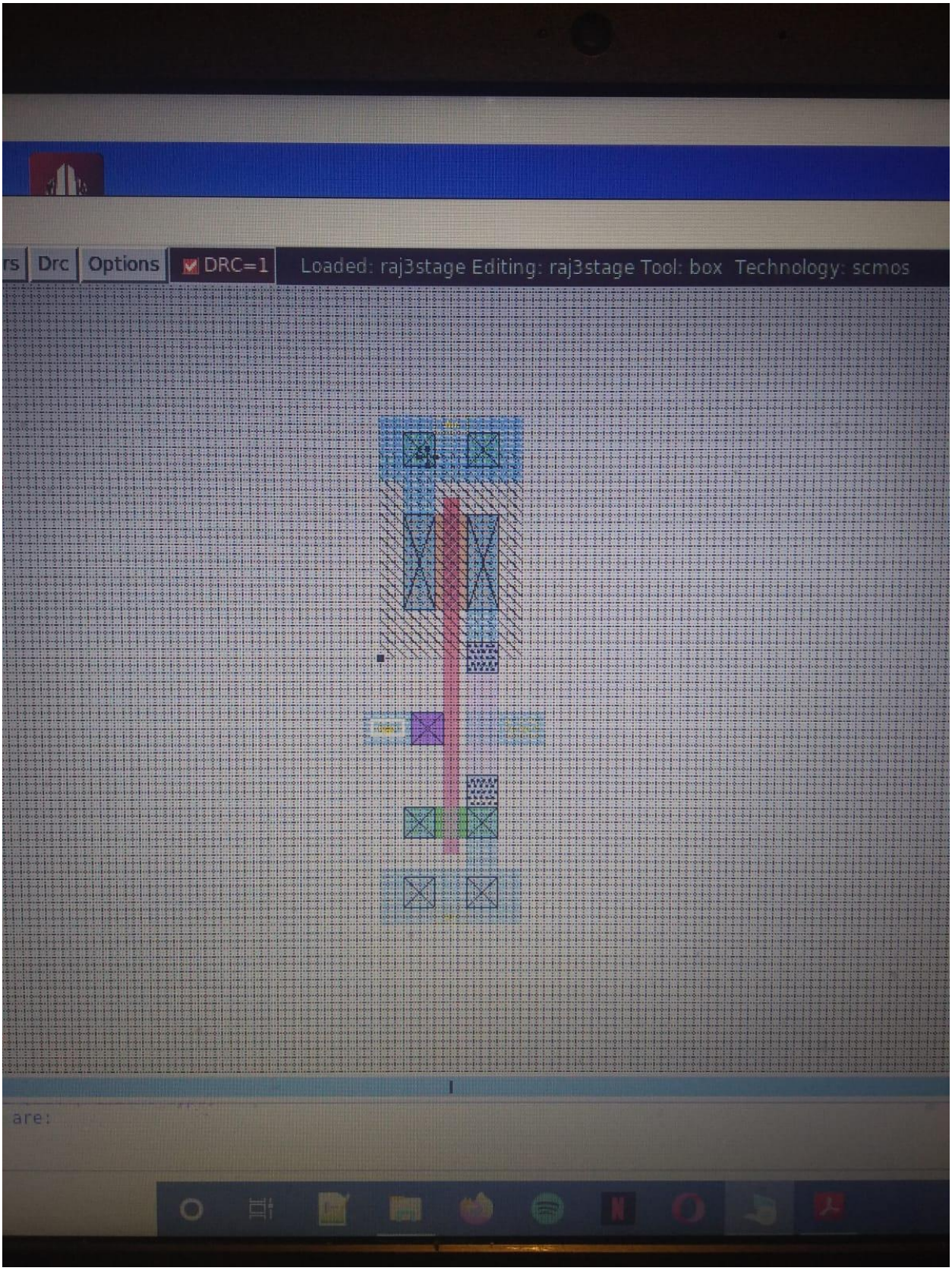


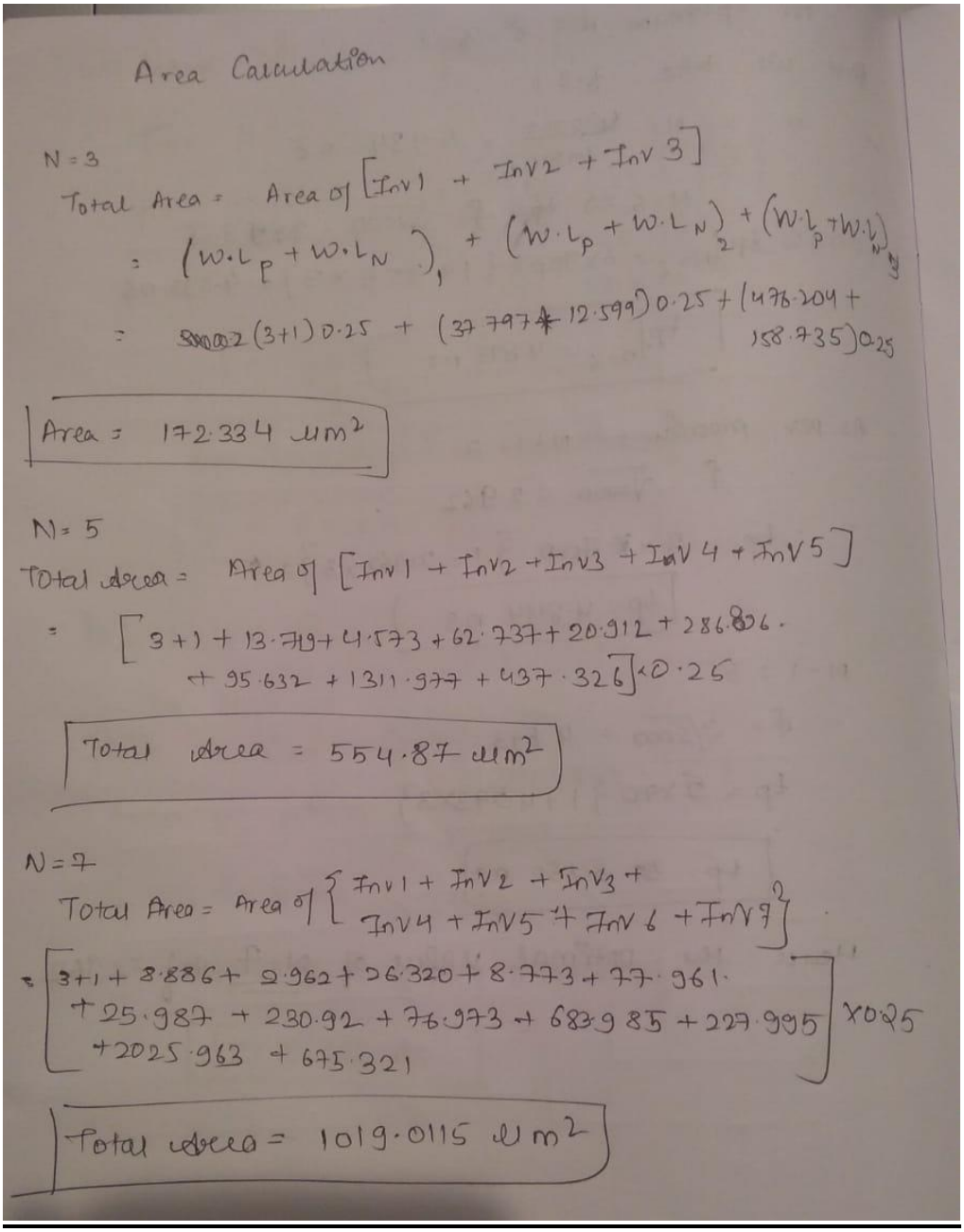
Figure-C.1

Below is the layout in MAGIC


rs
Drc
Options
DRC=1
Loaded: raj3stage Editing: raj3stage Tool: box Technology: scmos
are:

Conclusions:

- The Area calculations



Area Calculation

N = 3

Total Area = Area of [Inv1 + InV2 + InV3]

= $(W \cdot L_P + W \cdot L_N)_1 + (W \cdot L_P + W \cdot L_N)_2 + (W \cdot L_P + W \cdot L_N)_3$

= 2 (3+1) 0.25 + (37.797 + 12.599) 0.25 + (478.204 + 158.735) 0.25

Area = 172.334 μm^2

N = 5

Total area = Area of [Inv1 + InV2 + InV3 + InV4 + InV5]

= [3+1 + 13.719 + 4.573 + 62.737 + 20.912 + 286.806 + 95.632 + 1311.977 + 437.326] × 0.25

Total area = 554.87 μm^2

N = 7

Total Area = Area of {Inv1 + InV2 + InV3 + InV4 + InV5 + InV6 + InV7}

= [3+1 + 8.886 + 2.962 + 26.320 + 8.773 + 77.961 + 25.987 + 230.92 + 76.973 + 683.985 + 227.995 + 2025.963 + 675.321] × 0.25

Total area = 1019.0115 μm^2

- We can clearly see above that the area occupied increases with the increase in transistor sizes as well as number (in chain).
- Along with this delays for
    - N=3: 10.835ns
    - N=5: 7.8157ns
    - N=7: 7.7810ns

  So, it is clear that as the N increased the total propagation delay decreased. For the optimum value ,7 we have the least delay.

- **Yes, the theoretical values and experimental values have a difference, but that is because theory is an ideal scenario, whereas in experimental scene there are diffusion capacitances between two inverters and other reasons where the input itself get delayed resulting into delay in output too**

- It is also clear that if we want to reduce the delay, we need to compensate over the area used. For N=3 area is least and delay is maximum, while for N=7 area is max and the delay is least