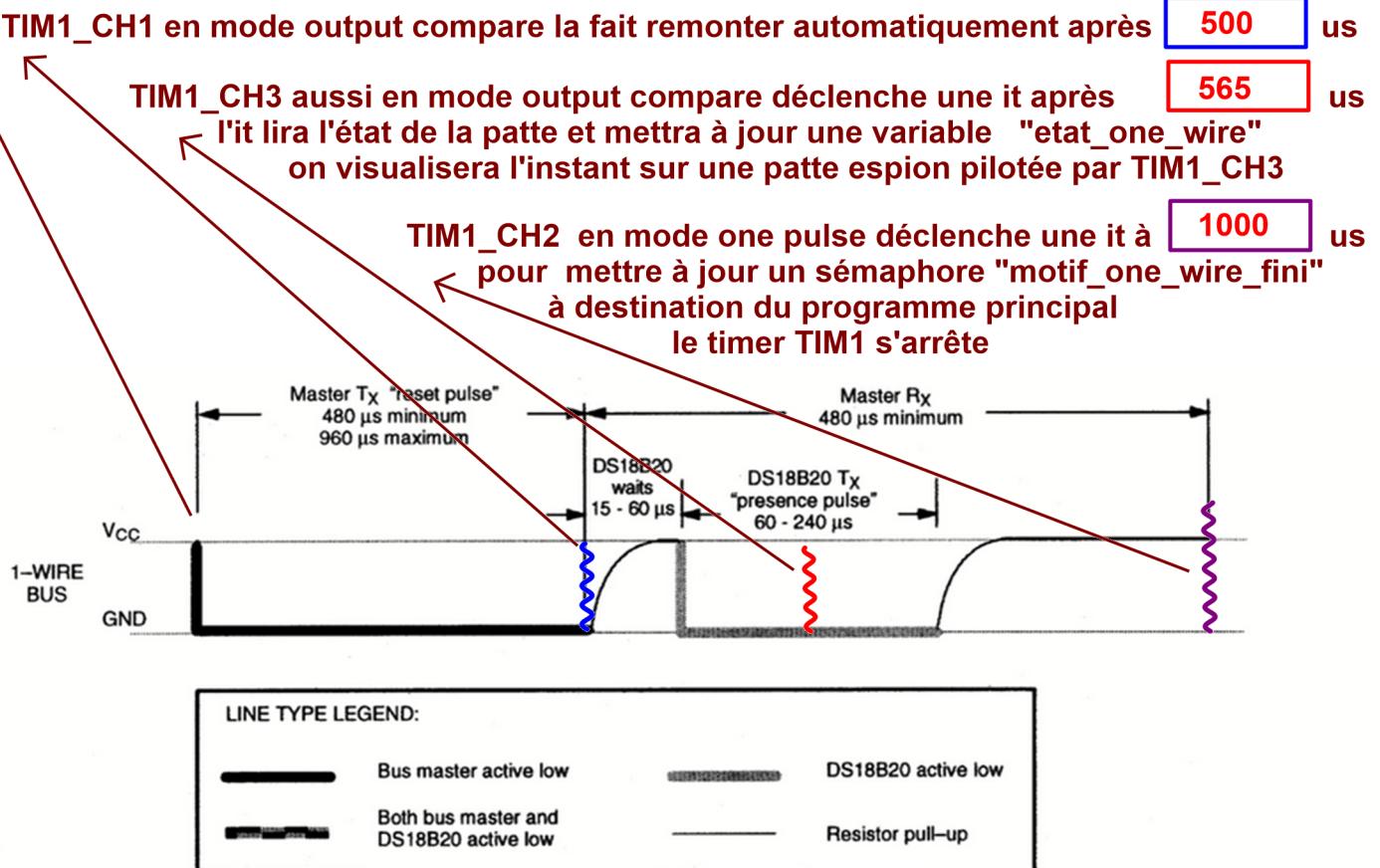
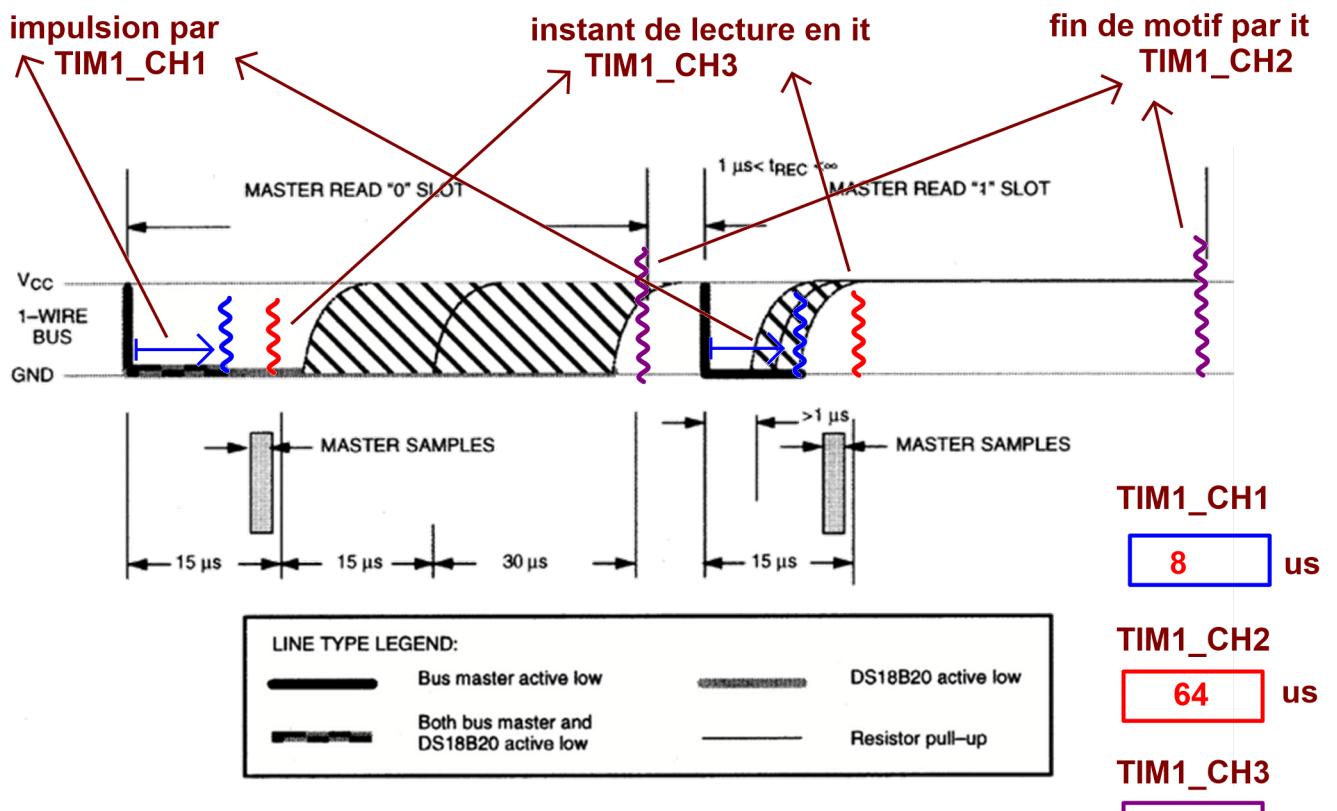


# gestion du signal de reset et détection présence

la fonction amorçant la gestion d'une impulsion niveau bas lance le timer TIM1

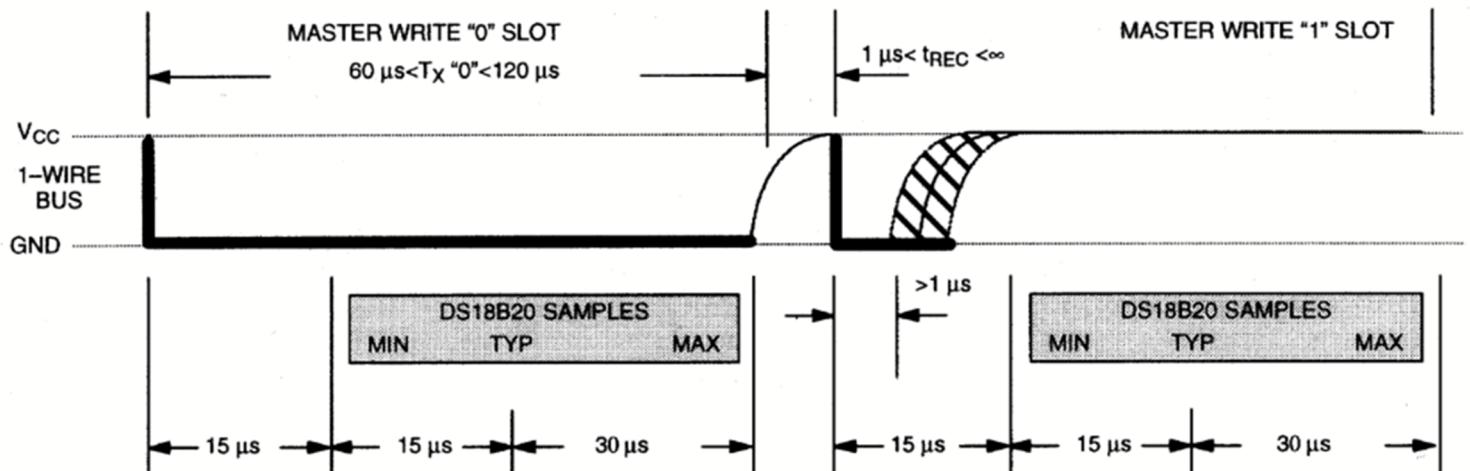


## gestion de la lecture d'un bit 0 ou 1 en one wire

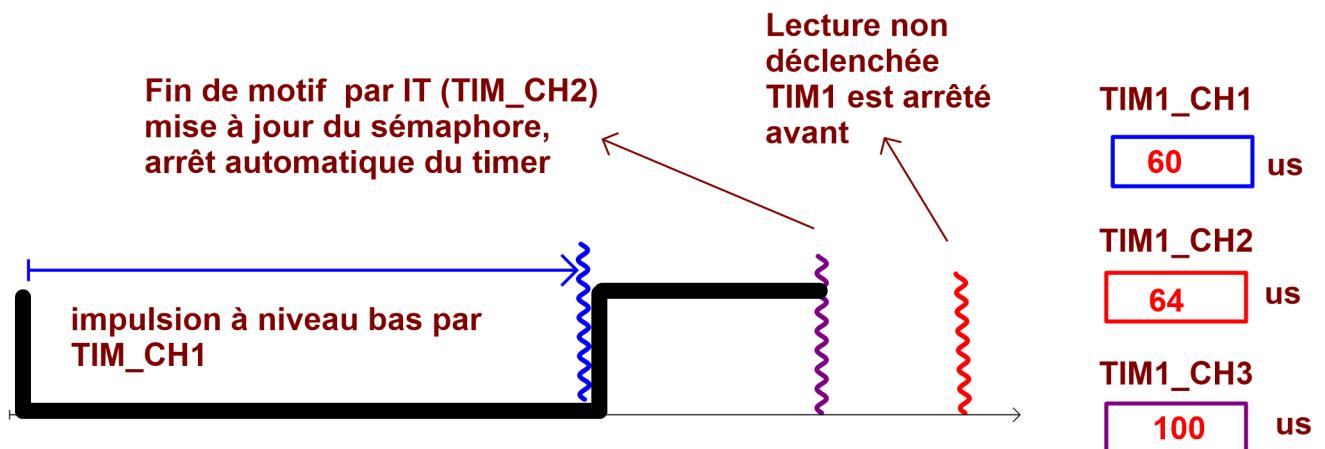


on utilisera donc la même fonction que celle lançant l'impulsion du reset en la paramétrant avec des temps différents

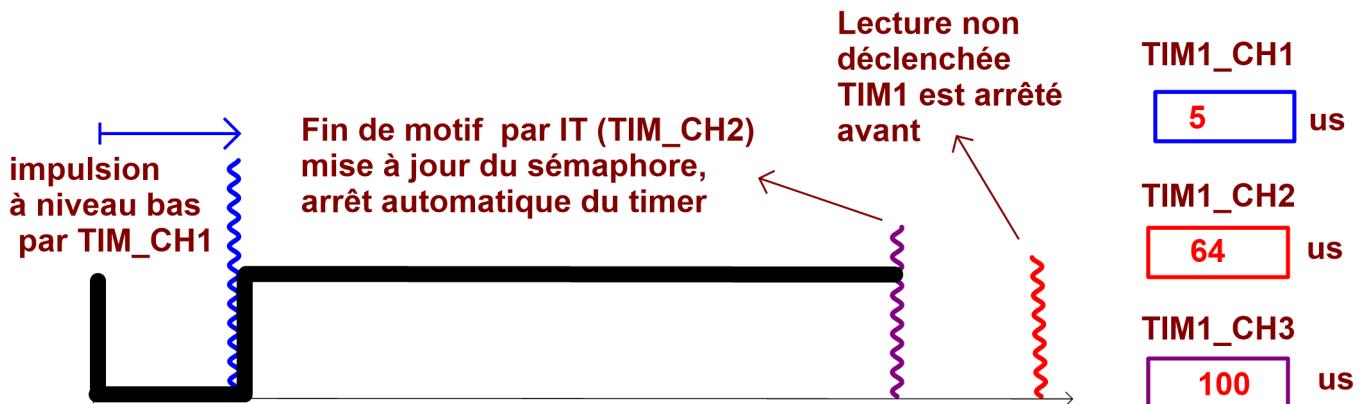
## gestion de l'écriture d'un bit 0 ou 1 en one wire



Réglages pour envoyer un 0 : la lecture est inutile, la mettre après la fin du motif



Réglages pour envoyer un 1 : la lecture est inutile, la mettre après la fin du motif



#### 14.4.1 TIM1 and TIM8 control register 1 (TIMx\_CR1)

Address offset: 0x00

Reset value: 0x0000

#### 14.4.2 TIM1 and TIM8 control register 2 (TIMx CR2)

Address offset: 0x04

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	OIS4	OIS3N	OIS3	OIS2N	OIS2	OIS1N	OIS1	TI1S	MMS[2:0]			CCDS	CCUS	Res.	CCPC
	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw		rw

#### 14.4.3 TIM1 and TIM8 slave mode control register (TIMx\_SMCR)

Address offset: 0x08

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETP	ECE	ETPS[1:0]		ETF[3:0]				MSM	TS[2:0]			Res.	SMS[2:0]		
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	Res.	rw	rw	rw

#### 14.4.4 TIM1 and TIM8 DMA/interrupt enable register (TIMx\_DIER)

Address offset: 0x0C

Reset value: 0x0000

#### 14.4.5 TIM1 and TIM8 status register (TIMx\_SR)

Address offset: 0x10

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	rc_w0	rc_w0	rc_w0	rc_w0	Res.	rc_w0									

#### 14.4.6 TIM1 and TIM8 event generation register (TIMx\_EGR)

Address offset: 0x14

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	w	w	w	w	w	w	w	BG	TG	COMG	CC4G	CC3G	CC2G	CC1G	UG

#### 14.4.7 TIM1 and TIM8 capture/compare mode register 1 (TIMx\_CCMR1)

Address offset: 0x18

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
OC2 CE	OC2M[2:0]			OC2 PE	OC2 FE	CC2S[1:0]			OC1 CE	OC1M[2:0]			OC1 PE	OC1 FE	CC1S[1:0]			
	IC2F[3:0]									IC1F[3:0]			IC1PSC[1:0]					
	rw			rw			rw		rw		rw		rw					
	rw			rw			rw		rw		rw		rw					

#### 14.4.8 TIM1 and TIM8 capture/compare mode register 2 (TIMx\_CCMR2)

Address offset: 0x1C

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
OC4 CE	OC4M[2:0]			OC4 PE	OC4 FE	CC4S[1:0]			OC3 CE.	OC3M[2:0]			OC3 PE	OC3 FE	CC3S[1:0]			
	IC4F[3:0]									IC3F[3:0]			IC3PSC[1:0]					
	rw			rw			rw		rw		rw		rw					
	rw			rw			rw		rw		rw		rw					

#### 14.4.9 TIM1 and TIM8 capture/compare enable register (TIMx\_CCER)

Address offset: 0x20

Reset value: 0x0000

#### 14.4.18 TIM1 and TIM8 break and dead-time register (TIMx\_BDTR)

Address offset: 0x44

Reset value: 0x0000