2.2 Memory organization

2.2.1 Introduction

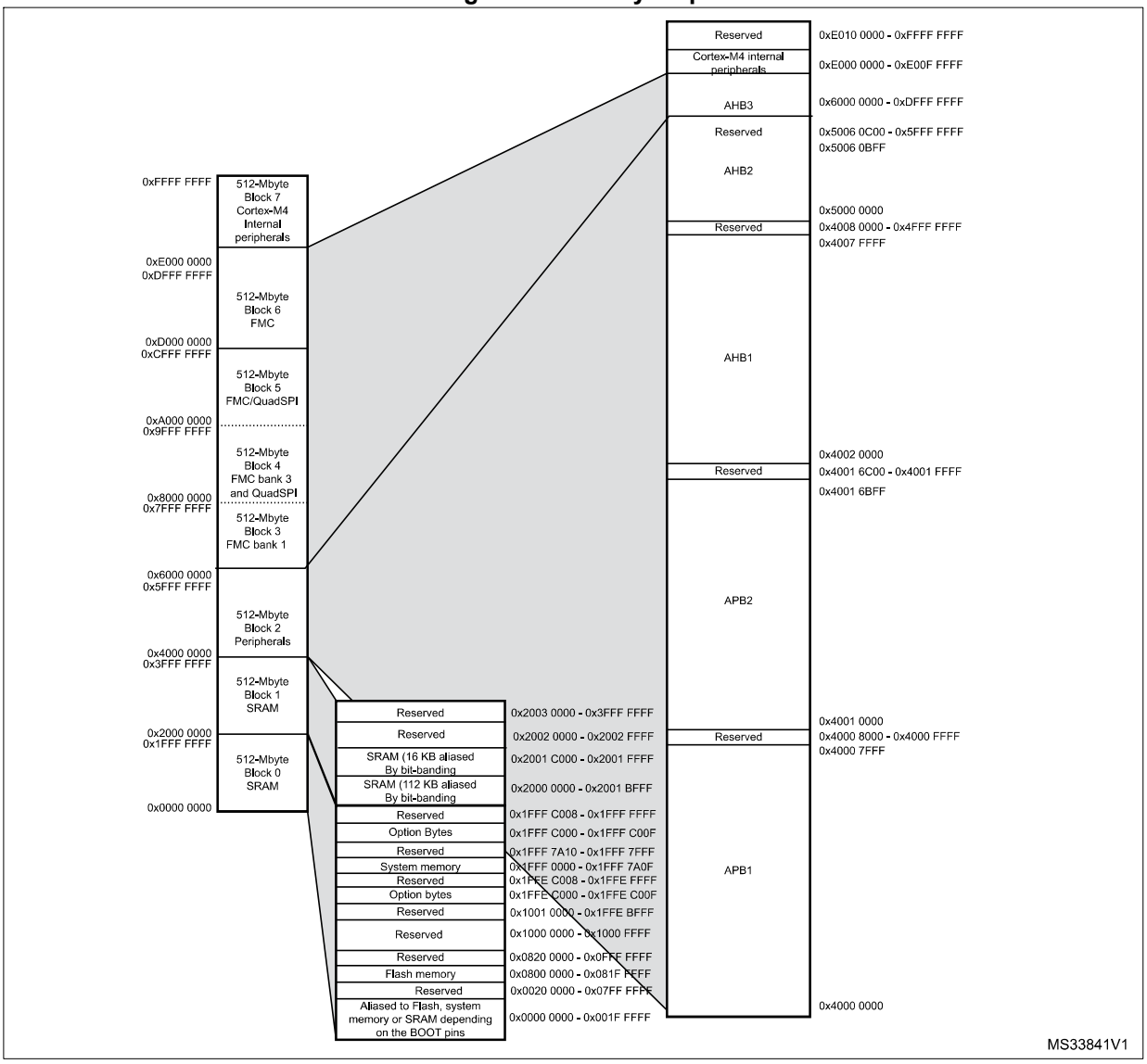
Program memory, data memory, registers and I/O ports are organized within the same linear 4-Gbyte address space.

The bytes are coded in memory in Little Endian format. The lowest numbered byte in a word is considered the word's least significant byte and the highest numbered byte the most significant.

The addressable memory space is divided into 8 main blocks, of 512 Mbyte each.

2.2.2 Memory map and register boundary addresses

Figure 2. Memory map



All the memory map areas that are not allocated to on-chip memories and peripherals are considered “Reserved”. For the detailed mapping of available memory and register areas.

The following table gives the boundary addresses of the peripherals available in the devices.

Table 1. STM32F446xx register boundary addresses

Boundary address	Peripheral	Bus	Register map
0xA000 0000 - 0xA000 0FFF	FMC control register	AHB3	*Section 11.8: FMC register map on page 323*
0xA000 1000 - 0xA000 1FFF	QUADSPI register	AHB3	*Section 12.5.14: QUADSPI register map on page 353*
0x5005 0000 - 0x5005 03FF	DCMI	AHB2	*Section 15.7.12: DCMI register map on page 448*
0x5000 0000 - 0x5003 FFFF	USB OTG FS	AHB2	*Section 31.15.61: OTG_FS/OTG_HS register map on page 1191*
0x4004 0000 - 0x4007 FFFF	USB OTG HS	AHB1	*Section 31.15.61: OTG_FS/OTG_HS register map on page 1191*
0x4002 6400 - 0x4002 67FF	DMA2		*Section 9.5.11: DMA register map on page 234*
0x4002 6000 - 0x4002 63FF	DMA1		
0x4002 4000 - 0x4002 4FFF	BKPSRAM		-
0x4002 3C00 - 0x4002 3FFF	Flash interface register		*Section 3.8: Flash interface registers on page 80*
0x4002 3800 - 0x4002 3BFF	RCC		*Section 6.3.28: RCC register map on page 172*
0x4002 3000 - 0x4002 33FF	CRC		*Section 4.4.4: CRC register map on page 91*
0x4002 1C00 - 0x4002 1FFF	GPIOH	AHB1	*Section 7.4.11: GPIO register map on page 193*
0x4002 1800 - 0x4002 1BFF	GPIOG		
0x4002 1400 - 0x4002 17FF	GPIOF		
0x4002 1000 - 0x4002 13FF	GPIOE		
0x4002 0C00 - 0x4002 0FFF	GPIOD		
0x4002 0800 - 0x4002 0BFF	GPIOC		
0x4002 0400 - 0x4002 07FF	GPIOB		
0x4002 0000 - 0x4002 03FF	GPIOA		
0x4001 5C00 - 0x4001 5FFF	SAI2	APB2	*Section 28.5.10: SAI register map on page 973*
0x4001 5800 - 0x4001 5BFF	SAI1		
0x4001 4800 - 0x4001 4BFF	TIM11	APB2	*Section 18.5.12: TIM10/11/13/14 register map on page 626*
0x4001 4400 - 0x4001 47FF	TIM10		
0x4001 4000 - 0x4001 43FF	TIM9		
0x4001 3C00 - 0x4001 3FFF	EXTI		*Section 10.3.7: EXTI register map on page 249*
0x4001 3800 - 0x4001 3BFF	SYSCFG		*Section 8.2.9: SYSCFG register maps on page 202*
0x4001 3400 - 0x4001 37FF	SPI4	APB2	*Section 26.7.10: SPI register map on page 896*

Table 1. STM32F446xx register boundary addresses (continued)

Boundary address	Peripheral	Bus	Register map
0x4001 3000 - 0x4001 33FF	SPI1	APB2	*Section 26.7.10: SPI register map on page 896*
0x4001 2C00 - 0x4001 2FFF	SDMMC		*Section 29.8.16: SDIO register map on page 1030*
0x4001 2000 - 0x4001 23FF	ADC1 - ADC2 - ADC3		*Section 13.13.18: ADC register map on page 398*
0x4001 1400 - 0x4001 17FF	USART6		*Section 25.6.8: USART register map on page 845*
0x4001 1000 - 0x4001 13FF	USART1		
0x4001 0400 - 0x4001 07FF	TIM8		*Section 16.4.21: TIM1&TIM8 register map on page 519*
0x4001 0000 - 0x4001 03FF	TIM1		