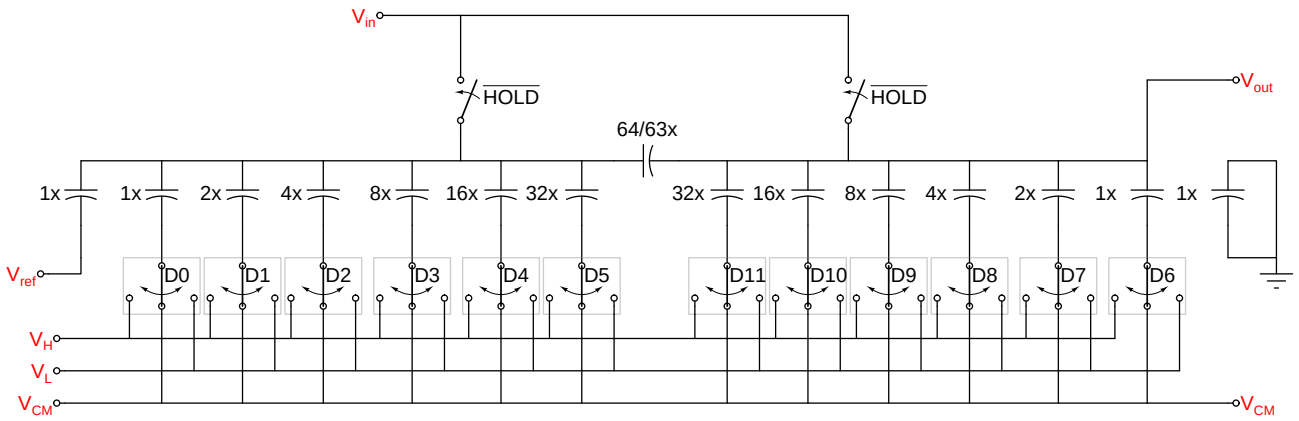
12-bit precision CDAC with integrated sample-and-hold for ADC

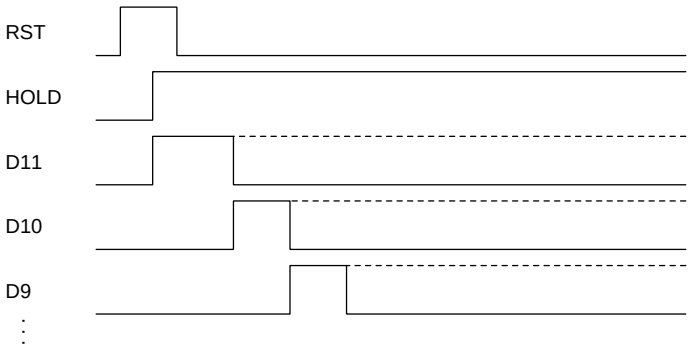


NOTE: The canonical DAC generates an output between V_L and V_H. For a SAR ADC, this output is compared to the input.
This variation first resets the cap top plates to V_{in} instead of V_L while the cap bottom plates are held at V_{CM}.
The digital value then changes the output value so that the output = V_{CM} when the traditional DAC output would be equal to V_{in}.
This allows the ADC comparator to be fine-tuned around an input of V_{CM} and it does not need rail-to-rail operation.
V_{ref} can be tuned (relative to V_{CM}) for calibration.
The DAC capacitor top plates act as the sampling capacitor for the input.

This operates like the original CDAC if $V_{in} = V_{CM} = V_L$. Otherwise, normal operation is with $V_{CM} = 1/2\ V_{DD}$ and may not differ from $1/2\ (V_H + V_L)$ by more than 1/2 V.

Voltage on cap bottom =
- V_{CM} if RST = 1
- V_L if RST = 0, Dx = 0
- V_H if RST = 0, Dx = 1

Timing:



RST must be asserted high when HOLD is applied

HOLD remains high for the duration of conversion

The first bit should be raised any time while RST is high

The comparator is sampled after each bit is applied. If the comparator result is high, then the bit is left high. If the comparator result is low, then the bit is set low. After all bits have been tested, the value D[11:0] is the result.