CMOS Logic

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Logic Implementation History

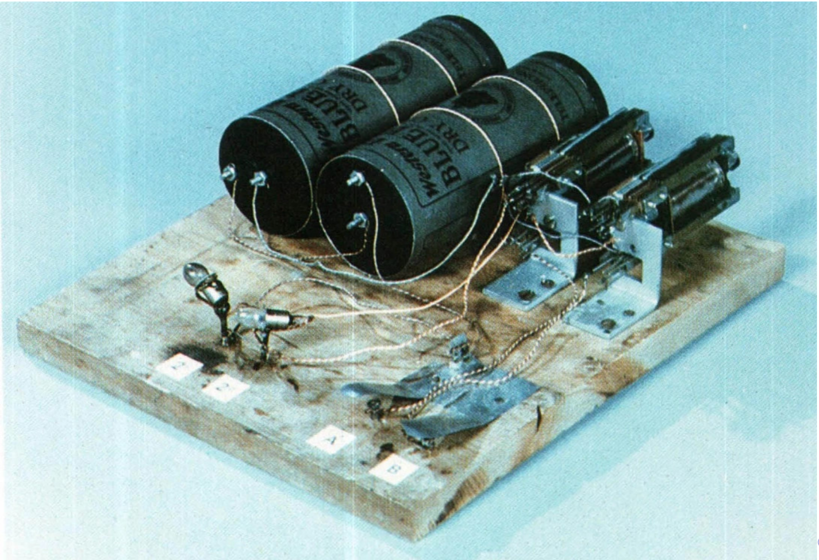
Part	Technology	Speed	Power	Date / Description
	Relay	10 ms	~ 5W	1930s-1940s
	Tubes	μs	~ 6W	1940s
	BJT	ns	~ 0.06W	1950s
7400	TTL	10-20 ns	1-10 mW	1960s
Intel 4004	PMOS	~ 100 ns	$\sim 217\mu$W	1971
74HC	CMOS	10-20 ns	μW	1980s
Motorola 68k	NMOS	~ 100 ns	$\sim 22\mu W$	1979, 8 MHz
Intel 80386	NMOS	~ 20 ns	$\sim 5.5\mu W$	1985, 12 MHz
Apple M1/M4	CMOS	~ 10 ps	few fJ	2020s, 5 nm
AMD Ryzen	CMOS	$\sim 5 - 20$ ps	few fJ	2023, 5 nm

Overview

- Technology improved from tubes to discrete transistors to integrated circuits
- Power per gates improved from watts to micro watts to femto watts
- Older circuits used power all the time
- Modern circuits use power only when state is changing
- Power per gate continues to decrease
- Speed of gates continues to increase slowly
- Problem is we keep using more transistors so power usage increases

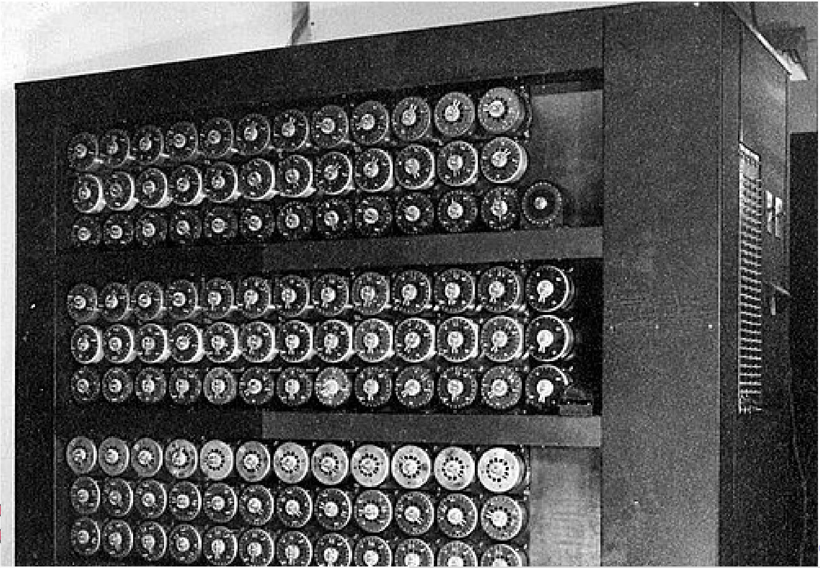
1920s: Relays

A relay is an electromechancial switch
Early automation of the phone system

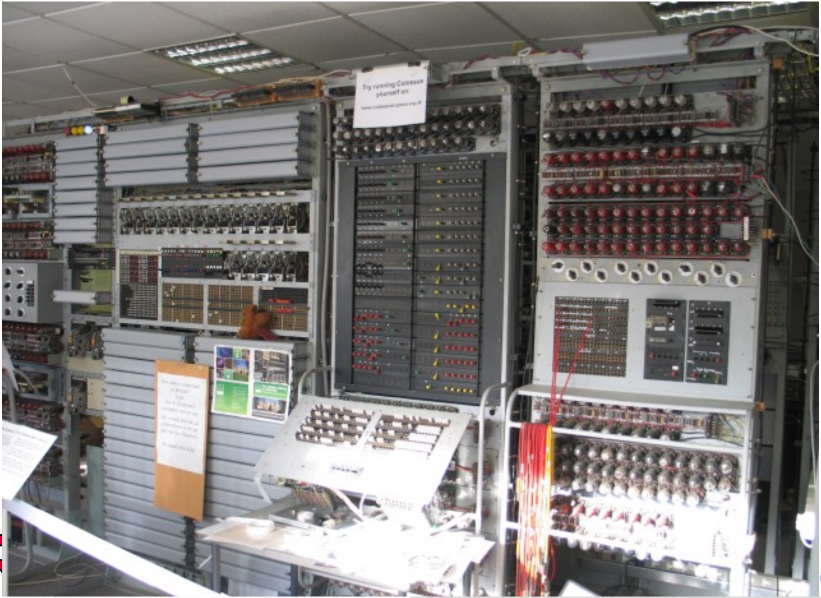


Last gasp of Relays: Turings Bombe

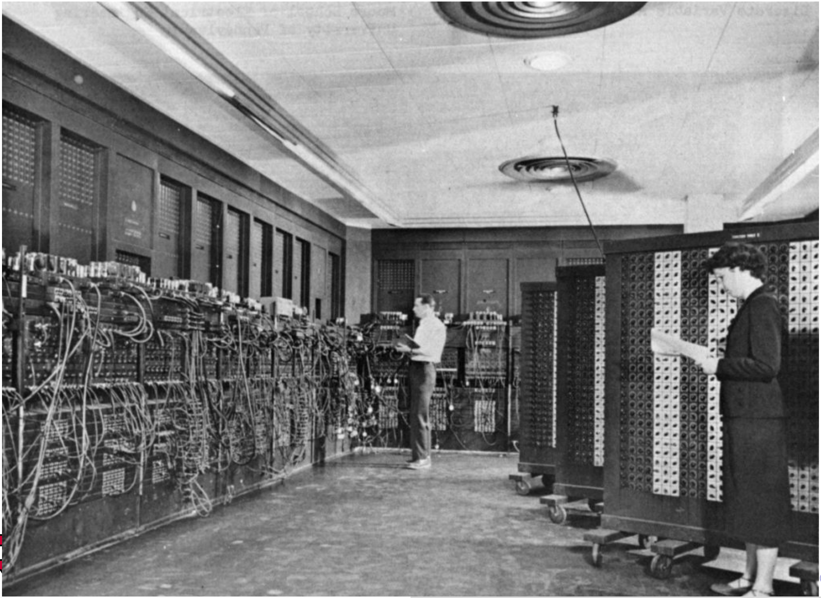
In World War II, used to break the German Enigma code
Fictionalized in the movie "The Imitation Game"



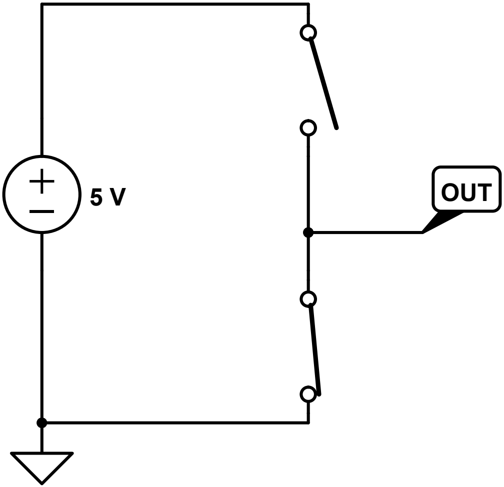
Much faster than Turing's Bombe: Collossus in WW II



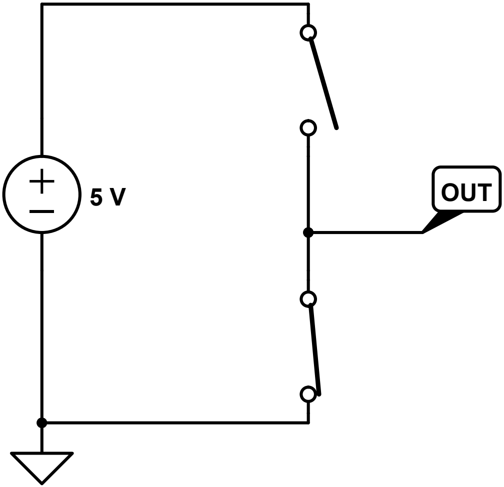
Early Tube Computers: ENIAC 1946



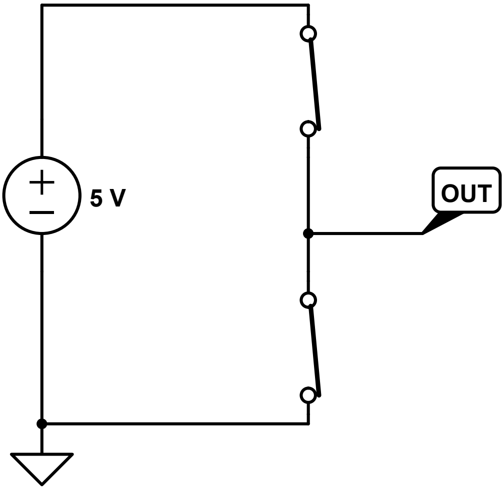
Switch Equivalents of Transistors



Switch Equivalents of Transistors 2

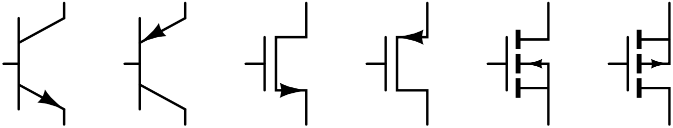


Switch Equivalents of Transistors 3



Two Kinds of Transistors

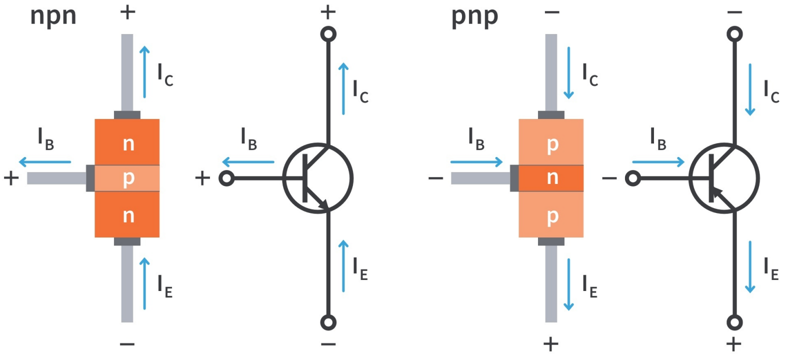
- Bipolar Junction Transistors (BJT)
  - Base, Emitter, Collector
- Field Effect Transistors (FET)
  - Gate, Source, Drain



BJT: Bipolar Junction Transistor

- First kind of Transistor
- Three terminals: Base, Emitter, Collector
- A small current at the base controls a larger current from the emitter to the collector
- Two types: NPN and PNP
- NPN is more efficient than PNP
- Dominated for most applications by FETs, used in low-cost applications

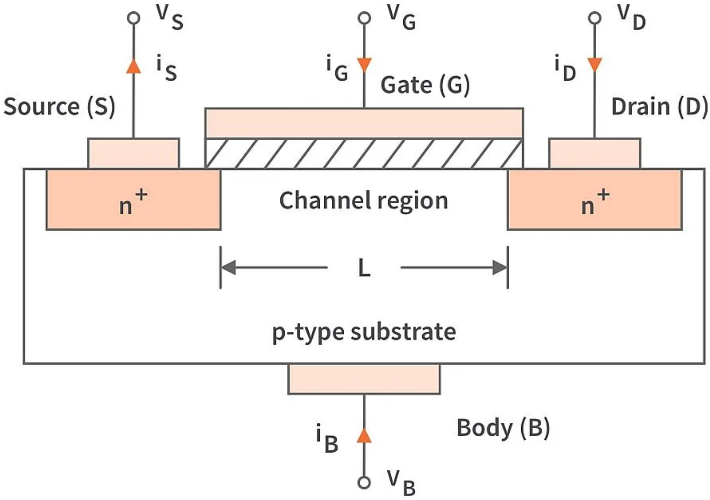
BJT: Bipolar Junction Transistor



See: BJT Basics

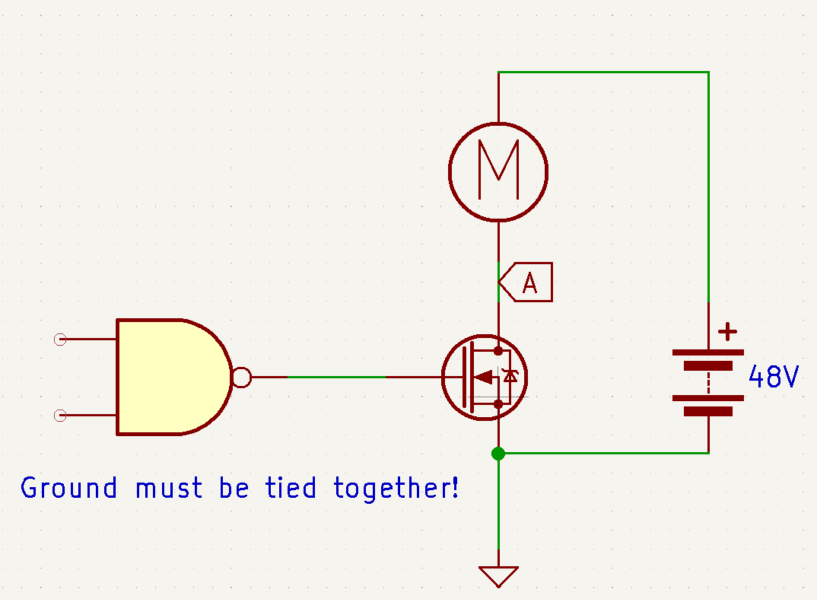
FET

- FETs are controlled by voltage
- Three terminals: Gate, Source, Drain
- Much lower power consumption than BJTs
- Very high gate resistance ($> 1M\Omega$)
- N-Channel: Turns on with $V_g > S + V_{GS}$
- P-Channel: Turns on with $V_g < S - V_{GS}$


v_S
i_S
Source (S)
v_G
i_G
Gate (G)
v_D
i_D
Drain (D)
n^+
Channel region
n^+
L
p-type substrate
i_B
Body (B)
v_B

Before Logic: Motor Control

Use a Power MOSFET to control a motor



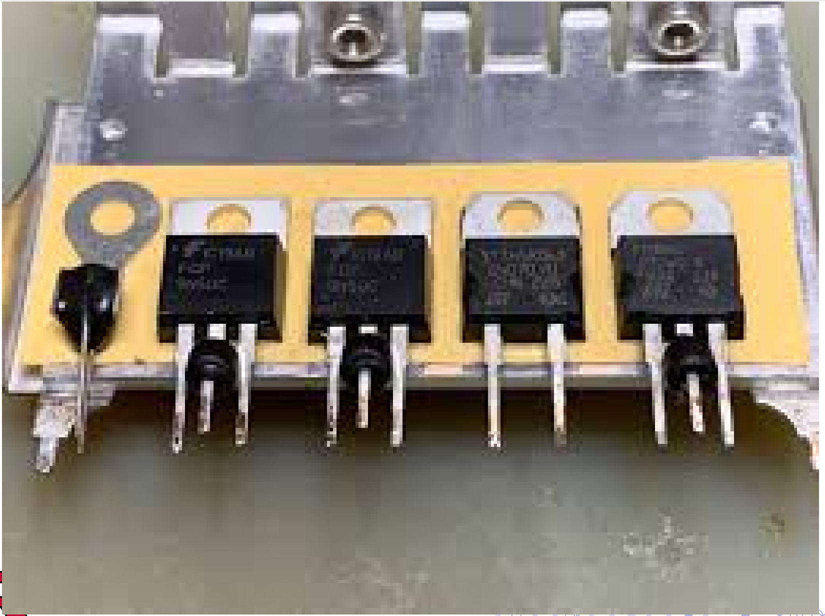
IRF540N Datasheet

- Maximum Drain-Source Voltage (V_{DS})
- Maximum Gate-Source Voltage (V_{GS})
- Maximum Drain Current (Id)
- Threshold Voltage ($V_{GS}(th)$)
- On-Resistance (RDS_{on})

MOSFET: Reading a Spec Sheet

Search part number + "spec" or "datasheet" How much voltage can the MOSFET switch on? (V_{DS})
What is the maximum voltage that can be applied to the gate?
What is the voltage to the gate needed to turn the MOSFET completely on?
What is the maximum current that can be drawn from the drain? (Id)
Note: This will require a heat sink to keep the MOSFET from overheating.
What is the resistance of the MOSFET when it is on? (RDS_{on})

MOSFET: Heat Sinks



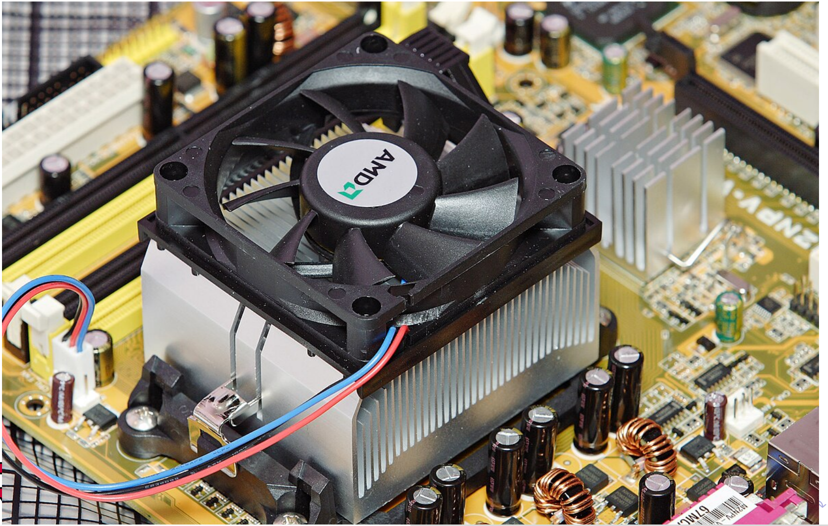
CPU Heat

- Heat is proportional to I^2R
- Consider each generation shrinking transistors by a factor of 2
- R decreases by a factor of 2?
- But there are now 4 times as many transistors
- I increases by a factor of 2? (seems wrong)
- So $P = I^2R$ increases by a factor of 4?
- this is not my area. But I have read that power consumption/dissipation increases by $\sqrt{2}$
- In any case, this is why voltage keeps decreasing. It has to.

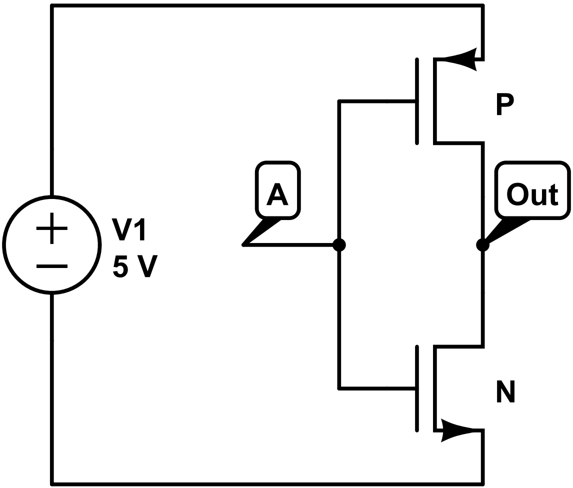
CPU Heat Sinks

The transistors in computers are very small, but there are a lot of them packed tightly

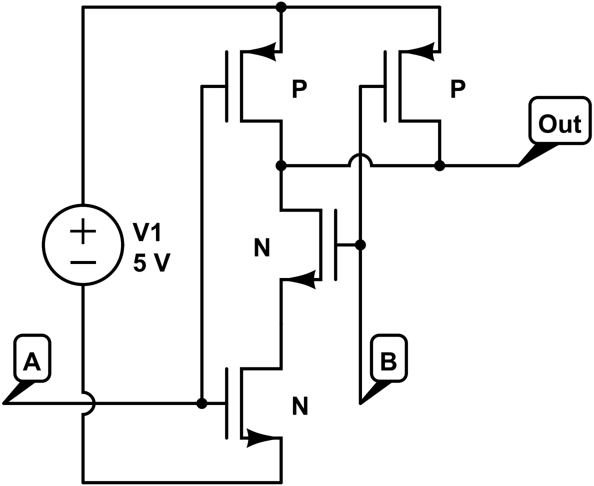
This generates a lot of heat



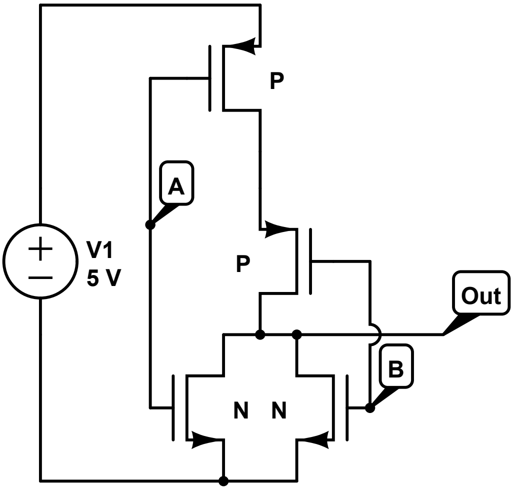
CMOS NOT Implementation



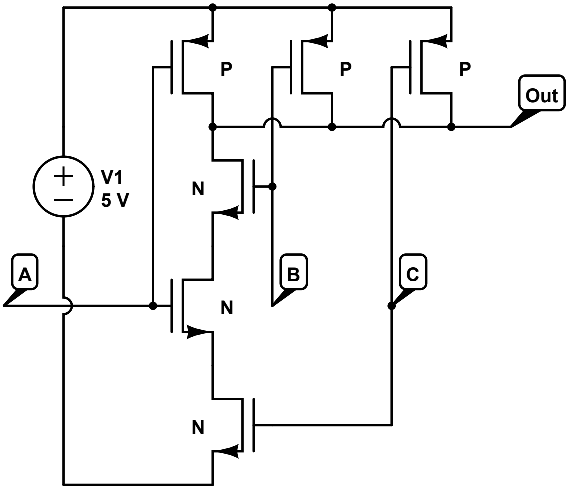
CMOS NAND Implementation



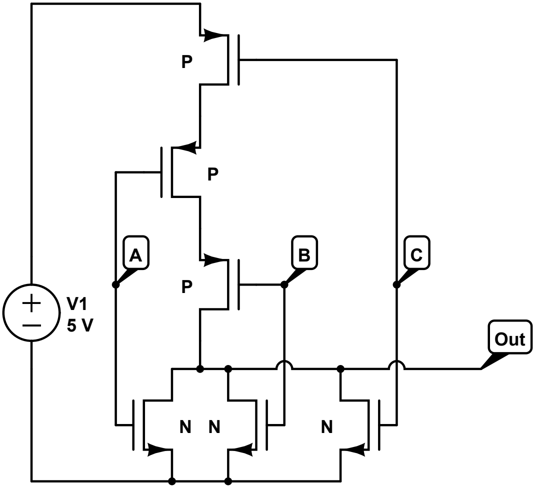
CMOS NOR Implementation



CMOS 3-Input NAND Implementation



CMOS 3-Input NOR Implementation



Switch Equivalent States: NAND

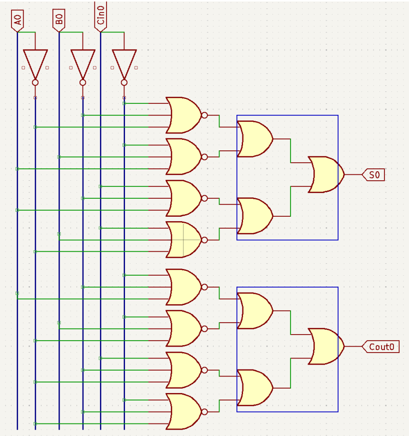
Switch Equivalent States: NOR

Gate Delays

- Switching a transistor on and off takes a finite time
- 74LS gate delays are 10ns
- 4000 CMOS delays are 1ns
- Modern Computers clock cycles of 3GHz
- In that time, hundreds of gate delays must happen
- Details are proprietary. Hard to find out how fast
- Assume 300 gate delays per clock cycle: $333ps/300 = 1.11ps$
- Chatgpt claims 5-20ps. It's probably right but I can't verify

Gate Delay for a Circuit

Gate delay is the longest path through the circuit.
What is the delay, given the NOT takes 500ps and



NAND/NOR/OR take 1ns?

A tri-state Buffer

A tri-state buffer can disconnect an input from an output

Used to create larger multiplexers by disconnecting all but one input