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Lab I: Blink a light; control the world

Introduction to Embedded Systems

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Executive Summary

In the grand scheme of embedded things, by the time you have gone through the process to successfully blink an LED at a regulated rate, you have probably done about 90% of groundwork for everything else you will do with the processor. This may seem like a very bold statement to make, but think about all the steps it actually takes to simply turn on and off one pin of a MCU. In this lab, you will be doing the equivalent of “Hello, World!” for multiple platforms and it is expected that everyone does it on their own. Since this assumed that this will be your first foray into using Microcontrollers and the C language, the assignment will remain simple. However; do not take this as an invitation to procrastinate as something as simple as blinking an LED could take hours to debug at first. Trust me, it has bitten me in the past.

Lab Goals

By the end of this lab you should:

1. become comfortable with the Code Composer Studio IDE
2. familiarize
3. Slave Functions
4. Integration Process

1 Physical Interfaces

1.1 MSP430FR4133 PIC24 Interface

1.1.1 MSP430FR4133

- Logic Levels $V_{cc} = 3V$
  - Input Positive Going Threshold: 1.35V - 2.25V
  - Input Negative Going Threshold: 0.75V - 1.65V
  - Output High: 2.4V - 3.0V
  - Output Low: 0.0V - 0.60V
- SPI Pins:
  - SCLK: Pin 22 (P1.2/UCA0CLK/A2)
  - MISO: Pin 23 (P1.1/UCA0RXD/UCA0SOMI/A1/V_{eref+})
  - MOSI: Pin 24 (P1.0/UCA0TXD/UCA0SIMO/A0/V_{eref-})

1.1.2 PIC24FJ256GA110

- Logic Levels $V_{cc} = 3.3V$
  - Input Positive Going Threshold: tbd
  - Input Negative Going Threshold: tbd
  - Output High: 2.7 - 3.3V
  - Output Low: 0.0 - 0.6V
- SPI Pins (SPI2):
  - SCLK: Pin 10 (RP21)
  - MISO: Pin 11 (RP26)
  - MOSI: Pin 12 (RP19)

1.2 Electrical Characteristics

1.2.1 MCU GPIO

This should be pulled straight from the data sheet

- MSP430FR4133
  - Input Capacitance, Digital Only Pin: 3pF
  - Input Capacitance, Shared Analog: 5pF
  - High-Impedance

2 Software Interfaces

2.1 SPI Settings

- SCLK: 2 MHz
- Data Order: MSB First

3 Slave Functions

Table 1: My caption

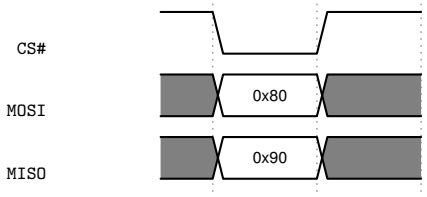
Received Command	Header	Function ID	Length	D1	D2...Dn	Cheksum
Clear to Send	0x80	-	-	-	-	-
Begin Experiment	0x80	0x11	0x05	Reps.	D, H, M, S	CHK
Pause Experiment	0x80	0x22	-	-	-	-
Resume Experiment	0x80	0x33	-	-	-	-
Abort Experiment	0x80	0x44	-	-	-	-
Send Experiment Data	0x80	0x55	n	D1	D2...Dn	CHK
Prepare Firmware Upload	0x80	0x66	0x01	Num. Of Packets	-	CHK
Send Firmware Upload	0x80	0x77	n	Packet Number	D1...Dn	CHK
Begin Bootloading	0x80	0x88				
Enter Low Power Mode	0x80	0x99	-	-	-	-
Enter Shutdown Mode	0x80	0xAA	-	-	-	-
Reset	0x80	0xBB	-	-	-	-

3.1 Clear to Send (CTS)

The CTS is sent prior to every other function to ensure that the slave processor is ready to receive a command. There are three possible responses to a sync frame: ACK, NACK, TIMEOUT.

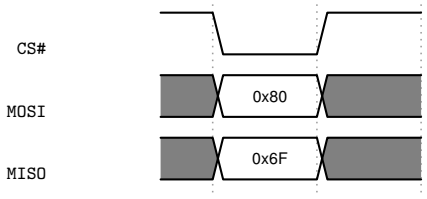
3.1.1 ACK

This is the typical response, where the slave device ACK's and sets itself into a ready state.



3.1.2 NACK

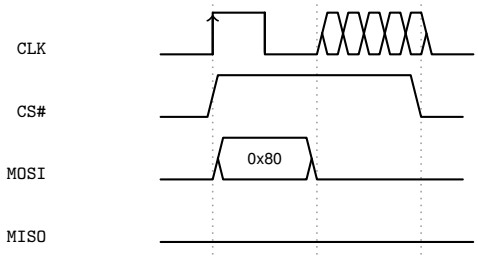
This response is sent by the processor when it is busy or can not process a command at the current time.



3.1.3 TIMEOUT

This is an atypical response and accounts for when the processor might be in an inescapable loop or in the middle of a bootloading sequence. In this scenario the slave device does not respond in any way to the

sync frame. A TIMEOUT is considered when there is no response after N clock cycles



3.2 Begin Experiment

This command tells the MME processor to execute multiple repetitions of its experiment with an interval of Days, Hours, Minutes, and Seconds. Reps, D, H, M, and S are all one byte long. Since this command has a fixed length, the length field remains at a constant 0x05. A valid checksum is required for the retrieval of an ACK. Upon receiving an ACK, the MME processor shall begin the experimental procedure.

A Reps. value of 0x00 corresponds to a single run of the experiment delayed by the DHMS bytes. The valid ranges of the Reps and DHMS values are:

- Reps.: 0xFF (255)
- D (Days): 0x07 (7)
- H (Hours): 0x17 (23)
- M (Minutes): 0x3B (59)
- S (Seconds): 0x3B (59)

All timing done by the MME processor shall be done by clock cycles referenced to the internal clock. If precision timing is required, it is recommended to perform a single read with no delay and utilize the CDH RTC.

At the end of the experiment, the data retrieved shall be stored in the MME processor's FRAM until the Send Experiment Data Command is received. It is currently undecided whether the overwrite previous data if needed or to send an error flag upon requesting to run the experiment.