Rowan ECE Department
Printed Circuit Board Design and Ordering Process

In an effort to support and further foster a hands-on engineering experience, the ECE Department batch orders printed circuit boards (PCB) by combining them into one large order. We combine PCB designs from many students and faculty/staff members onto a large panel that can be manufactured very cost effectively. The boards are paid for by the department, there is no cost to you.

We will post the submission dates for orders, typically 3-4 orders per semester.

To minimize board panelization errors we prefer you use Diptrace. If you would like to use a different PCB CAD tool, please check with us BEFORE you start your design. You can download Diptrace here:

http://diptrace.com/download-diptrace/

We use Prototron to fabricate our panels. Below is the link to their board specs. You will follow the specs for the Tuscon facility.

http://www.prototron.com/documents/FullCapabilities.pdf

These are the typical panel specs:

18" x 24" panel (16" x 22" usable space)
Inter-board spacing = 0.2"
2 layers
0.062" FR4
1 oz. copper
ENIG finish
Solder mask color – varies
5-day fabrication time (business days)
3-day transit time (business days)

Make sure to place your name on your board (top or bottom silk screen layers) so we can identify it during fabrication and when the boards arrive here.

Each student/team should name their files as follows:

Filename root syntax: ccccc-ss_uuuuuu_d_q.xxx

ccccc = 5 digit course number
ss = 2 digit section number (01-99)
uuuuuu = Rowan Username (i.e. uuuuu@students.rowan.edu) of person submitting the design
d = design number
- 0 = only one design is being submitted
- 1 = design #1 of a multi design submission
- 2 = design #2 of a multi design submission
- ...

q = quantity of boards needed, typically one per team member/student
xxx = file extensions per below

Example:
for Intro to Embedded section 2, file root name is: 09342-02_leonem_0_1.xxx

List of project files:

09342-02_leonem_0_1.dch	Diptrace schematic
09342-02_leonem_0_1.dip	Diptrace PCB layout

Generated by File/Export/Gerber

09342-02_leonem_0_1.gto	top silk layer
09342-02_leonem_0_1.gts	top solder mask
09342-02_leonem_0_1.gtl	top copper layer
09342-02_leonem_0_1.gbl	bottom copper layer
09342-02_leonem_0_1.gbs	bottom solder mask
09342-02_leonem_0_1.gbo	bottom silk layer
09342-02_leonem_0_1.gko	board outline

Generated by File/Export/NC Drill

09342-02_leonem_0_1.xln	drill file

09342-02_leonem_0_1.zip	ZIP file of the above files

Start by creating your schematic. Before starting your PCB layout, perform a Verification/Electrical Rule Check (F9) and address all identified errors. Save your file with your root name (default extension is .DCH).

If you have not been provided a board for your project, File/Convert to PCB (Ctl+B) and begin laying out your board in the PCB Layout program.

If you have been provided a board outline, open the provided template in the PCB Layout and save it as your root name (default extension is DIP). Associate your schematic with the template - File/Renew Layout From Schematic…/By Components… and select your .DCH file.

Layout your board. Once you are done with the board layout:

- Perform board verification (3 checks)
  - Verification/Check Design Rules
  - Verification/Check Net Connectivity
  - Verification/Compare to Schematic
- Export files
  - File/Export/Gerber
    - Click Files and make sure file syntax is correct
      - Board naming conventions are found here: https://oshpark.com/guidelines
        - Make sure that all files have the same base name and all extensions are correct.
        - Please see Fig. 1 showing Gerber file output configuration. You will only need to do this once.

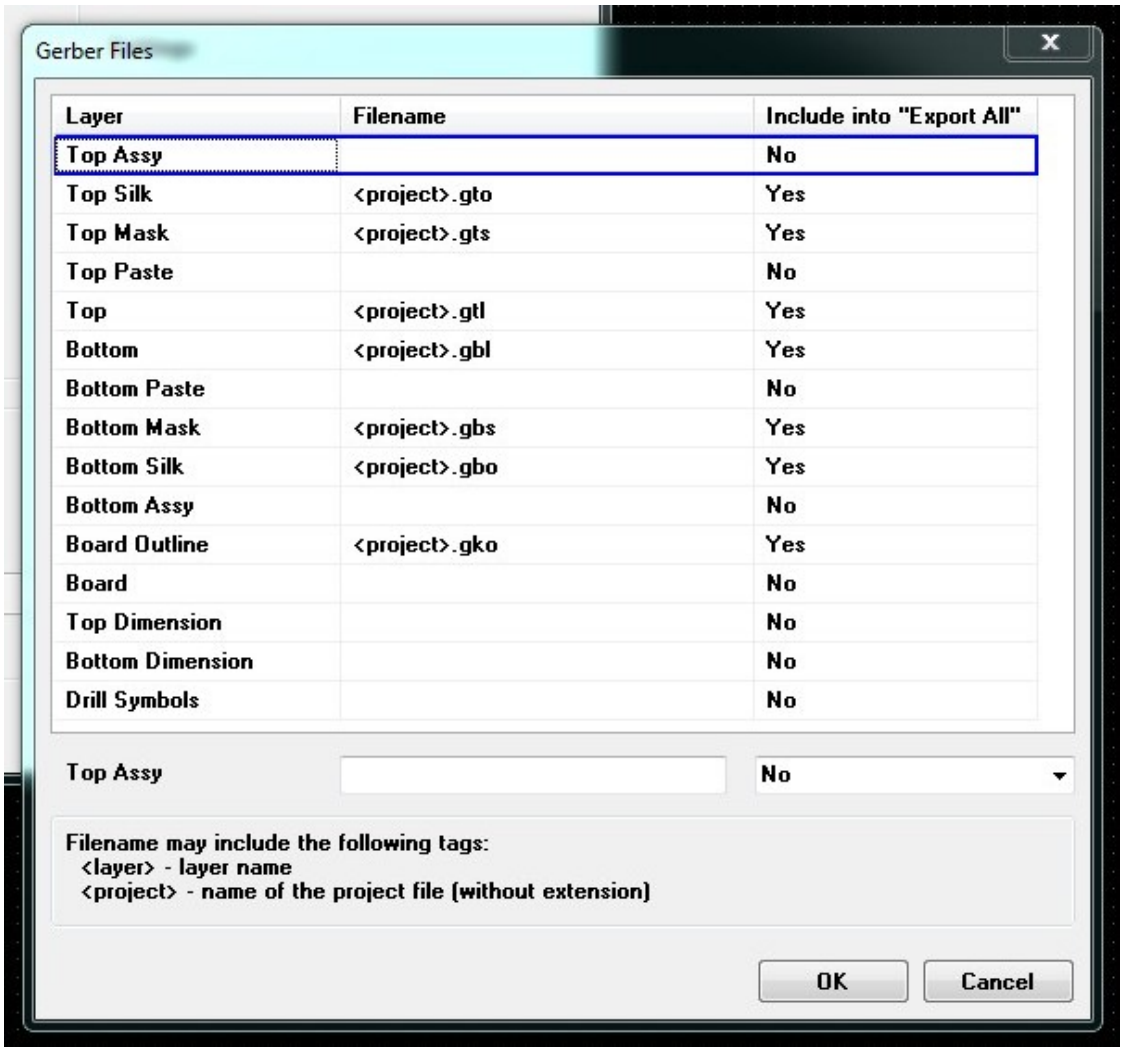

Fig. 1

- Export All (you will need to hit Save for each layer)

o File/Export/NC Drill

- Click Auto to assign tools
- Export All
  - Rename the file to your baseboard name with a .XLN extension (no .DRL), **you may need to manually do this in the file directory after export**.

- You will have 8 files as listed above
- Verify your output files by opening them in *gerbv* (File/Open layers…/[navigate to your folder and select all 8 layers]). Gerbv is a free open-source Gerber viewer; it supports all

popular OS's. You may turn layers on/off individually to make sure each layer looks like you expect.

- Zip the 8 files (using the **ZIP format**), no encryption, use the base board name [e.g. 09342-02_leonem_0_1.zip], **DO NOT place files in a sub-folder within the ZIP file, place them in the root of the ZIP file**.
- Upload the zip file to OSH Park (https://oshpark.com/). This is an excellent tool for visually checking your work, plus OSH Park does some error checking for you. Just because it uploads without error does not ensure a clean design. CAREFULLY examine each layer, look at all error messages.

If all looks good, email the ZIP file to leonem@rowan.edu and meyersj2@rowan.edu with the Subject: ECEBR

COMMON ERRORS (from previous classes)
No name on the PCB (silk layers)
Files have different base names
Files have incorrect extensions
Incorrect copper pours
Missing drill files (or misnamed)
Non-ZIP formats (.7z, .rar)
Files not in ZIP rot

Any designs found to have errors will not be included in the panel fabrication, so make sure you double check your work.

Stencil Addendum

Stencils can be ordered through Oshstencil. Stencils are needed for boards using surface mount parts with a lead pitch smaller than approximately 1mm, and can provide substantial time savings for surface mount boards that use parts large enough to manually paste.

Two types of stencils are available: Stainless, which are recommended for any parts with a .65mm or smaller pitch, and Kapton, which are a lower cost option for pcbs using larger parts.

To submit a stencil order, in addition to the board files listed above, you will need to export an additional gerber file, which is labeled paste or pastemask depending on which program you are using (Top Paste in Diptrace). You will then need to submit that and the board outline file in a zip.

Follow the same rules listed above for boards for file naming (append '_stencil' to the zip file).

Example file names:

09342-02_leonem_0_1.gtp	top paste mask layer
09342-02_leonem_0_1.gko	board outline
09342-02_leonem_0_1_stencil.zip	zip containing above 2 files

Before submitting, upload your zip to oshstencil and make sure that it processes correctly. Ensure that the Paste mask openings are smaller than the pads by an appropriate amount, that the correct parts are represented (connectors, through hole parts, etc. should not be on the stencil), and that the design dimensions shown are correct.

Once the stencil is correct, email the ZIP file to leonem@rowan.edu and meyersj2@rowan.edu with the Subject: ECESR

Reference standard:

http://www.pcbcart.com/skins/default/en/IPC-7525.pdf

Use this as a starting point, it won't always be possible to follow this exactly, but it's definitely a step in the right direction.