System Time

Signature and Grading Sheet

Group #:_____ Name(s):_____ .

Signature

Section 3.1(c): _____.

Section 3.2(b): _____.

Grading

- Section 3.1(a): C code (40 points):_____.
  Attach code printout (the code must be properly formatted and commented to get full credit)
- Section 3.1(b): code size (10 points) _____.
  Attach screen capture of file size (similar to Figure A.17)
- Section 3.1(c): demo (30 points):_____.
- Section 3.2(a): C code (10 points):_____.
  Attach code printout (the code must be properly formatted and commented to get full credit)
- Section 3.1(b): demo (10 points):_____.

Total points: _____.

Experiment
System Time

1 Purpose

To learn basic low-level I/O programming

2 Reading

- Chapters 8 and 9 of *FPGA Prototyping b VHDL Examples 2nd edition: Xilinx MicroBlaze MCS SoC.*

3 Design Procedures

3.1 System time

Implement the system time in Experiment 9.10.4 in book. The vanilla FPro system derived in previous experiment can be used. Note that the displayed time should look like a "digital clock" (i.e., in the same place of terminal window) not a new message every second.

(a) Derive application software.

(b) Check the software code size.

(c) Demonstrate the circuit to instructor and get signature.

3.2 Wall time

We can synchronize the "system time" to a wall clock so that the mm:ss displayed on the terminal window is the same as the wall clock. This can be done by sending the current time as four digits via the terminal window (i.e., PuTTY) to "set the system". The rx_byte( ) method (i.e., uart.rx_byte( )) can be used to receive one byte (see Section 11.4).

(a) Derive application software.

(b) Demonstrate the circuit to instructor and get signature.