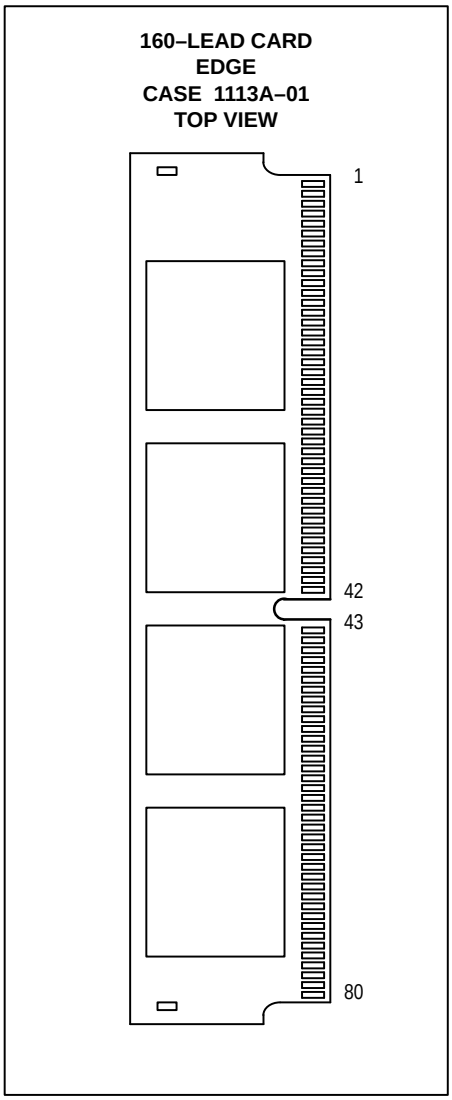
MCM72CF32
MCM72CF64

Advance Information

256KB and 512KB BurstRAM™ Secondary Cache Module for Pentium™



The MCM72CF32SG and MCM72CF64SG are designed to provide a burstable, high performance, 256K/512K L2 cache for the Pentium microprocessor. The modules are configured as 32K x 72 and 64K x 72 bits in a 160 pin card edge memory module. The module uses four of Motorola's MCM67C518 or MCM67C618 BiCMOS BurstRAMs.

Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$). Subsequent burst addresses are generated internal to the BurstRAM by the burst advance ($\overline{ADV}$) input pin.

Write cycles are internally self timed and are initiated by the rising edge of the clock (K) input. Eight write enables are provided for byte write control.

The cache family is designed to interface with popular Pentium cache controllers with on board tag.

PD0 – PD2 are reserved for density identification.

- Pentium–style Burst Counter on Board
- Pipelined Data Out
- 160 Pin Card Edge Module
- Single 5 V ± 5% Power Supply
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Byte Parity
- Byte Write Capability
- Fast Module Clock Rates: 66 MHz
- Decoupling Capacitors for each Fast Static RAM
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- I/Os are 3.3 V Compatible
- Burndy Connector, Part Number: CELP2X80SC3Z48
- Series 20Ω Resistors for Noise Immunity

BurstRAM is a trademark of Motorola.
Pentium is a trademark of Intel Corp.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

PIN ASSIGNMENT
68–LEAD CARD EDGE MODULE
TOP VIEW

V_{SS}	81	1	V_{SS}
DQ63	82	2	DQ62
$V_{CC}5$	83	3	$V_{CC}3$*
DQ61	84	4	DQ60
$V_{CC}5$	85	5	$V_{CC}3$*
DQ59	86	6	DQ58
DQ57	87	7	DQ56
V_{SS}	88	8	V_{SS}
DQP7	89	9	DQP6
DQ55	90	10	DQ54
DQ53	91	11	DQ52
DQ51	92	12	DQ50
V_{SS}	93	13	V_{SS}
DQ49	94	14	DQ48
DQ47	95	15	DQ46
DQ45	96	16	DQ44
DQ43	97	17	DQ42
V_{SS}	98	18	V_{SS}
DQ41	99	19	DQ40
DQP5	100	20	DQP4
DQ39	101	21	DQ38
DQ37	102	22	DQ36
DQ35	103	23	DQ34
V_{SS}	104	24	V_{SS}
DQ33	105	25	DQ32
DQ31	106	26	DQ30
DQ29	107	27	DQ28
DQ27	108	28	DQ26
DQ25	109	29	DQ24
V_{SS}	110	30	V_{SS}
DQP3	111	31	DQP2
DQ23	112	32	DQ22
DQ21	113	33	DQ20
$V_{CC}5$	114	34	$V_{CC}3$*
DQ19	115	35	DQ18
V_{SS}	116	36	V_{SS}
DQ17	117	37	DQ16
$V_{CC}5$	118	38	$V_{CC}3$*
DQ15	119	39	DQ14
DQ13	120	40	DQ12
V_{SS}	121	41	V_{SS}
DQ11	122	42	DQ10
$V_{CC}5$	123	43	$V_{CC}3$*
DQ9	124	44	DQ8
DQP1	125	45	DQP0
$V_{CC}5$	126	46	$V_{CC}3$*
DQ7	127	47	DQ6
DQ5	128	48	DQ4
DQ3	129	49	DQ2
DQ1	130	50	DQ0
V_{SS}	131	51	V_{SS}
A3B	132	52	A3A
A4B	133	53	A4A
A5B	134	54	A5A
A6B	135	55	A6A
A7	136	56	A8
V_{SS}	137	57	V_{SS}
A9	138	58	A10
A11	139	59	A12
A13	140	60	A14
A15	141	61	A16
A17	142	62	A18**
V_{SS}	143	63	V_{SS}
*A19	144	64	PD0
PD1	145	65	PD2
K0	146	66	K1
*K2	147	67	K3*
$\overline{V_{SS}}$	148	68	$\overline{V_{SS}}$
$\overline{WE7}$	149	69	$\overline{WE6}$
$\overline{WE5}$	150	70	$\overline{WE4}$
$\overline{WE3}$	151	71	$\overline{WE2}$
WE1	152	72	WE0
$\overline{V_{SS}}$	153	73	$\overline{V_{SS}}$
$\overline{ADSC1}$	154	74	$\overline{ADSC0}$
$\overline{E1}$	155	75	$\overline{E0}$
$\overline{ADV1}$	156	76	$\overline{ADV0}$
G1	157	77	G0
$\overline{V_{CC}5}$	158	78	$\overline{V_{CC}3}$*
ADSP1	159	79	ADSP0
V_{SS}	160	80	V_{SS}

PD2	PD1	PD0	Cache Size	Module
V_{SS}	V_{SS}	NC	256KB	72CF32SG
V_{SS}	V_{SS}	V_{SS}	512KB	72CF64SG

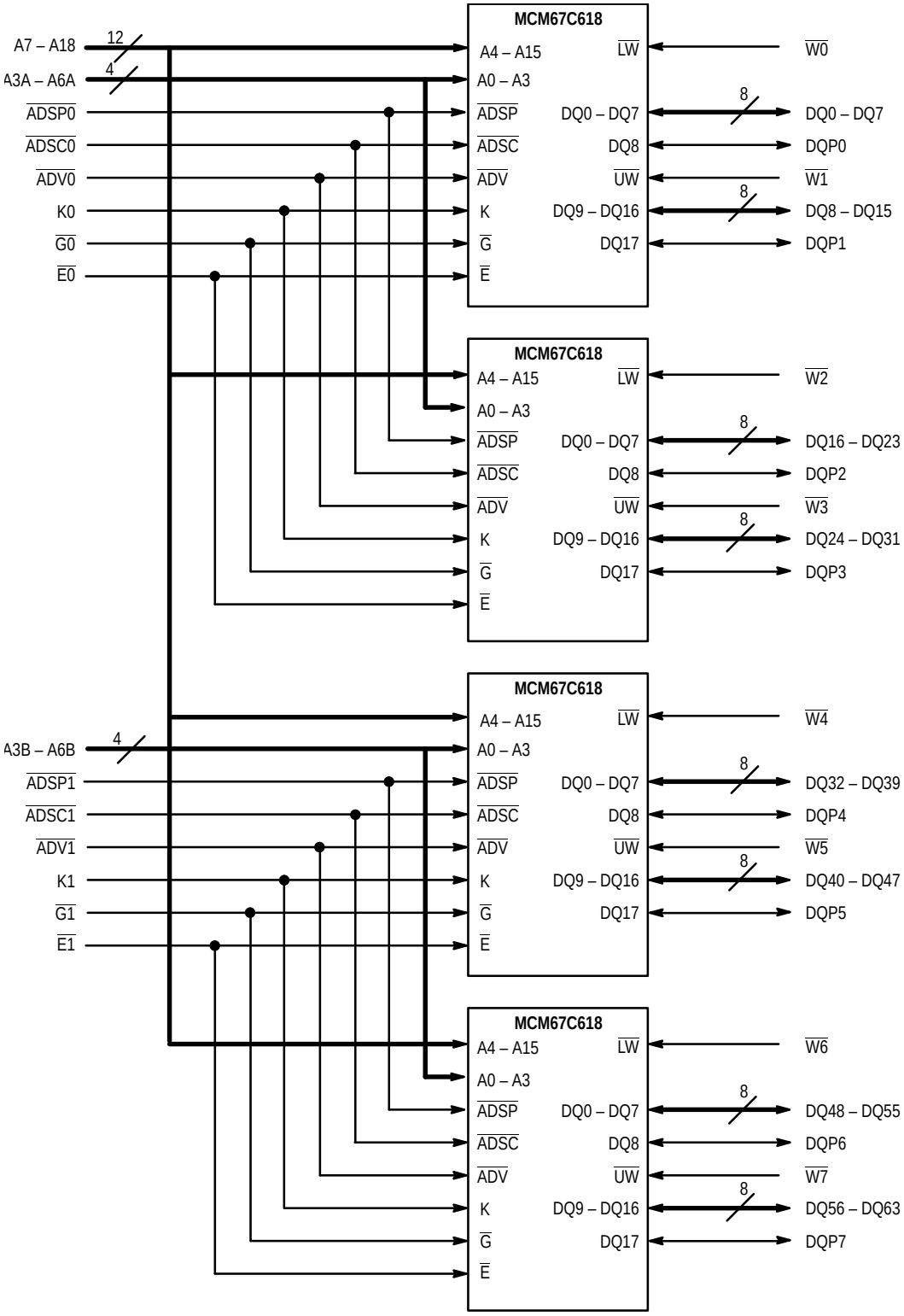
PIN NAMES

A3 – A18	Address Inputs
K0, K1	Clock
$\overline{W0}$ – $\overline{W7}$	Byte Write
$\overline{E0}$, $\overline{E1}$	Module Enable
$\overline{G0}$, $\overline{G1}$	Module Output Enable
DQ0 – DQ63	Cache Data Input/Output
DQP0 – DQP7	Data Parity Input/Output
$\overline{ADSC0}$, $\overline{ADSC1}$	Controller Address Status
$\overline{ADSP0}$, $\overline{ADSP1}$	Processor Address Status
$\overline{ADV0}$, $\overline{ADV1}$	Burst Advance
PD0 – PD2	Presence Detect
$V_{CC}5$	+ 5 V Power Supply
V_{SS}	Ground

* No Connect for MCM72CF32/MCM72CF64

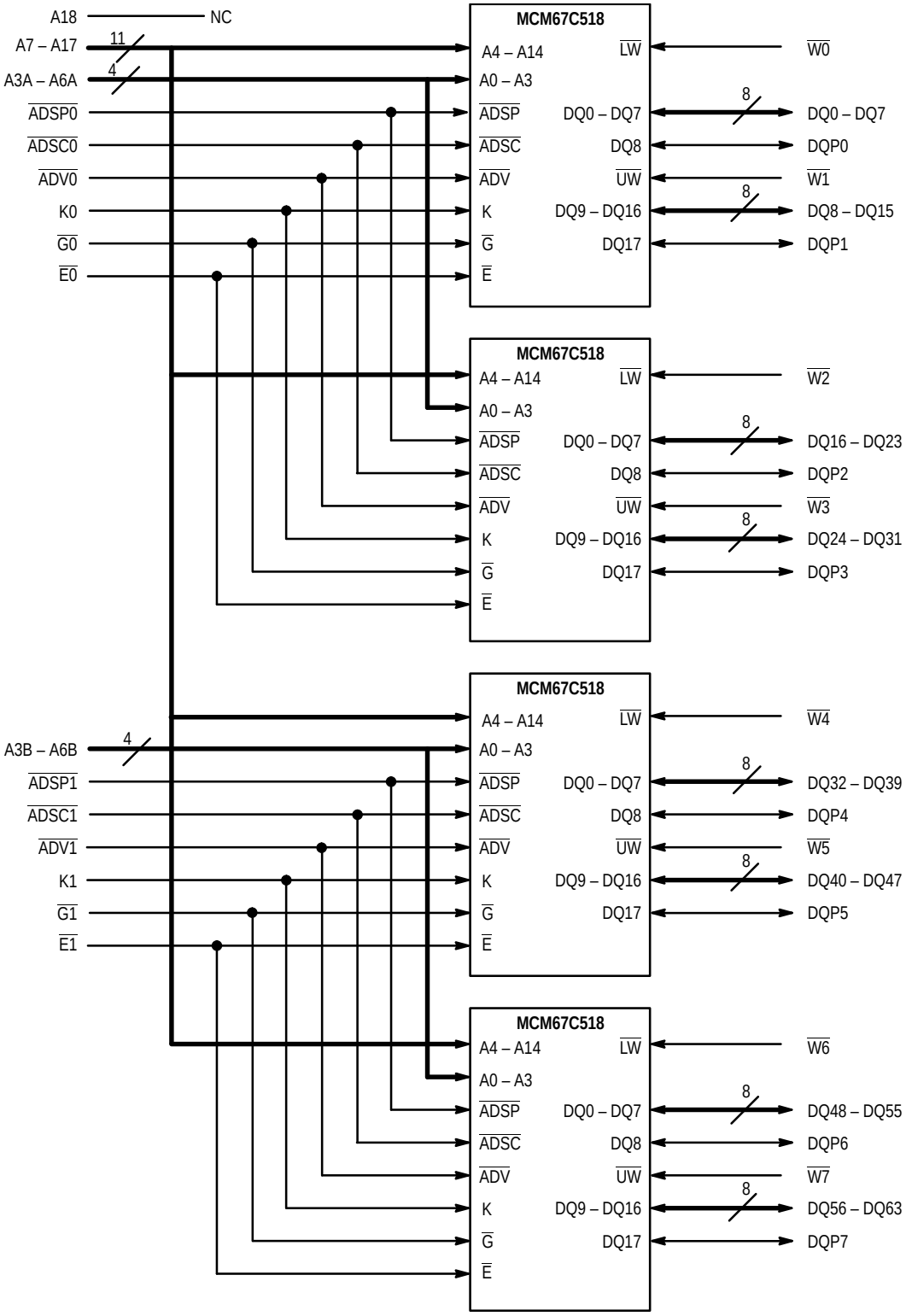
** No Connect for MCM72CF32

64K x 72 BurstRAM MEMORY MODULE BLOCK DIAGRAM



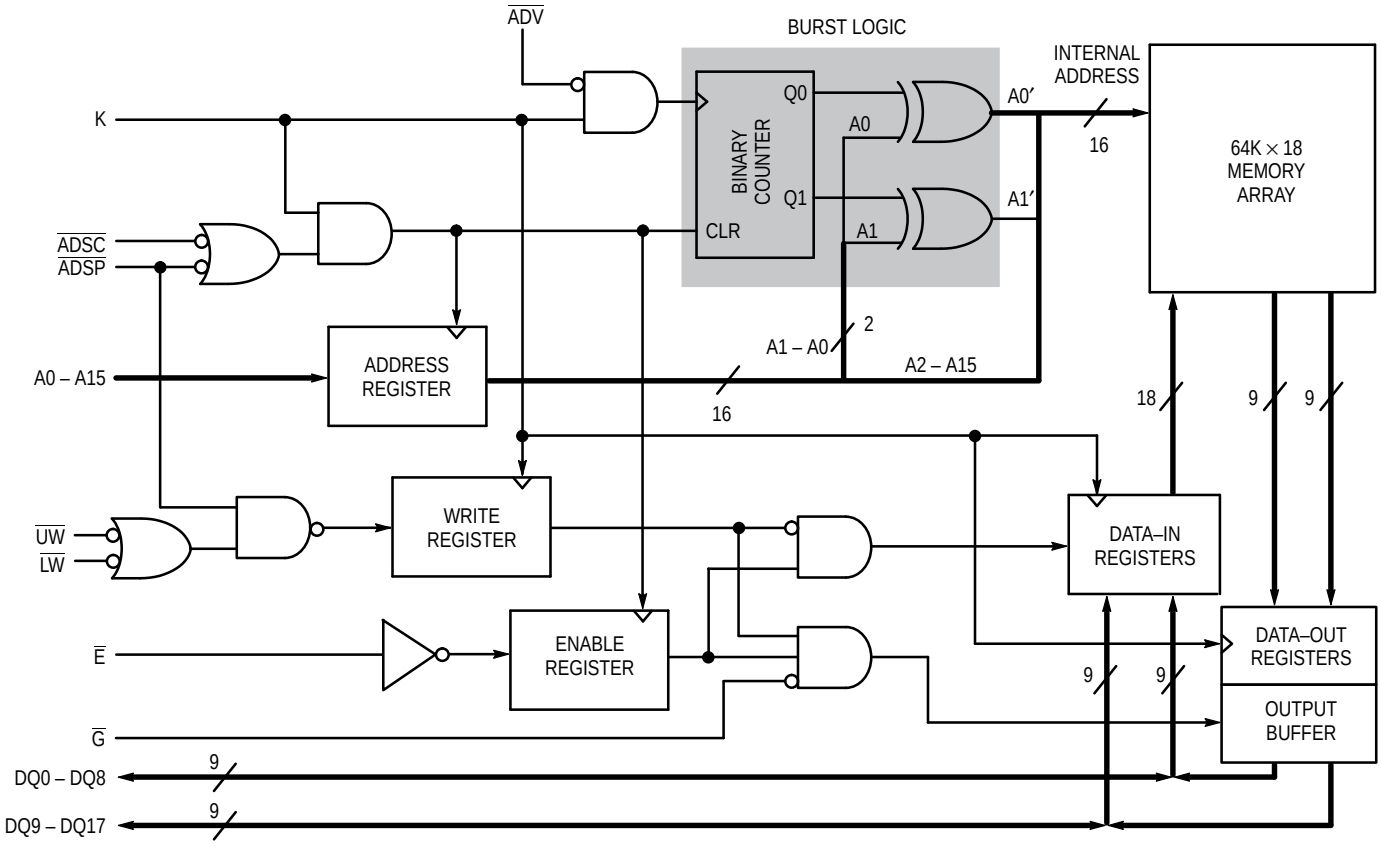
DQ 0–63 and DQP 0–7 are series terminated with 20Ω resistors.

32K x 72 BurstRAM MEMORY MODULE BLOCK DIAGRAM



DQ0–63 and DQP0–7 are series terminated with 20Ω resistors.

MCM67C618 BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{\text{ADSC}}$ or $\overline{\text{ADSP}}$ signals control the duration of the burst and the start of the next burst. When $\overline{\text{ADSP}}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{\text{W}}$ and $\overline{\text{ADSC}}$) is performed using the new external address. Alternatively, an $\overline{\text{ADSP}}$–initiated two cycle WRITE can be performed by asserting $\overline{\text{ADSP}}$ and a valid address on the first cycle, then negating both $\overline{\text{ADSP}}$ and $\overline{\text{ADSC}}$ and asserting $\overline{\text{LW}}$ and/or $\overline{\text{UW}}$ with valid data on the second cycle (see Single Write Cycle in WRITE CYCLES timing diagram).
When $\overline{\text{ADSC}}$ is sampled low (and $\overline{\text{ADSP}}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{\text{W}}$) is performed using the new external address. Chip enable ($\overline{\text{E}}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{\text{ADV}}$ controls subsequent burst cycles. When $\overline{\text{ADV}}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{\text{ADV}}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{\text{LW}}$, $\overline{\text{UW}}$).

BURST SEQUENCE TABLE (See Note)

External Address	A15 – A2	A1	A0
1st Burst Address	A15 – A2	A1	$\overline{\text{A0}}$
2nd Burst Address	A15 – A2	$\overline{\text{A1}}$	A0
3rd Burst Address	A15 – A2	$\overline{\text{A1}}$	$\overline{\text{A0}}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	L	X	X	X	L–H	N/A	Deselected
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	6.4	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA66}	—	1100	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	300	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Input Capacitance (A7 – A18)	C_{in}	20	pF
Input Capacitance (A3 – A6, $\overline{ADSPx}$, $\overline{ADSCx}$, $\overline{ADVx}$, Kx, $\overline{Gx}$, $\overline{Ex}$, $\overline{Wx}$)	C_{in}	10	pF
Input/Output Capacitance (DQ0 – DQ63, DQP0 – DQP7)	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

Output Timing Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM72CF64SG66		Unit	Notes
		Min	Max		
Cycle Time	t_{KHKH}	15	—	ns	
Clock Access Time	t_{KHQV}	—	9	ns	5
Output Enable to Output Valid	t_{GLQV}	—	6	ns	
Clock High to Output Active	t_{KHQX1}	2	—	ns	
Clock High to Output Change	t_{KHQX2}	2	—	ns	
Output Enable to Output Active	t_{GLQX}	1	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	2	6	ns	6
Clock High to Q High–Z	t_{KHQZ}	—	6	ns	
Clock High Pulse Width	t_{KHKL}	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	5	—	ns	
Setup Times: Address Address Status Data In Write Address Advance Chip Enable	t_{AVKH} t_{ADSVKH} t_{DVKH} t_{WVKH} t_{ADVVKH} t_{EVKH}	2.5	—	ns	7
Hold Times: Address Address Status Data In Write Address Advance Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHADVX} t_{KHEX}	0.5	—	ns	7

NOTES:
1. In setup and hold time W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible Pentium external bus cycles.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled.Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

AC TEST LOADS

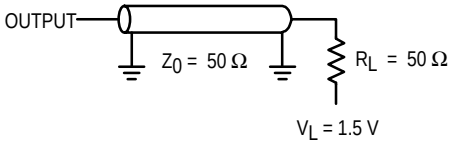


Figure 1A

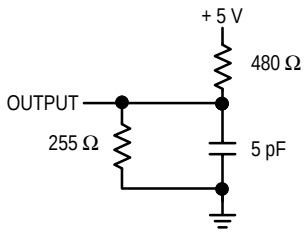
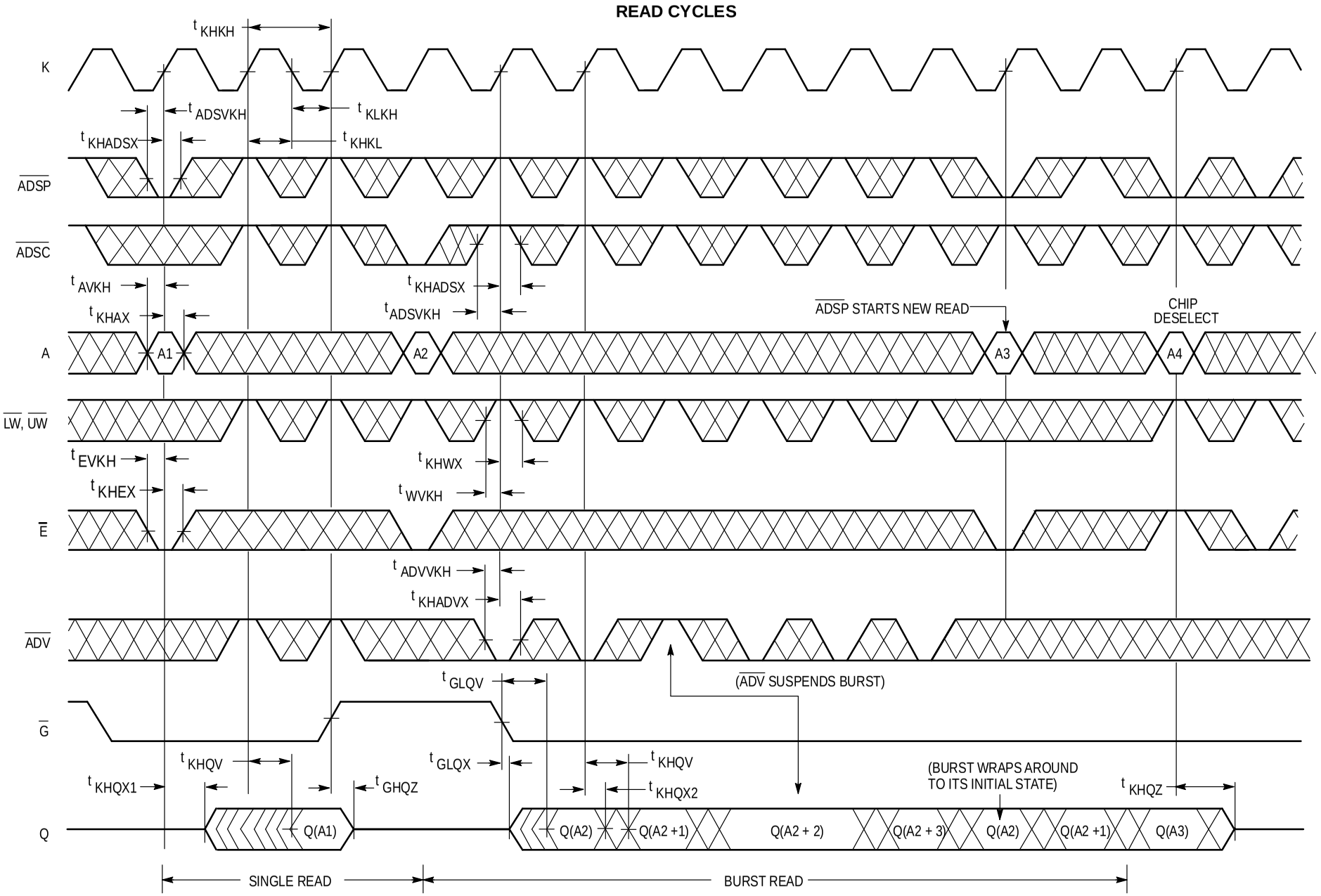
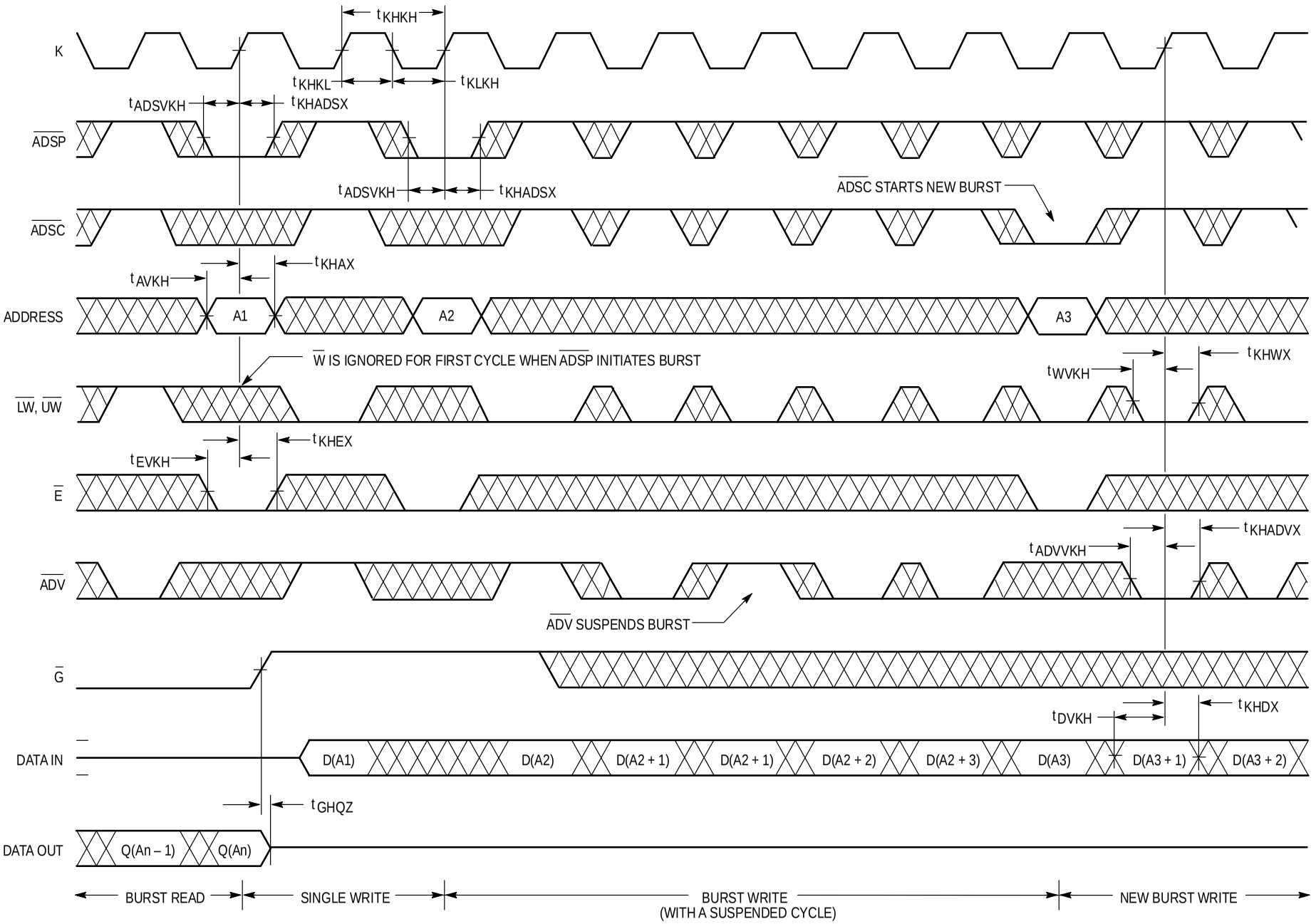


Figure 1B

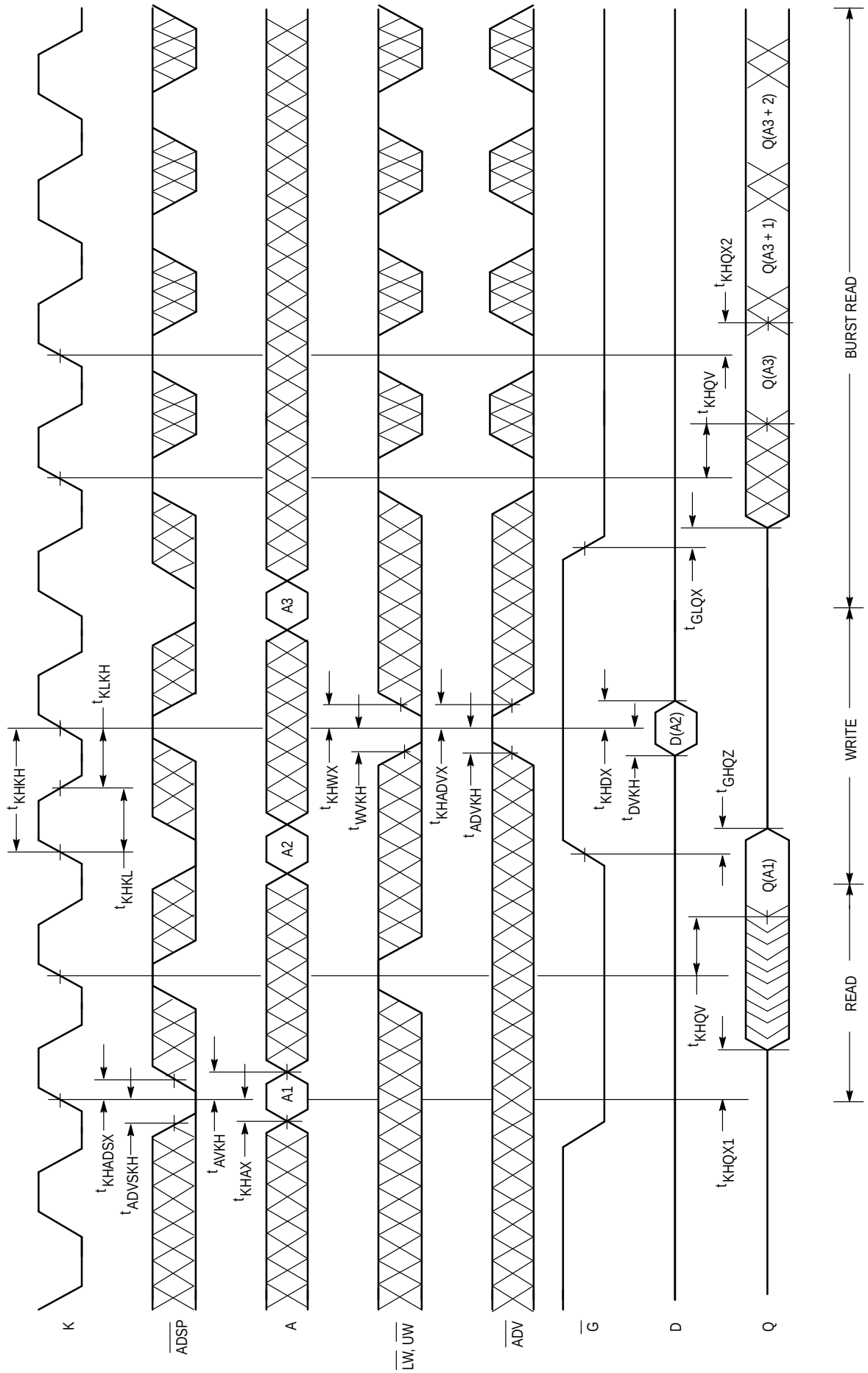
READ CYCLES


tKHKH
K
tADSVKH
tKLKH
tKHADSX
tKHKL
ADSP
ADSC
tAVKH
tKHADSX
tKHAX
tADSVKH
ADSP STARTS NEW READ
CHIP DESELECT
A
A1
A2
A3
A4
LW, UW
tEVKH
tKHWX
tKHEX
tWVKH
E
tADVVKH
tKHADVX
ADV
(ADV SUSPENDS BURST)
tGLQV
G
tKHQV
tGLQX
tKHQV
tKHQX1
tGHQZ
tKHQX2
(BURST WRAPS AROUND TO ITS INITIAL STATE)
tKHQZ
Q
Q(A1)
Q(A2)
Q(A2 +1)
Q(A2 + 2)
Q(A2 + 3)
Q(A2)
Q(A2 +1)
Q(A3)
SINGLE READ
BURST READ

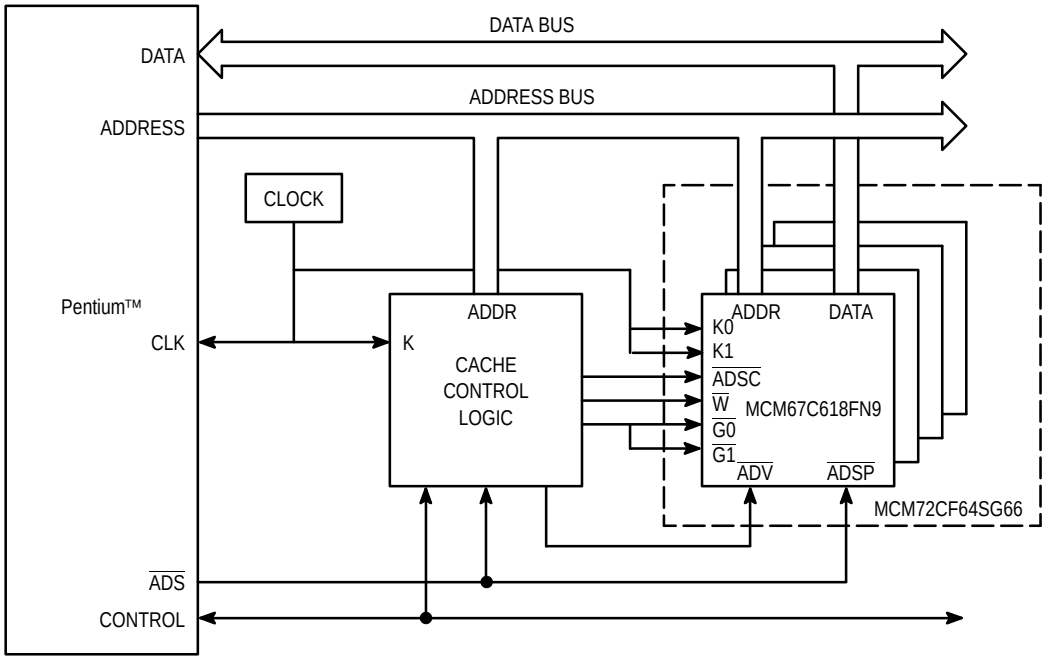
WRITE CYCLES



COMBINATION READ/WRITE CYCLES ($\overline{E}$ low, $\overline{ADSC}$ high)



APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache
Using MCM72CF64SG66 with a 66 MHz Pentium

Figure 2

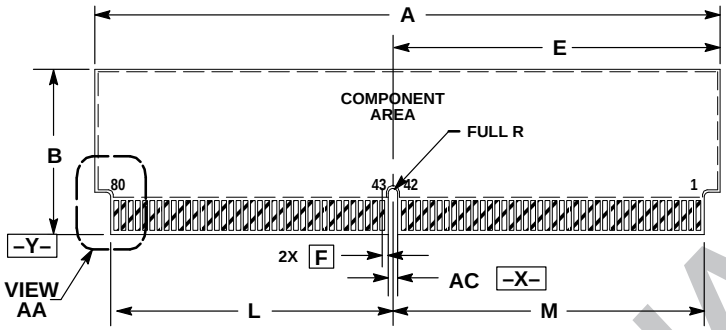
ORDERING INFORMATION
(Order by Full Part Number)

	MCM	72CF32 72CF64	XX	XX	
Motorola Memory Prefix					Speed (66 = 66 MHz)
Part Number					Package (SG = Gold Pad SIMM)

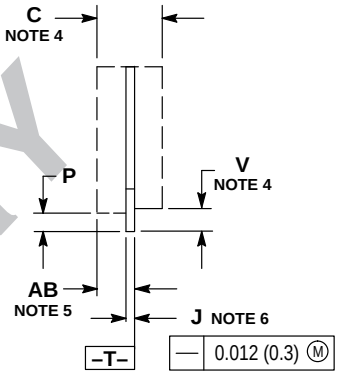
Full Part Numbers — MCM72CF32SG66
MCM72CF64SG66

PACKAGE DIMENSIONS

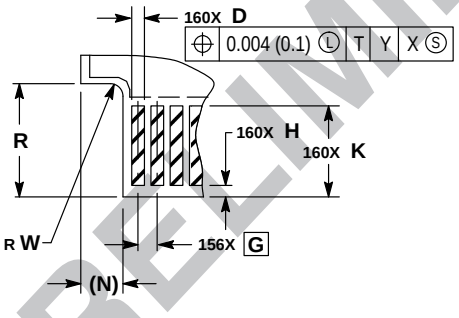
160–LEAD
CARD EDGE MODULE
CASE 1113A–01



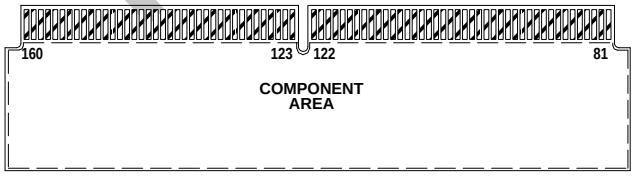
FRONT VIEW



SIDE VIEW



VIEW AA



BACK VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALLIZATION.
4. DIMENSIONS C AND V DEFINE A DOUBLE–SIDED MODULE.
5. DIMENSION AB DEFINES OPTIONAL SINGLE–SIDED MODULE.
6. STRAIGHTNESS CALLOUT APPLIES TO TAB AREA ONLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	4.330	4.350	109.98	110.49
B	1.270	1.310	32.26	33.27
C	—	0.454	—	11.53
D	0.033	0.037	0.84	0.94
E	2.265	2.275	57.53	57.79
F	0.075 BSC		1.91 BSC	
G	0.050 BSC		1.27 BSC	
H	—	0.030	—	0.51
J	0.055	0.069	1.40	1.75
K	0.210	—	5.33	—
L	1.955	1.965	49.66	49.91
M	2.155	2.165	54.74	54.99
N	0.110 REF		2.79 REF	
P	0.125	—	3.18	—
R	0.285	0.305	7.24	7.75
V	0.157	—	3.99	—
W	0.040	0.060	1.02	1.52
AB	—	0.262	—	6.66
AC	0.072	0.076	1.83	1.93

Literature Distribution Centers:
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ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.