DAC YF

A Truly "no man in the loop" Open-Source Idea to Layout SoC Workflow

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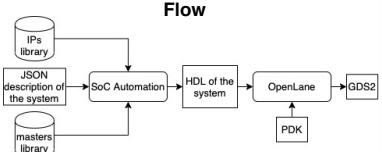
Introduction

This tool automates SoC design through taking in a JSON description of the system and generating Verilog HDL for the and its GDS2

Motivation

- Facilitating SoC design for everyone
- Reducing time to fabrication
- Making use of the common features among different SoC designs (IPs, bus protocols, hierarchy, …)

Flow

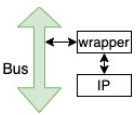


Libraries

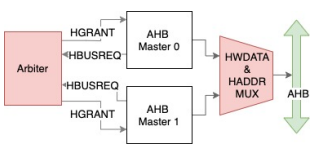
- IPs library contains JSON descriptions for verified open-source IPs
- Masters library contains JSON descriptions for Arm Cortex M0, Arm Cortex M3 and N5 (open-source core)

Supported Features

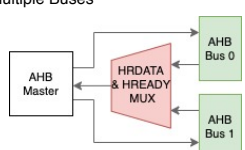
1) Non-AHB/APB IPs



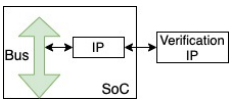
2) Multiple Masters



3) Multiple Buses



4) Verification IPs



Configurable Options

- Width of address line
- Number and types of masters/peripherals
- Number of AHB/APB buses
- Base addresses of peripherals, systems and subsystems
- External connections of peripherals

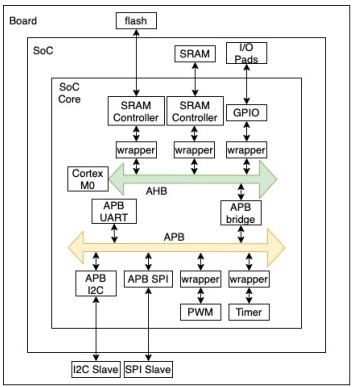
Testing

- Auto-generation of a dummy master
- Auto-generation of self-checking testbench
- The system in the example has been tested using CM0, CM3 and N5, without human intervention.

GitHub

SCAN ME

A Generated System



Work In Progress

- Integration with OpenLane
- Creating a library for technology-specific components (e.g. I/O pads)
- Supporting masters that aren't bus specific
- Supporting more bus protocols
- FPGA Validation
- Auto-generation of datasheet