BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI

I SEMESTER 2024-25, MEL G621 – VLSI DESIGN

LAB ASSIGNMENT – 5

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AIM: To construct the schematics of CMOS NAND and NOR gates with appropriate sizing and find:

i. The critical points and hence the noise margins from Voltage transfer characteristics curve for various input combinations.
ii. The propagation delays t_{pHL}, t_{pLH} and t_p for various input combinations

Tools used: Cadence Virtuoso

1. CMOS NAND Gate

The CMOS NAND gate is implemented using 4 transistors, 2 P-MOSFETs in series and 2 N-MOSFETs in parallel. The NAND gate is appropriately sized for symmetric operation. Intermediate capacitance of 100 fF and output capacitance of 200 fF are placed.

nMOS parameters

Model name – nch

Length of transistor = 180nm

Width of transistor = 220nm

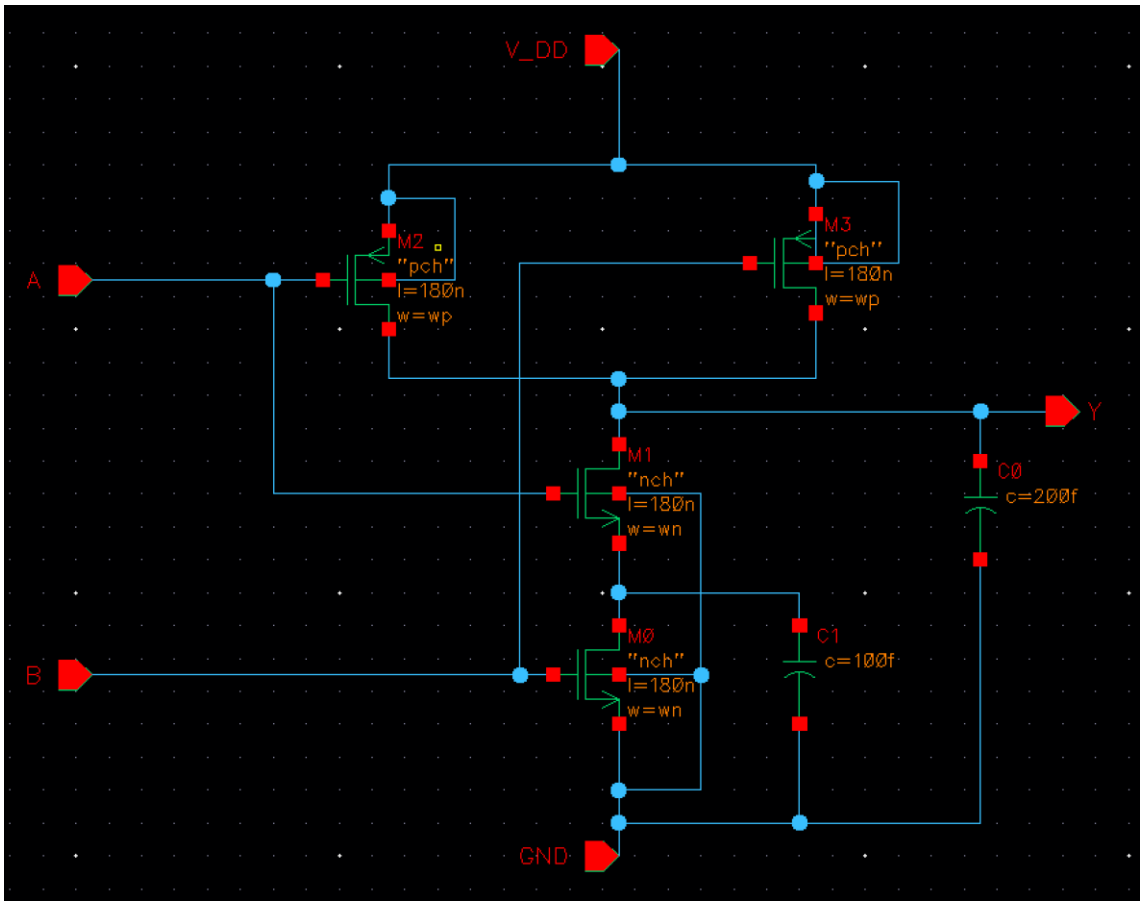
pMOS parameters

Model name - pch

Length of transistor = 180nm

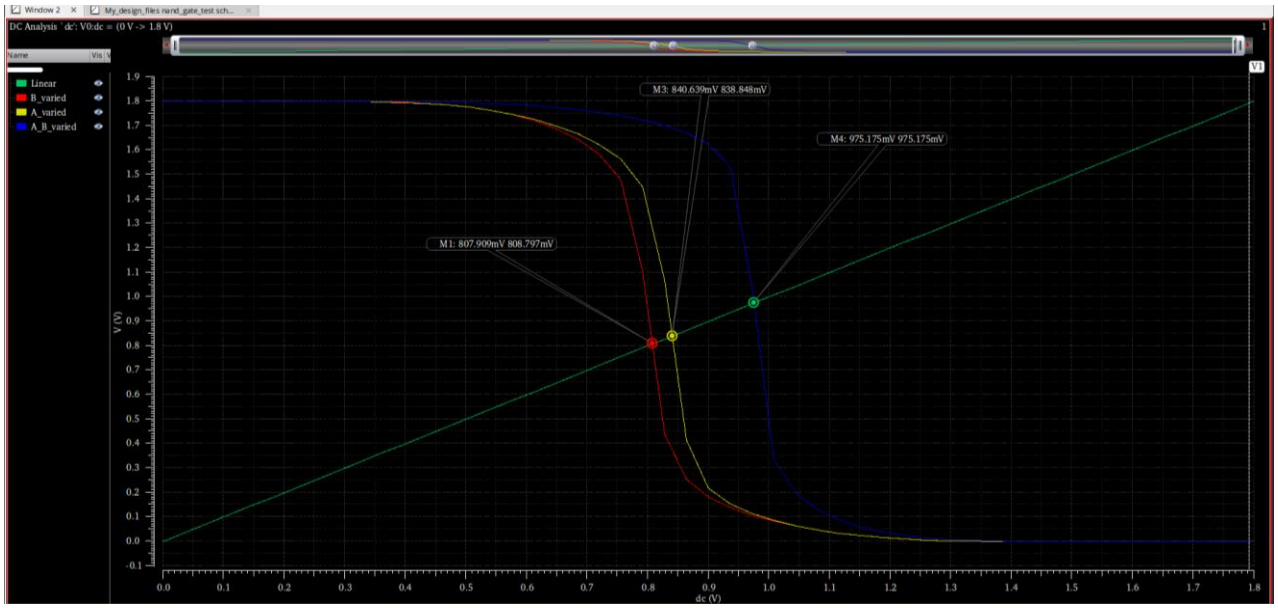
Width of transistor = 599.5nm

Circuit schematic of NAND Gate



i. Voltage transfer characteristics of NAND Gate

Due to multiple input combinations associated with 2-inputs, transistors are in different regions of operations. Thus for 3 input combinations, we get 3 voltage transfer characteristics.

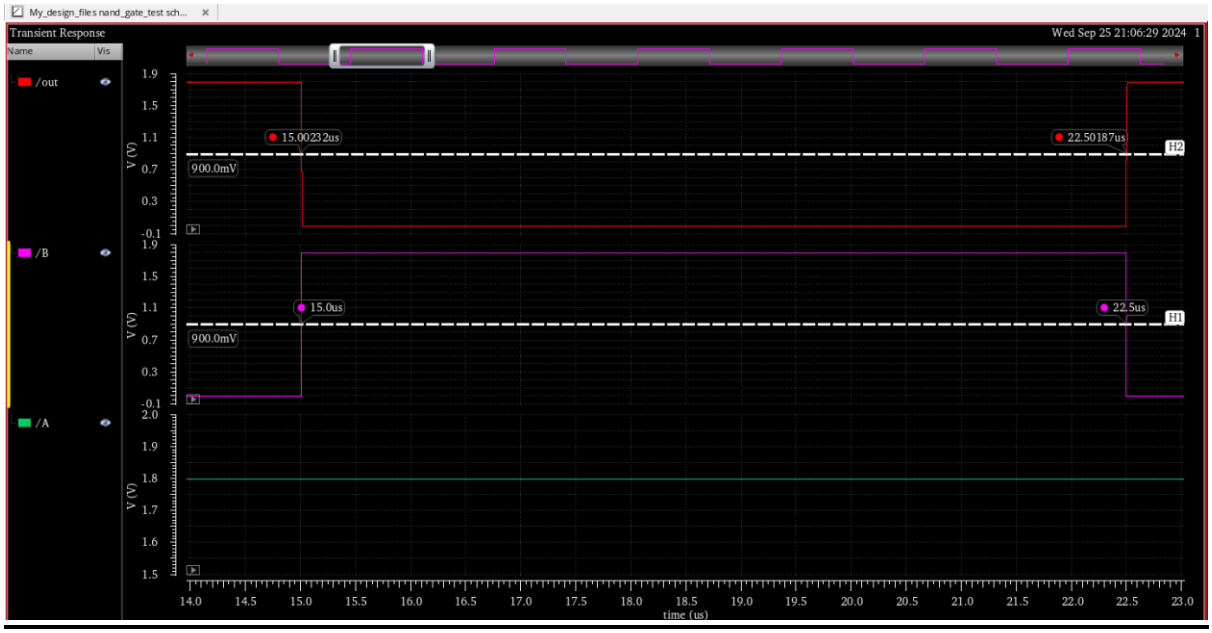


The critical points, switching thresholds and noise margins are tabulated below.

Inputs	V_{OH}	V_{OL}	V_{IL}	V_{IH}	V_{TH}	V_{NMH}	V_{NML}
A=B=0to1	1.8V	49nV	658.85m	959.9m	975.1m	658.85m	840.1m
A=1, B=0to1	1.8V	49nV	658.85m	959.9m	807.9m	658.85m	840.1m
B=1, A=0to1	1.8V	49nV	694.53m	981.99m	840.64m	694.53m	818.002m

ii. Transient analysis of NAND Gate:

Transient analysis was performed to calculate the propagation delays for the various input cases. The below waveform is for case-2.



The propagation delays for the other cases are tabulated below.

Inputs	**t_{pLH}**	**t_{pHL}**	**t_p**
A=B=0to1	0.69 ns	1.58 ns	1.135 ns
A=1, B=0to1	1.87 ns	2.33 ns	2.1 ns
B=1, A=0to1	1.37 ns	1.58 ns	1.475 ns

2. CMOS NOR Gate

The CMOS NOR gate is implemented using 4 transistors, 2 P-MOSFETs in series and 2 N-MOSFETs in parallel. The NOR gate is appropriately sized for symmetric operation. Intermediate capacitance of 100 fF and output capacitance of 200 fF are placed.

nMOS parameters

Length of transistor = 180nm

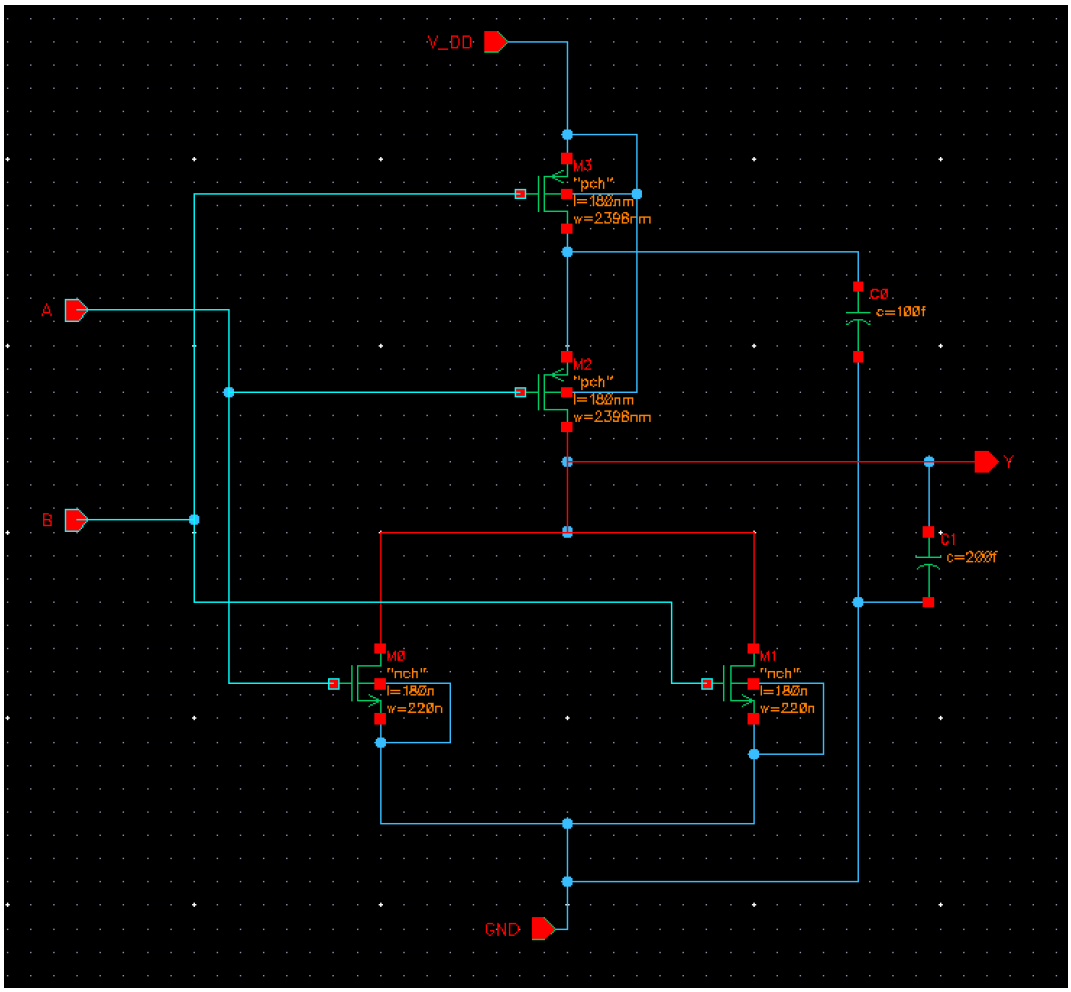
Width of transistor = 220nm

pMOS parameters

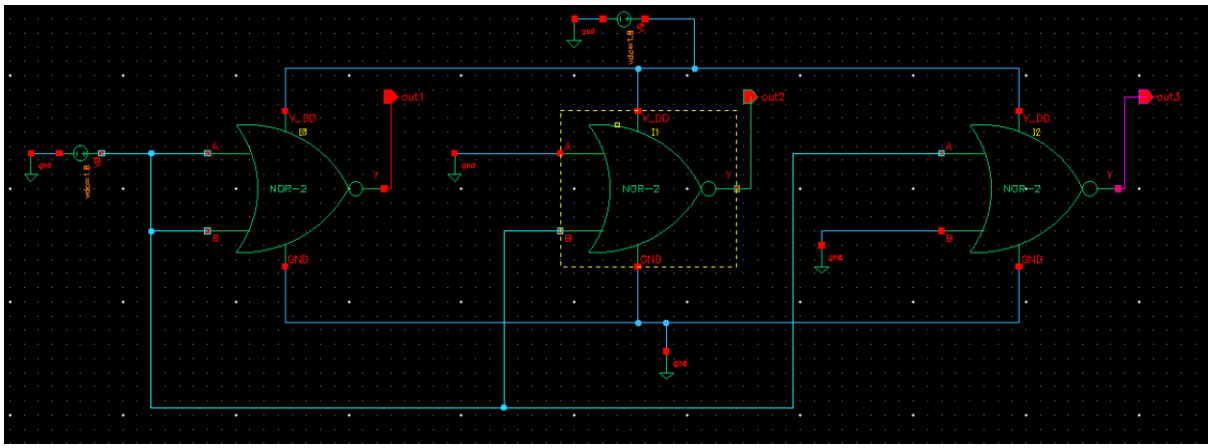
Length of transistor = 180nm

Width of transistor = 2398nm

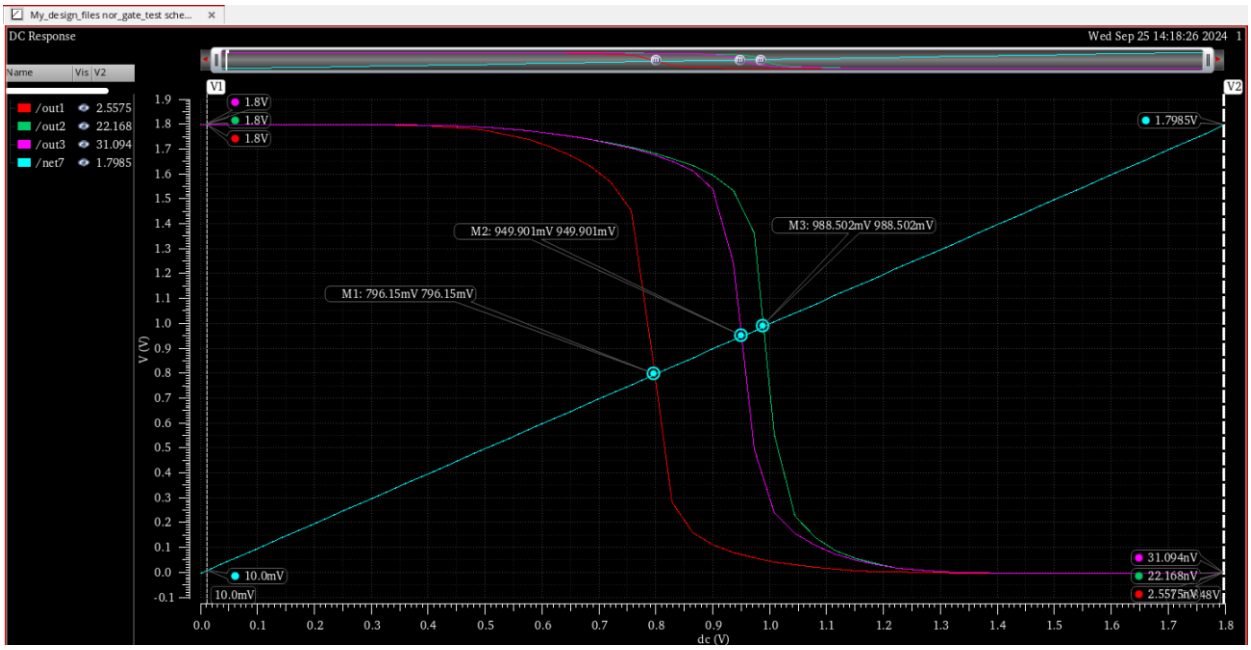
Circuit Schematic of NOR gate



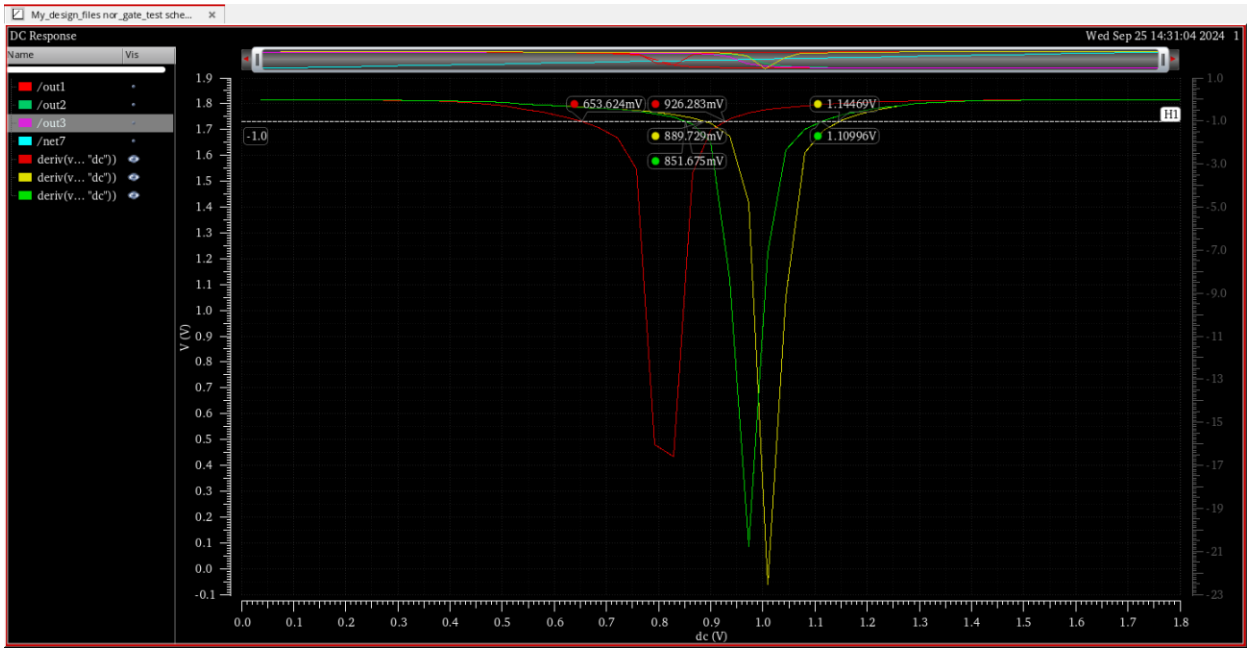
i. Voltage transfer characteristics of NOR Gate



Due to multiple input combinations associated with 2-inputs, transistors are in different regions of operations. Thus for 3 input combinations, we get 3 voltage transfer characteristics.



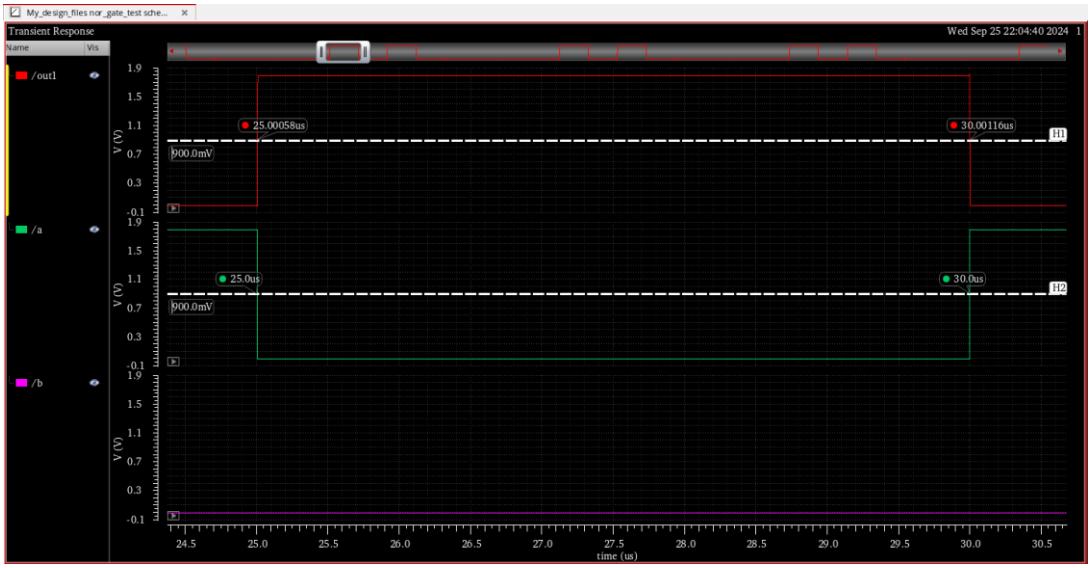
V_{IL} and V_{IH} are found by taking the derivative of the respective VTCs and finding the points where slope = -1. The derivative curves are shown below.



Inputs	V_{OH}	V_{OL}	V_{IL}(mV)	V_{IH}(mV)	V_{TH}(mV)	V_{NMH}(mV)	V_{NML}(mV)
A=B= 0to1	1.8V	2.55nV	653.624	926.283	796.15	873.717	653.624
A=0, B=0to1	1.8V	22.16nV	889.729	1144.69	988.5	655.31	889.729
B=0, A=0to1	1.8V	31.04nV	851.67	1109.96	949.901	690.04	851.67

ii. Transient analysis of NOR Gate

Transient analysis was performed to calculate the propagation delays for the various input cases. The below waveform is for case-2.



The propagation delays for the other cases are tabulated below.

Inputs	$\mathbf{t_{pLH}}$	$\mathbf{t_{pHL}}$	$\mathbf{t_p}$
A=B=0to1	0.58 ns	0.58 ns	0.58 ns
A=0, B=0to1	0.83 ns	1.66 ns	1.245 ns
B=0, A=0to1	0.58 ns	1.169 ns	0.8745 ns