BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI

I SEMESTER 2024-25, MEL G621 – VLSI DESIGN

LAB ASSIGNMENT – 2

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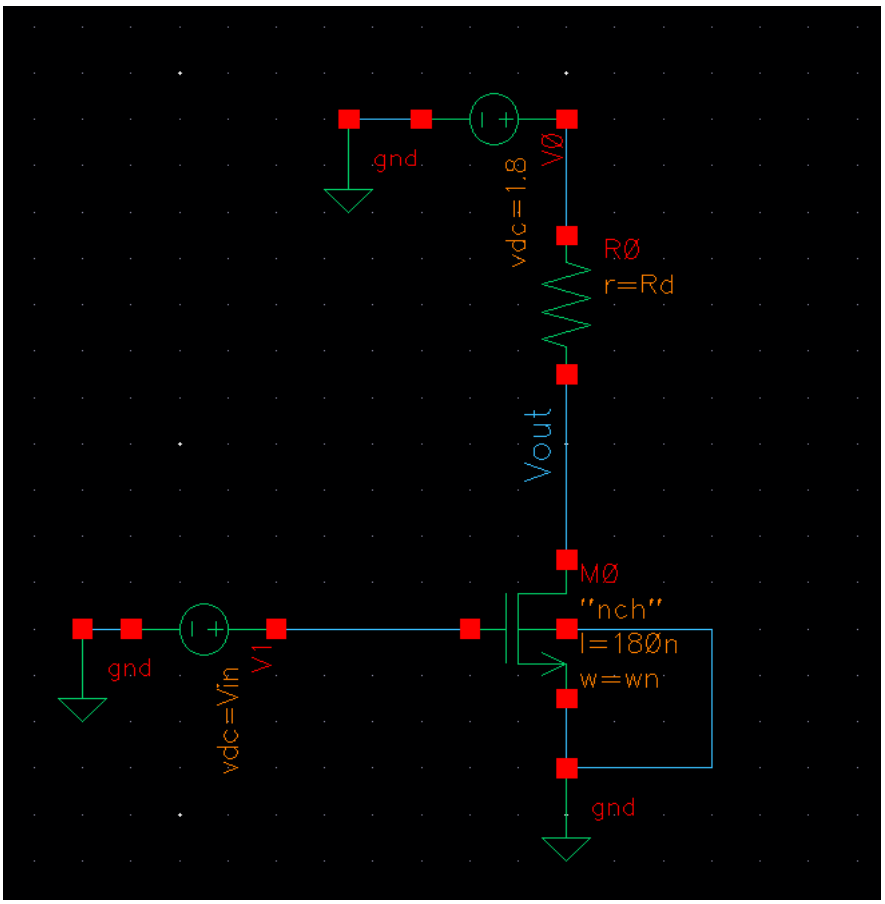
AIM: To draw the schematic of resistive load inverter and plot its Voltage Transfer Characteristics (VTC) for varying transistor width and load resistance.

Tools used: Cadence Virtuoso

Circuit Schematic:

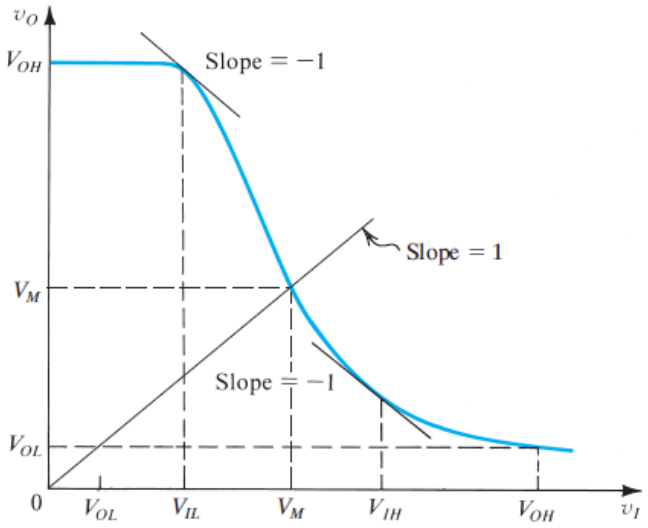


VOLTAGE TRANSFER CHARACTERISTICS:

A typical VTC plot for a resistive inverter is shown below with clearly marked critical points. Noise margins were calculated using the formula:

$$NM_L = V_{OH} - V_{IH}$$

$$NM_H = V_{IL} - V_{OL}$$



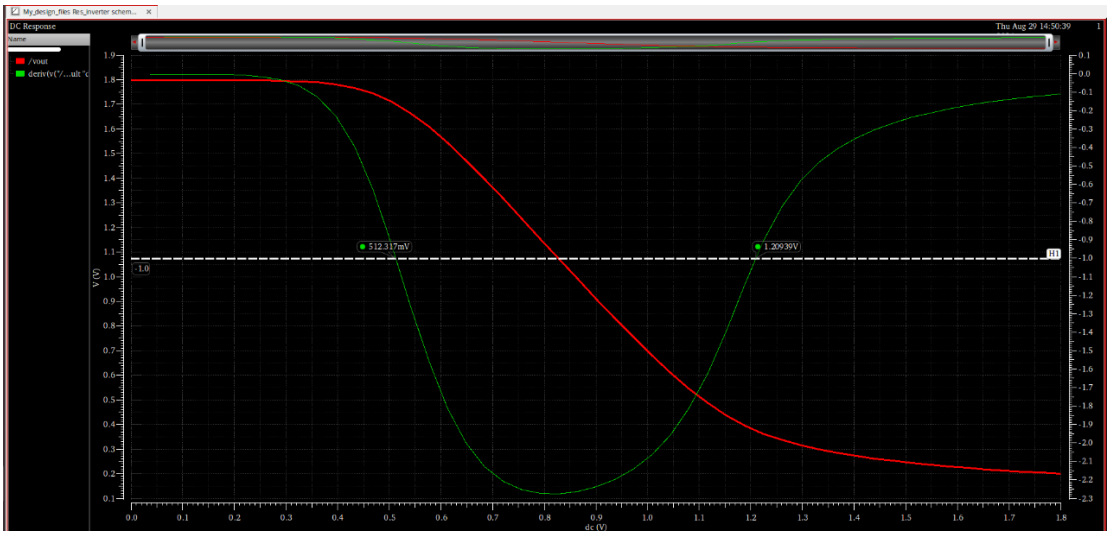
NMOS Transistor parameters:

Model name –'nch'; Transistor width = 220nm; Transistor length = 180nm

Load resistance = 20kΩ

1. Voltage transfer characteristics

VTC is plotted by measuring changes in V_{out} as V_{in} is swept from 0 to 1.8V.

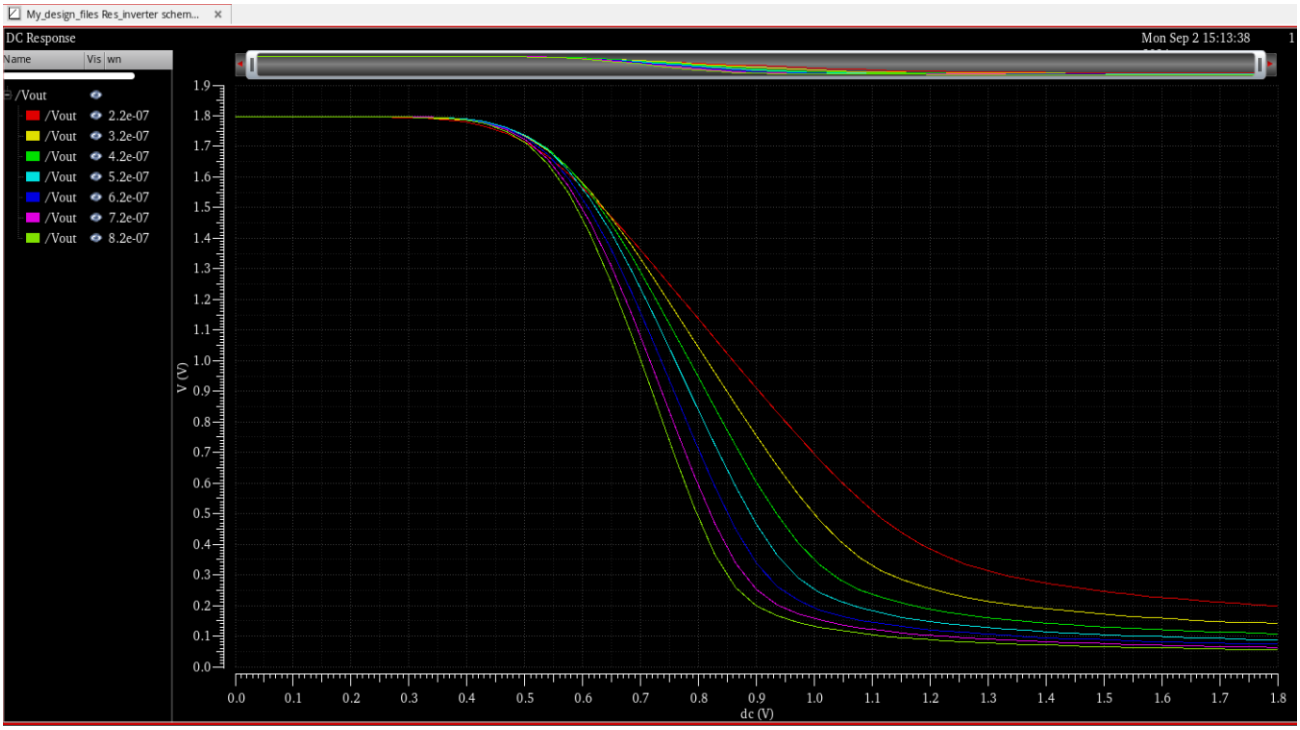


Derivative of the curve is plotted (in green above) using ‘deriv’ function to get the slope of VTC. V_{IL} and V_{IH} were marked where slope of the curve was ‘-1’. Corresponding V_{OL} and V_{OH} were found.

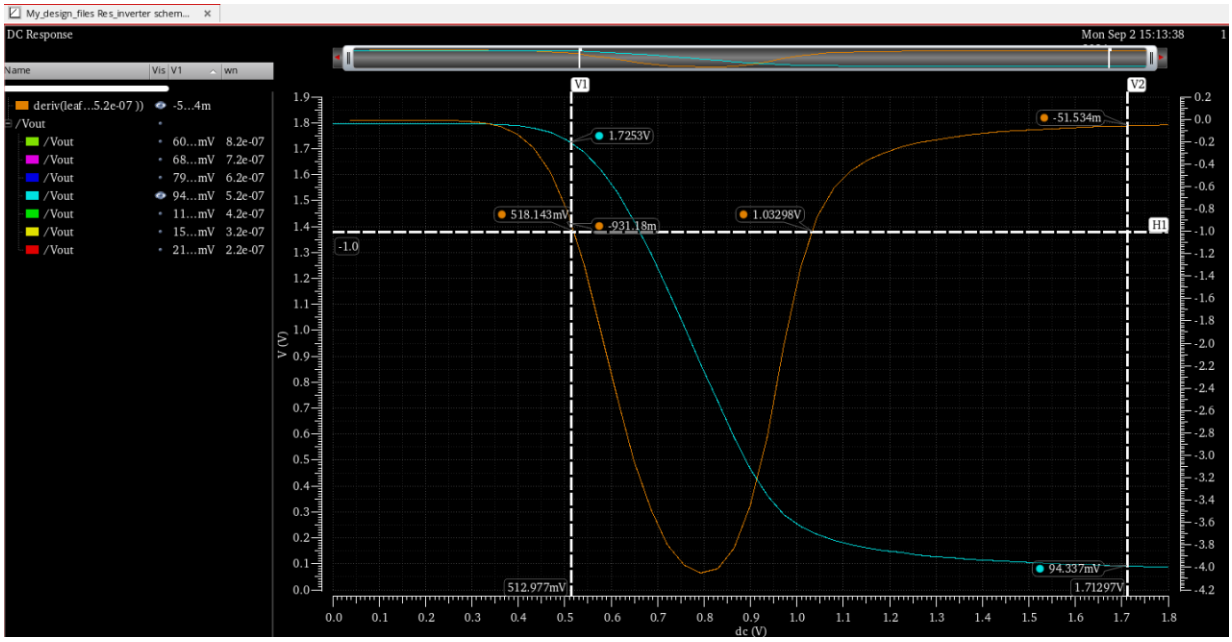
V_{IL}	V_{IH}	V_{OL}	V_{OH}	NM_L	NM_H
512.32mV	1.2093V	202.41mV	1.8V	309.91m	590.7mV

2. VTC with varying transistor width ‘w_n’

Parametric analysis was performed by sweeping V_{in} for different values of w_n to observe the critical points and noise margins.



Below plot shows the critical points for w_n = 520nm.

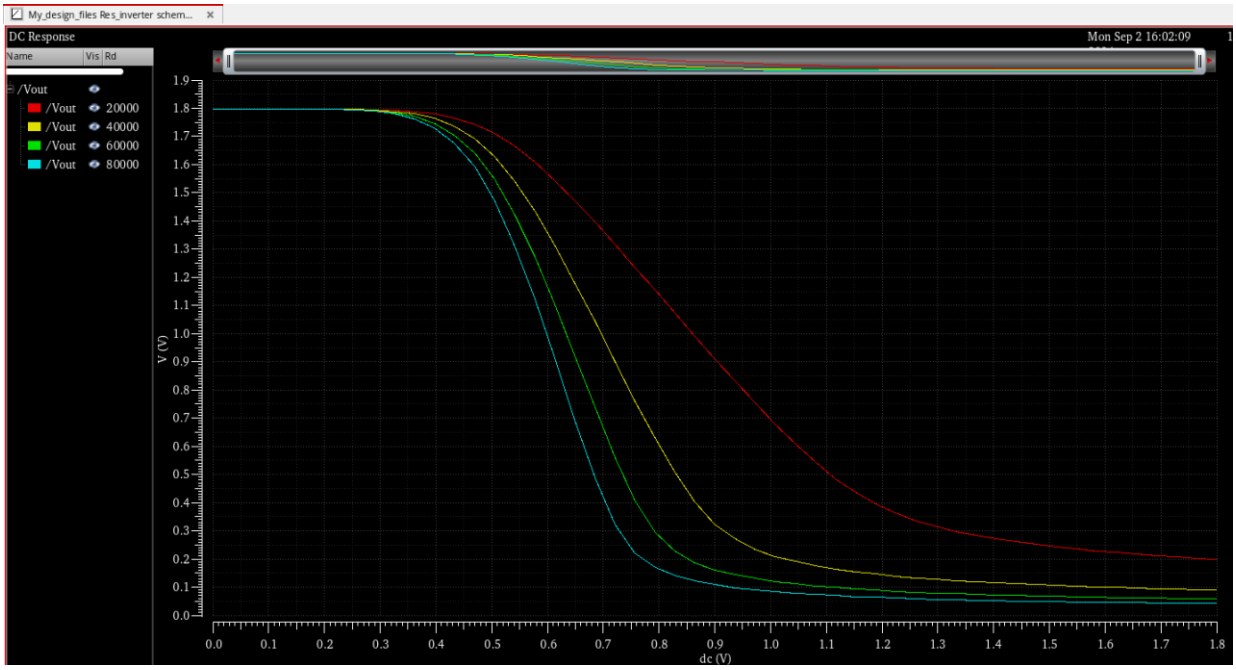


The below table shows the critical points and noise margins for all plots of w_n.

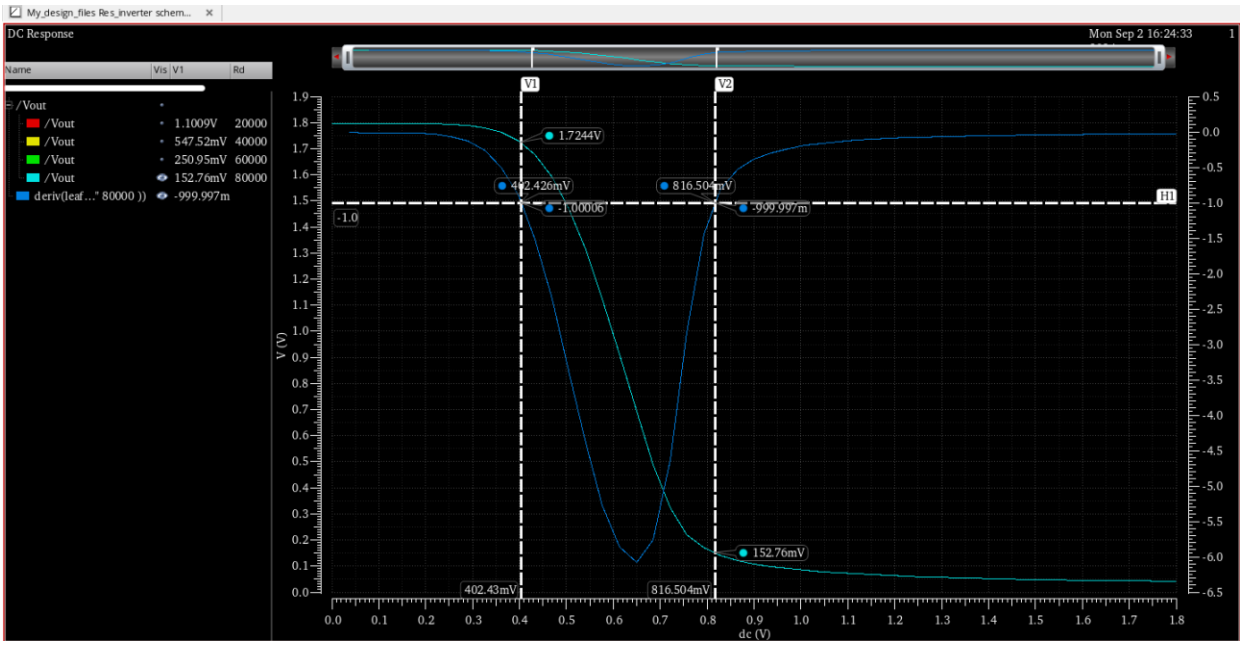
W_n(nm)	V_{IL}(V)	V_{IH}(V)	V_{OL}(V)	V_{OH}(V)	NM_L(V)	NM_H(V)
220	512.32m	1.2093	202.41m	1.8	309.91m	0.5907
320	512.732m	1.1324	143.62m	1.8	369.11m	0.6676
420	522.166m	1.0755	110.97m	1.8	411.2m	0.7245
520	518.143m	1.0329	90.406m	1.8	427.74m	0.7671
620	508.667m	0.9927	76.44m	1.8	432.23m	0.8073
720	500.535m	0.9605	66.22m	1.8	434.32m	0.8395
820	492.694m	0.9323	58.41m	1.8	434.28m	0.8677

3. VTC with varying load resistance 'R_d'

Parametric analysis was performed by plotting V_{out} vs V_{in} for different values of load resistance to observe the critical points and noise margins.



Below plot shows the critical points for $R_d = 80k\Omega$.



The below table shows the critical points and noise margins for all plots of R_d.

$R_d(k\Omega)$	$V_{IL}(V)$	$V_{IH}(V)$	$V_{OL}(V)$	V_{OH} (V)	$NM_H(V)$	$NM_L(V)$
20	512.317m	1.2094	202.41	1.8	0.5906	309.91m
40	449.959m	971.166m	93.768	1.8	0.8289	356.19m
60	420.97m	872.67m	60.915	1.8	0.928	360.06m
80	402.43m	816.504m	45.098	1.8	0.984	357.33m

Inference:

The critical points and noise margins for varying load resistance and transistor width were calculated. From the tabulations, we observe that:

i. As w_n is increased, the VTC curve starts shifting to the left, i.e., the NMOS transistor's strength increases. This matches with the increase in transistor current as w_n increases.
ii. As R_d 5is increased, the VTC curve starts shifting to the left.