BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI

I SEMESTER 2024-25, MEL G621 – VLSI DESIGN

LAB ASSIGNMENT – 1

Name: Arun R V **ID No: 2024H1230173P**

AIM: To simulate the input and output characteristics of NMOS and PMOS

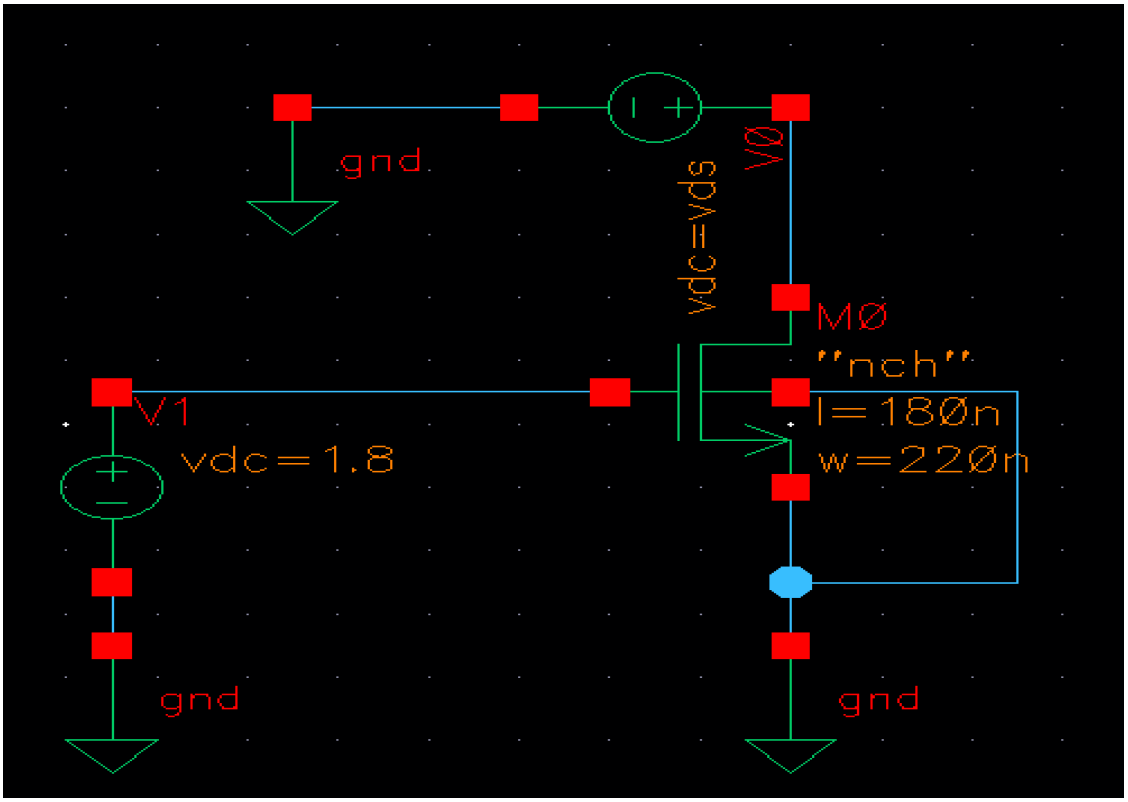
Tools used: Cadence Virtuoso

1. N-MOSFET

Model name: nch

Width of NMOS: 220nm

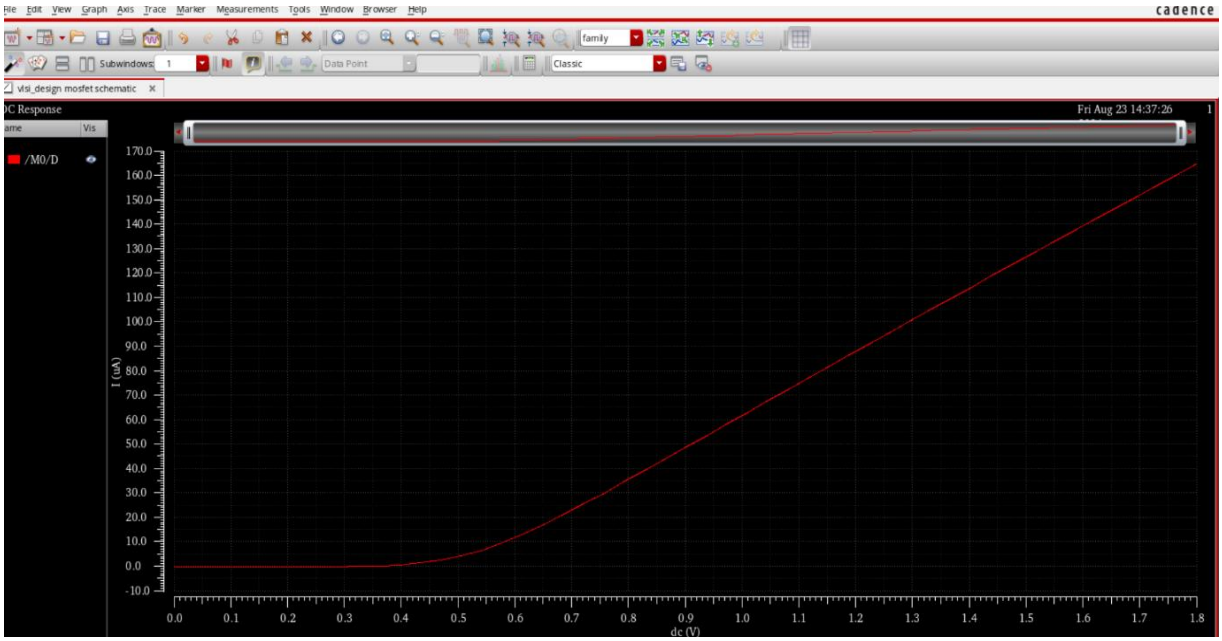
Length of NMOS: 180nm



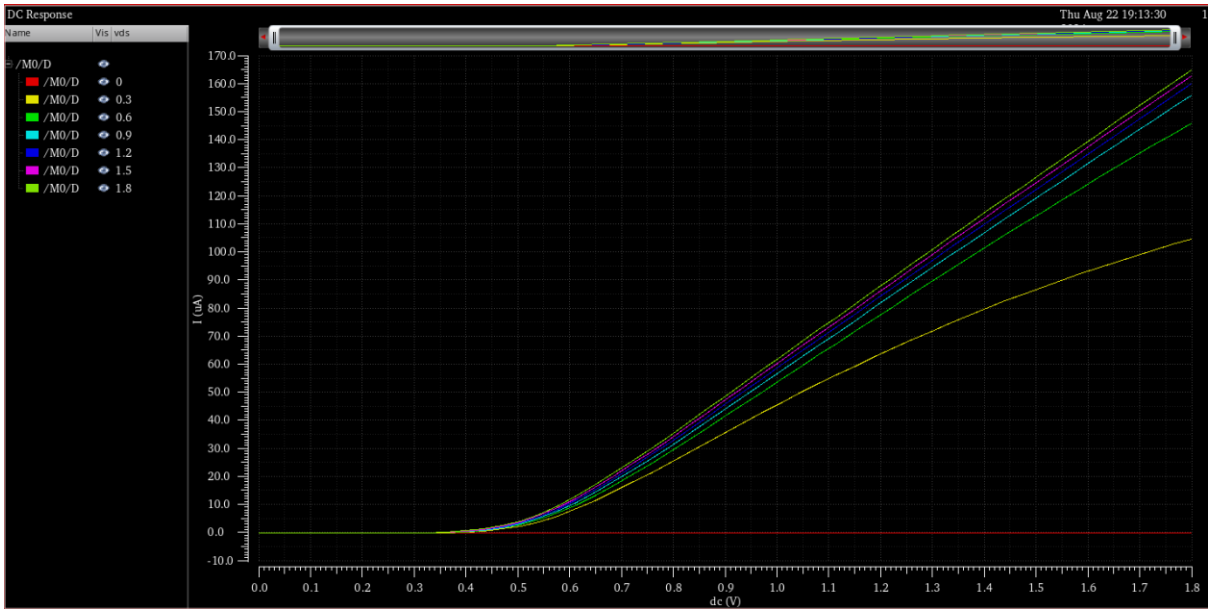
Schematic of NMOS

Input characteristics:

Firstly, we plot drain current I_d vs V_{gs}, taking V_{ds} = 1.8V and sweeping V_{gs} 0 to 1.8V.



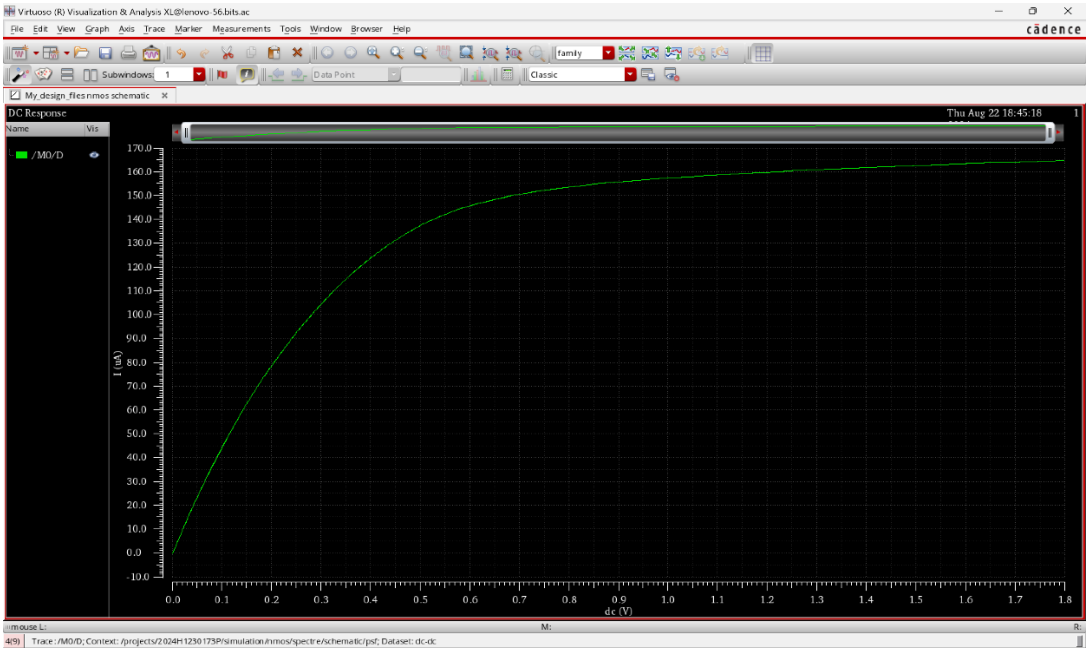
Below is a plot of I_d vs V_{gs} at various V_{ds} values from 0 to 1.8V at steps of 0.3V.



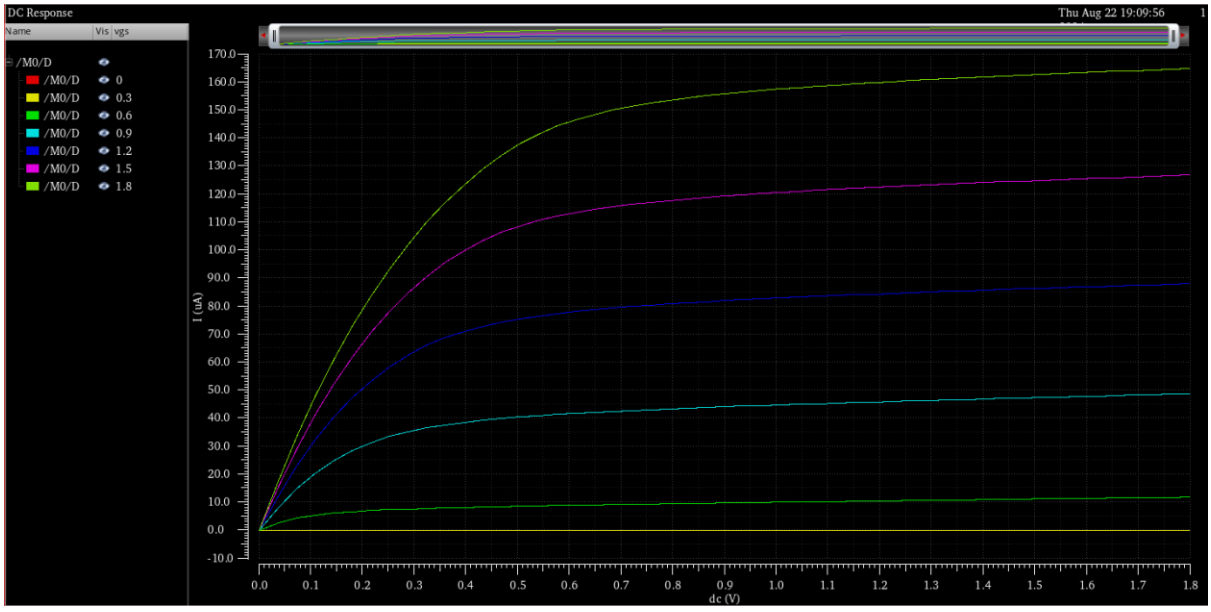
V_{ds} step (V)	V_{th} (mV)
0.3	450
0.6	440
0.9	430
1.2	420
1.5	420
1.8	410

Output characteristics:

A plot of I_d vs V_{ds} at V_{ds} = 1.8V and V_{gs} = 1.8V is shown below.



Below is a plot of I_d vs V_{ds} at various V_{gs} values from 0 to 1.8 V at steps of 0.3V.

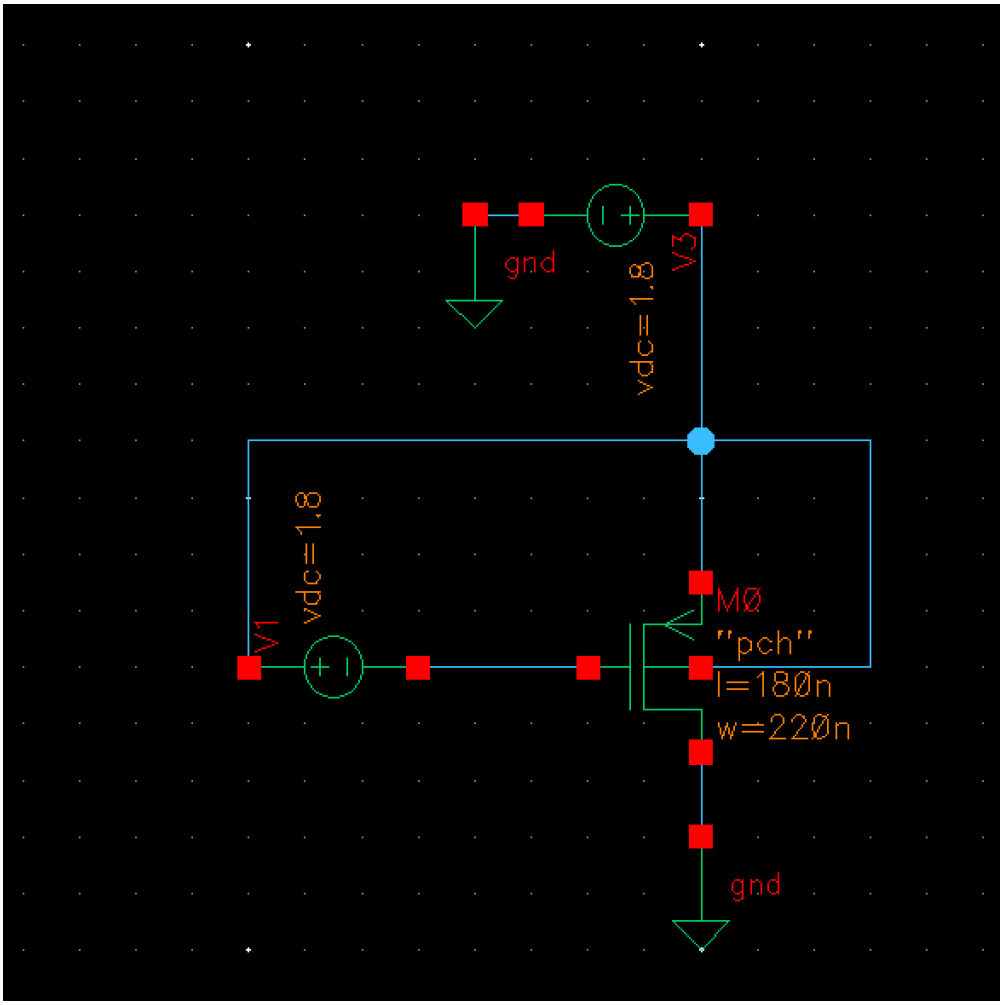


2. P-MOSFET

Model name: pch

Width of PMOS: 220nm

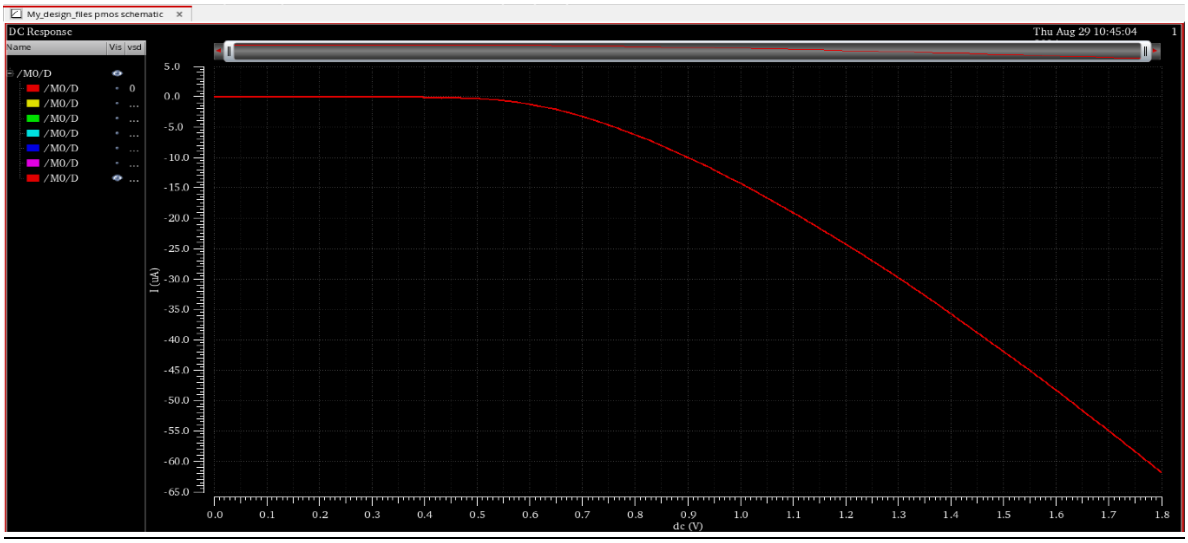
Length of PMOS: 180 nm



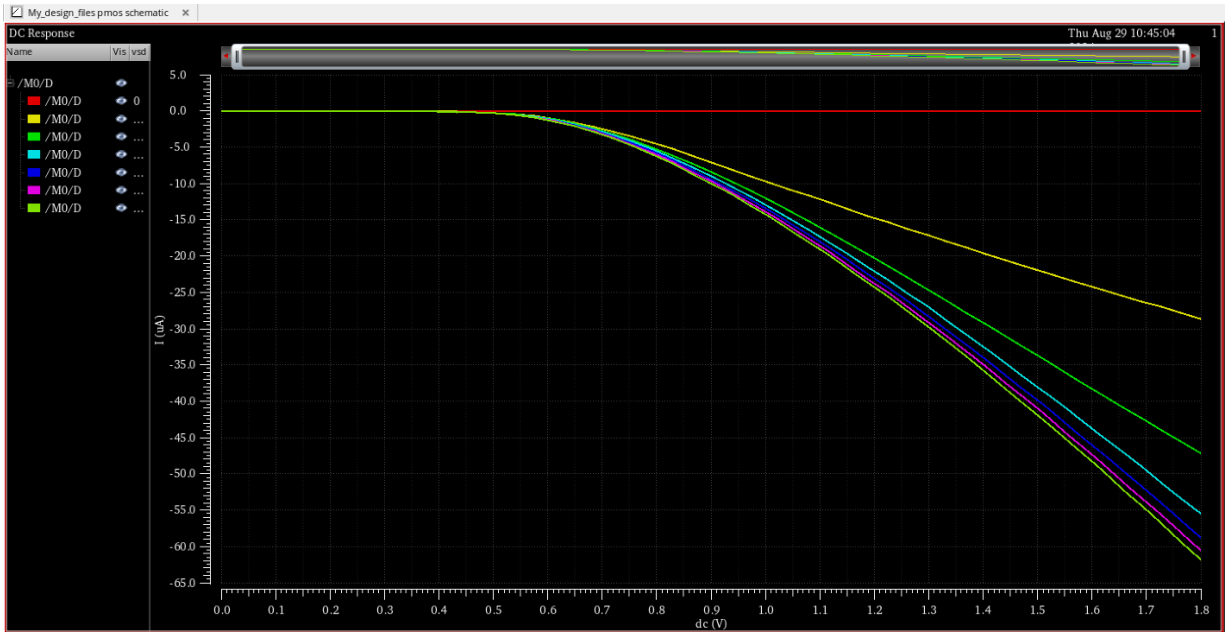
Schematic of PMOS

Input characteristics:

Plot of drain current I_d vs V_{sg} taking V_{sd} = 1.8V and sweeping V_{sg} from 0 to 1.8V.



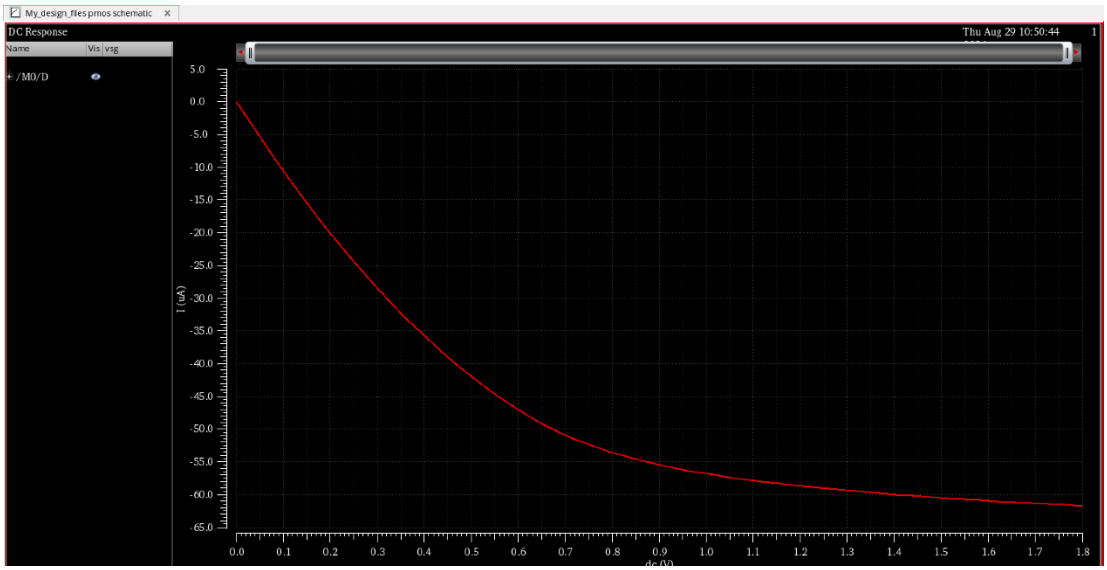
Below is a plot of I_d vs V_{sg} at various V_{sd} values from 0 to 1.8V at steps of 0.3V.



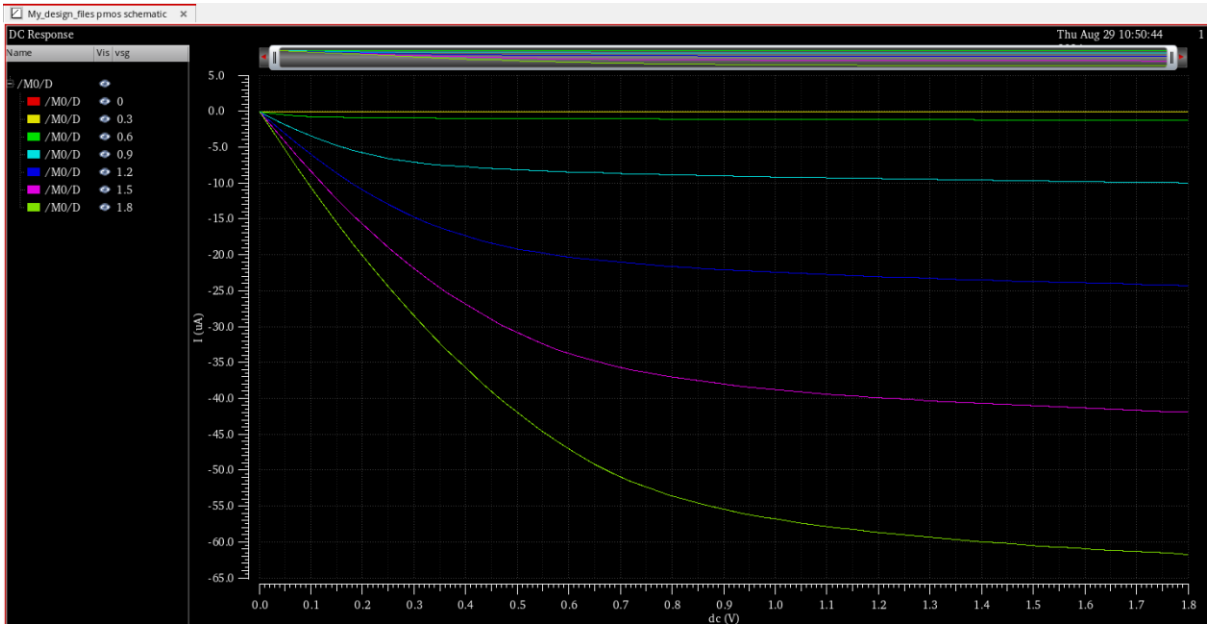
V_{sd} step (V)	V_{th} (mV)
0.3	-648
0.6	-612
0.9	-612
1.2	-612
1.5	-612
1.8	-612

Output characteristics:

A plot of I_d vs V_{sd} at V_{sg} = 1.8V and sweeping V_{sg} from 0 to 1.8V is shown below.



Below is a plot of I_d vs V_{ds} at various V_{gs} values from 0 to 1.8 V at steps of 0.3V.



Inference:

We have successfully plotted and observed NMOS and PMOS input and output characteristics.