BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI

I SEMESTER 2024-25, MEL G621 – VLSI DESIGN

LAB ASSIGNMENT – 7

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AIM: 1. To implement the function Y = ((A'+B').(C'+D'+E')+F').G' using CMOS logic and size the design as that of the inverter with $(W/L)_n = 2$ and $(W/L)_p = 6$. Find the delays for the worst case and best-case scenarios.

2. To implement above function Y using pseudo NMOS logic and find the delays for the worst and best-case scenarios.

3. To implement XNOR gate using dual and non-dual implementation and compare their best and worst-case delays.

Tools used: Cadence Virtuoso

1. Static CMOS function implementation

A static CMOS circuit gives the complemented version of the function implemented. To get desired function, we first write the complemented form of Y so that CMOS implementation yields output Y.

$$Y = ((A.B + C.D.E).F + G)'$$

The sizing must be done so that equivalent widths of pull-up and pull-down networks match given reference inverter with $(W/L)_n = 2$ and $(W/L)_p = 6$. The circuit with sized transistors is shown in Fig.1. The 7 inputs were given pins from A to G and output is taken from pin Y.

The intermediate node capacitance was taken as 100fF and output load capacitance was taken as 200fF. The base width according to which the transistors were sized was taken as 220nm. Transistor channel length is 180nm. The circuit schematics of the pull-up and pull-down networks are shown in Fig.2 and Fig.3.

Input square wave has a time period of 50ns. To make the input square wave as close to ideal step as possible, input rise and fall times are set to 1 attosecond (10^{-18} s).

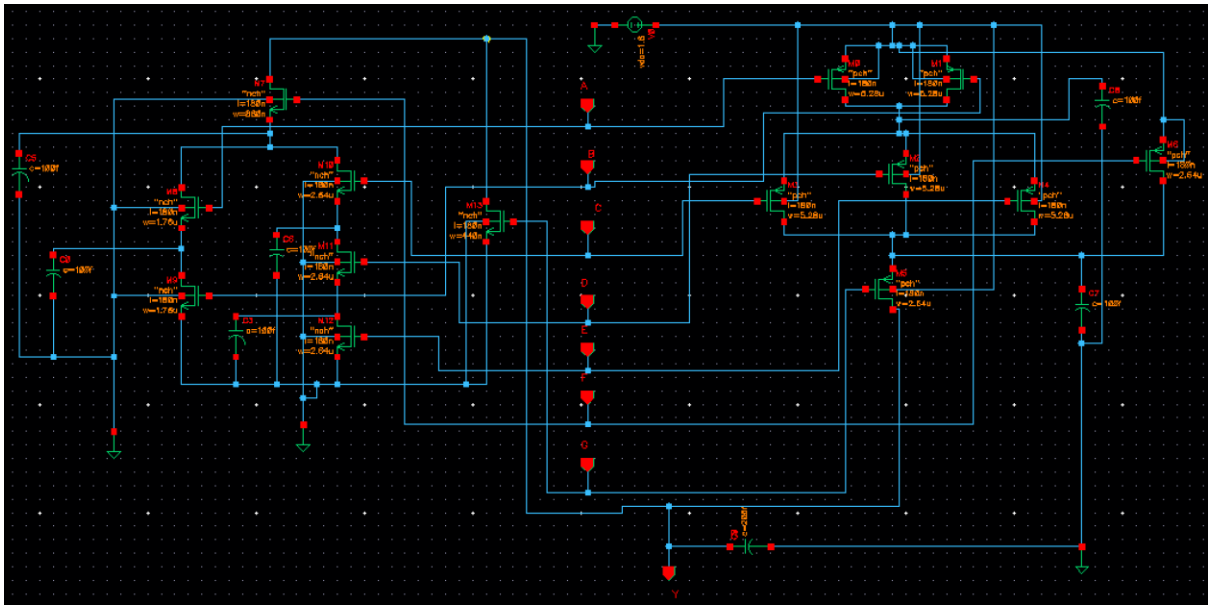


Fig1. Static CMOS implementation

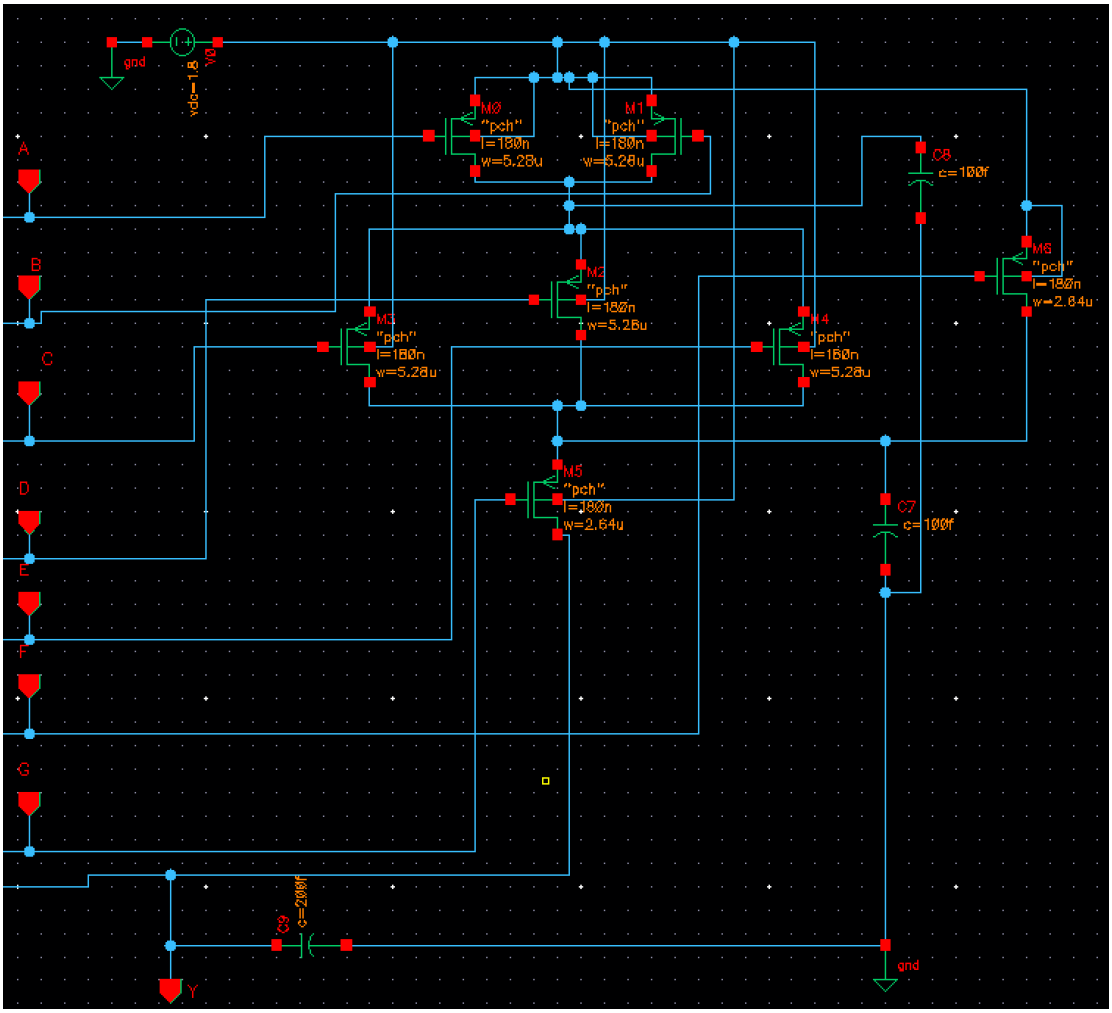


Fig2. Pull-up network

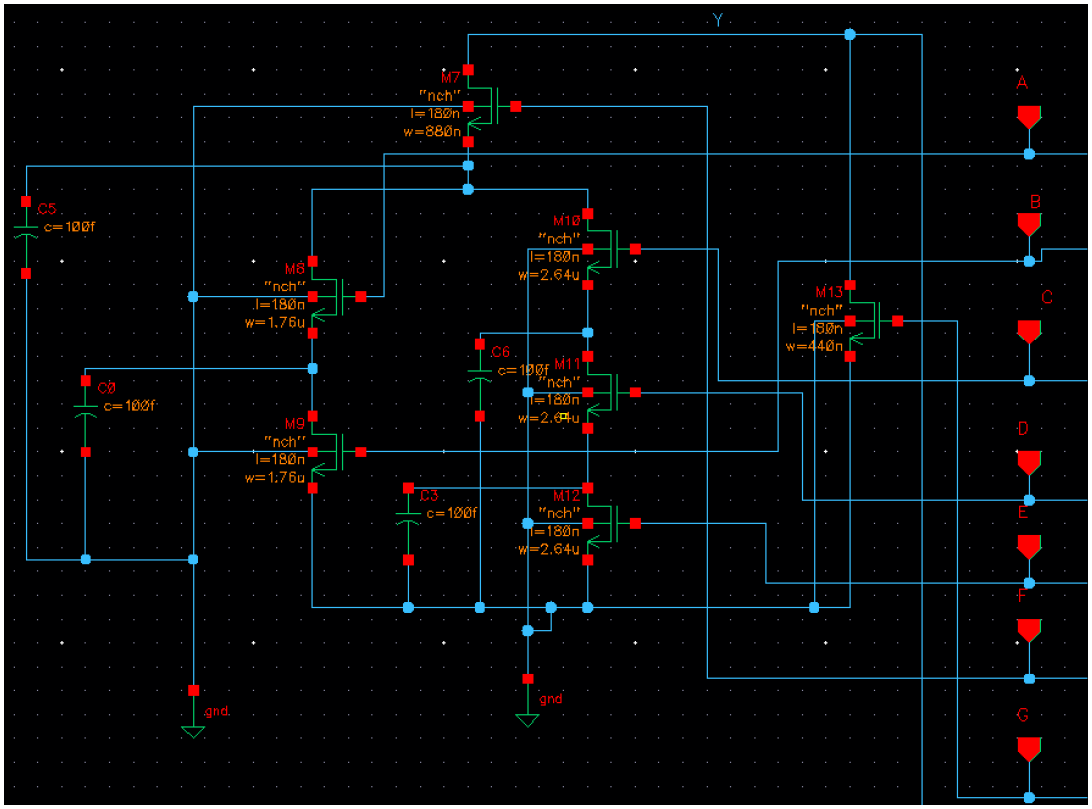
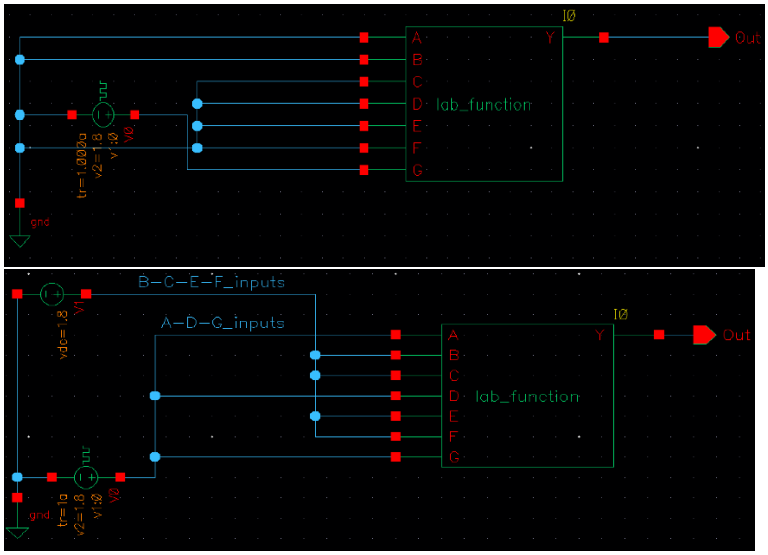


Fig3. Pull-down network

The worst-case propagation delay is seen when the maximum number of transistors in a single path are ON from a power supply (V_{DD} or GND) to the output. The best-case propagation delay is seen when the minimum number of transistors are in a single path are ON from a power supply (V_{DD} or GND) to the output. The high to low delays are caused when pull-down network transistors are ON (rising inputs) and low to high delays are caused when pull-up network transistors are ON (falling inputs).



Test schematic with circuit symbol for worst and best-case propagation delay(rise and fall time) calculation.

This gives us 4 cases, whose propagation delays are tabulated below.

Pull-down Network	Worst case	F-C-D-E on	t_{pHL}= **0.7515ns**
	Best case	All NMOS on	t_{pHL}= **0.2531ns**
Pull-up Network	Worst case	A-D-G on	t_{pLH}= **0.9344ns**
	Best case	All PMOS on	t_{pLH}= **0.3675ns**

Figures 4-7 show the waveforms for the 4 cases.

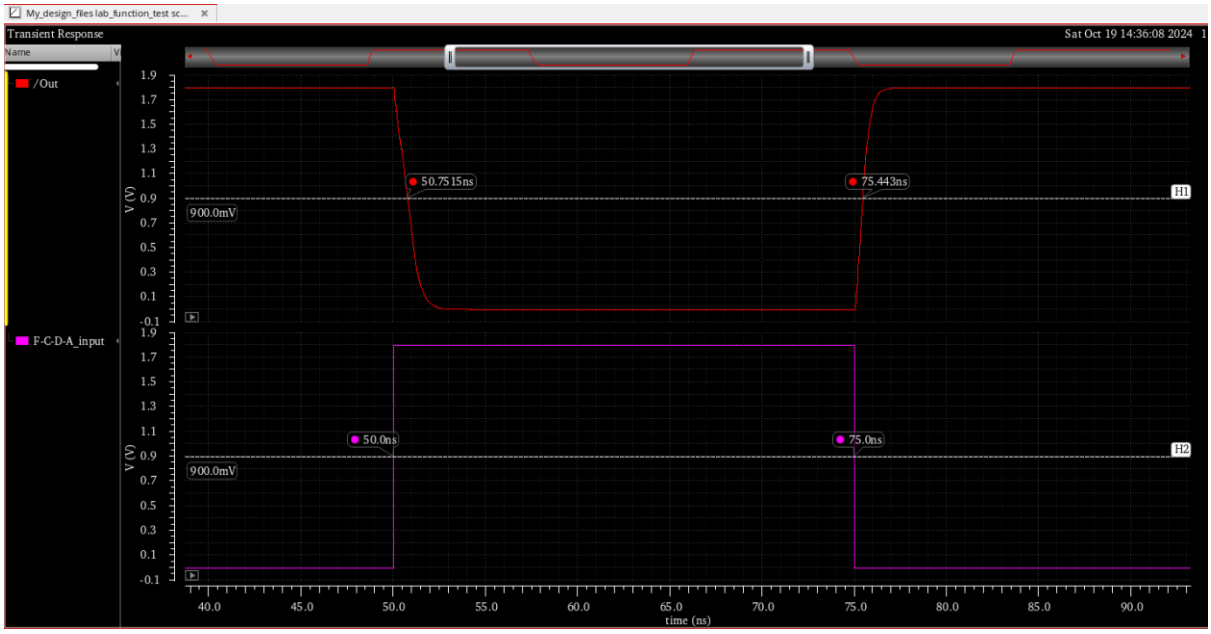


Fig4. Worst case t_{pHL} for rising input at F,C,D & A pins

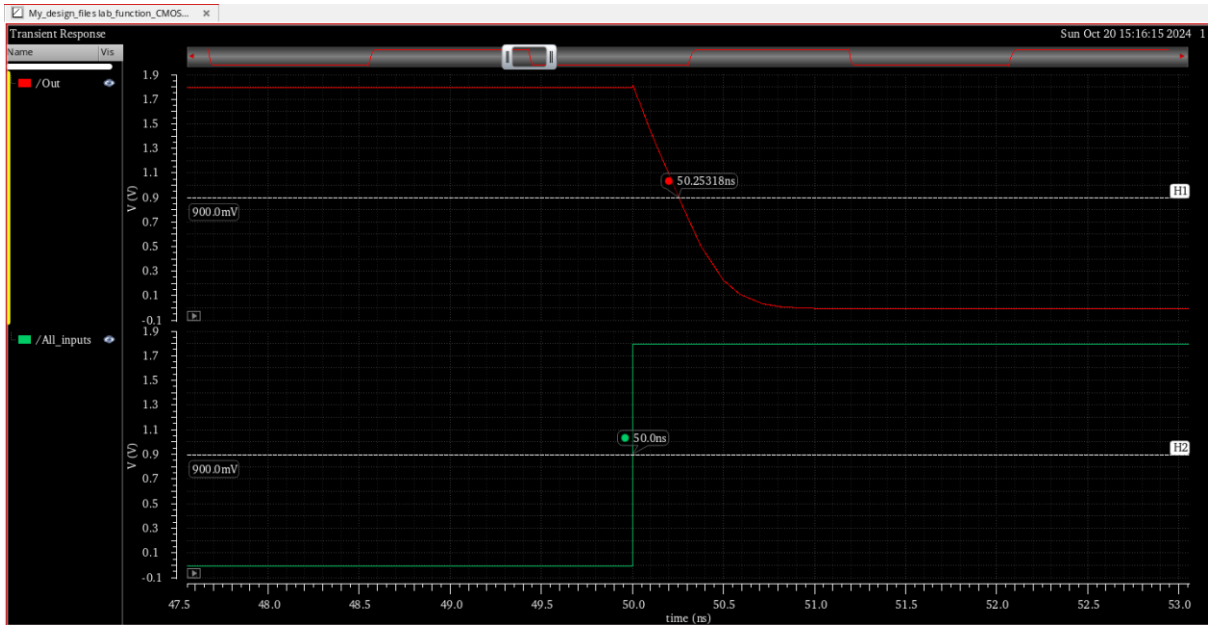


Fig5. Best case t_{pHL} for rising input at each pin

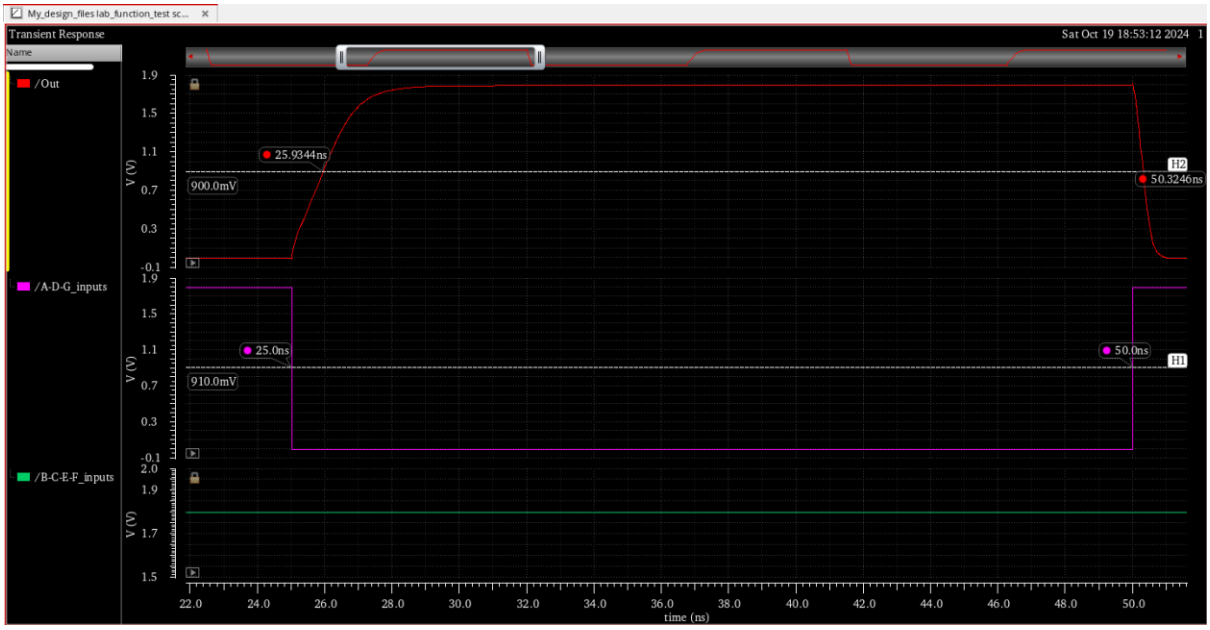


Fig6. Worst case $\mathbf{t_{pLH}}$ for falling input at A, D & G pins

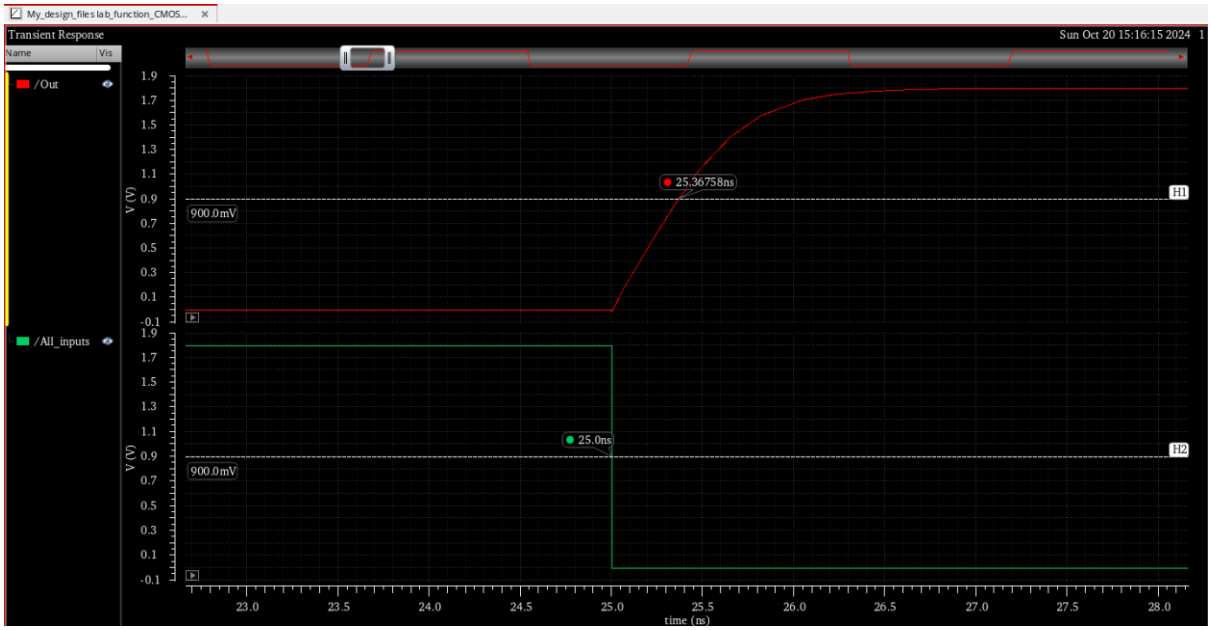


Fig7. Best case $\mathbf{t_{pLH}}$ for falling input at each pin

2. Pseudo NMOS function implementation

In a pseudo NMOS logic circuit, the entire pull-up network is replaced by a single PMOS transistor that is always in ON state while the pull-down network remains the same. Thus, instead of 2N transistors in a CMOS circuit, a pseudo NMOS circuit for the same function requires N+1 transistors. The circuit schematic is shown in Figure 8.

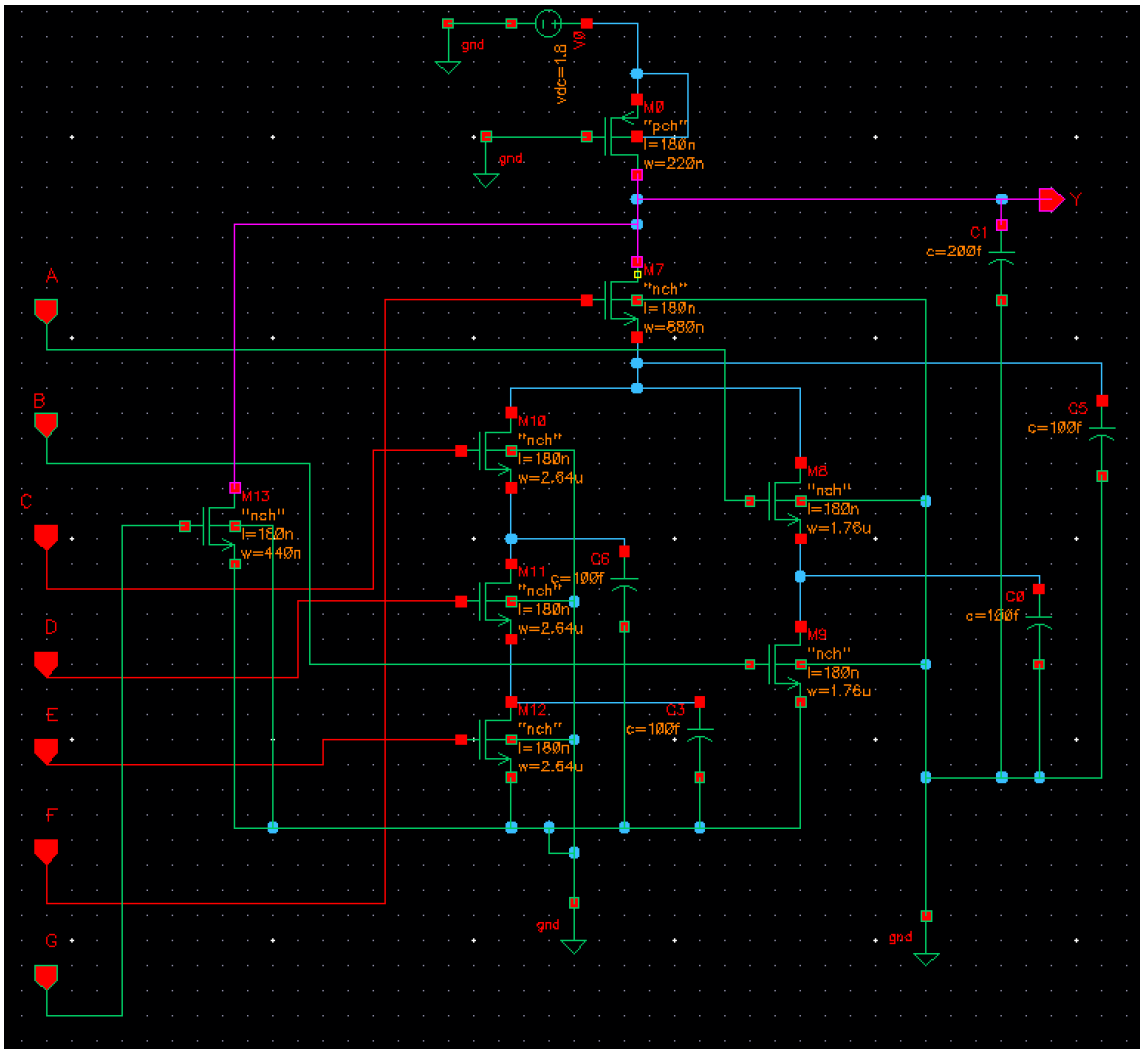


Fig8. Pseudo NMOS implementation

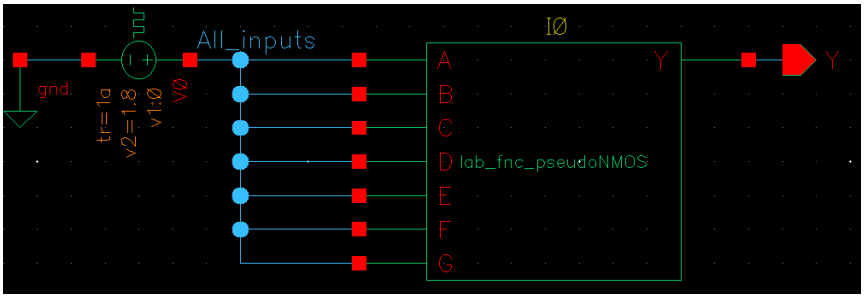


Fig9. Pseudo NMOS circuit test schematic with symbol

The delays for pseudo NMOS circuit are tabulated below.

Pull-down Network	Worst case	F-C-D-E on	t_{pHL}= **0.4848ns**
	Best case	All NMOS on	t_{pHL}= **0.2528ns**
Pull-up Network	Worst case	PMOS on	t_{pLH}= **3.0621ns**
	Best case	PMOS on	t_{pLH}= **3.0621ns**

The waveforms are for pseudo NMOS are shown in Figures 10 to 12.

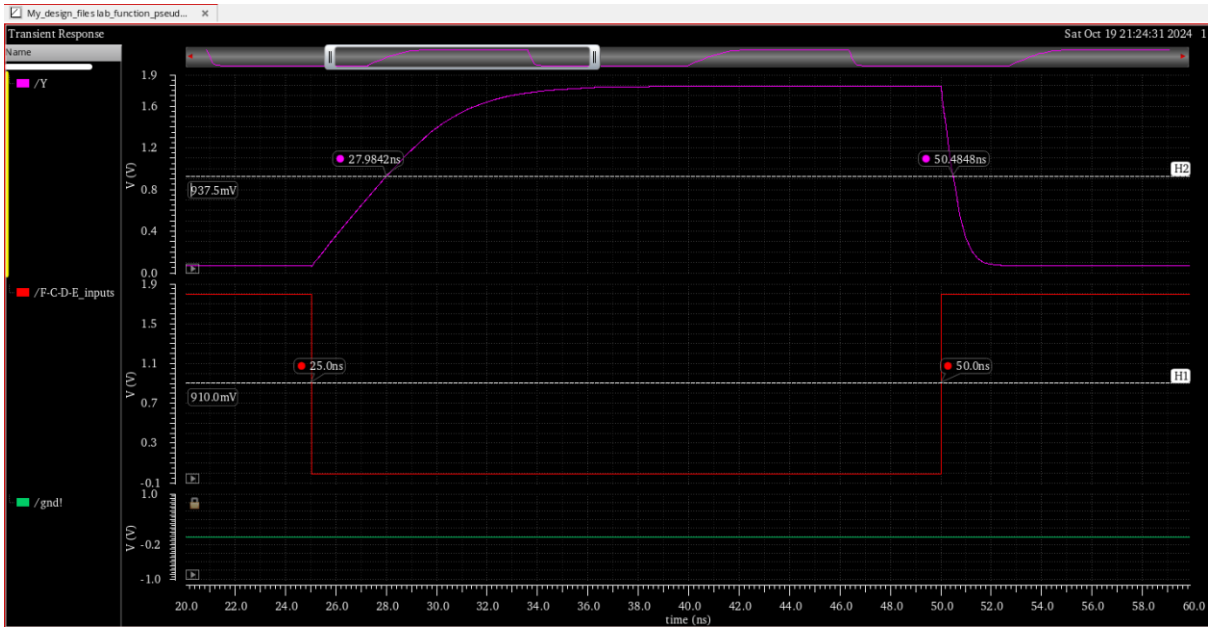


Fig10. Worst case t_{pHL} for rising input at F,C,D & E pins

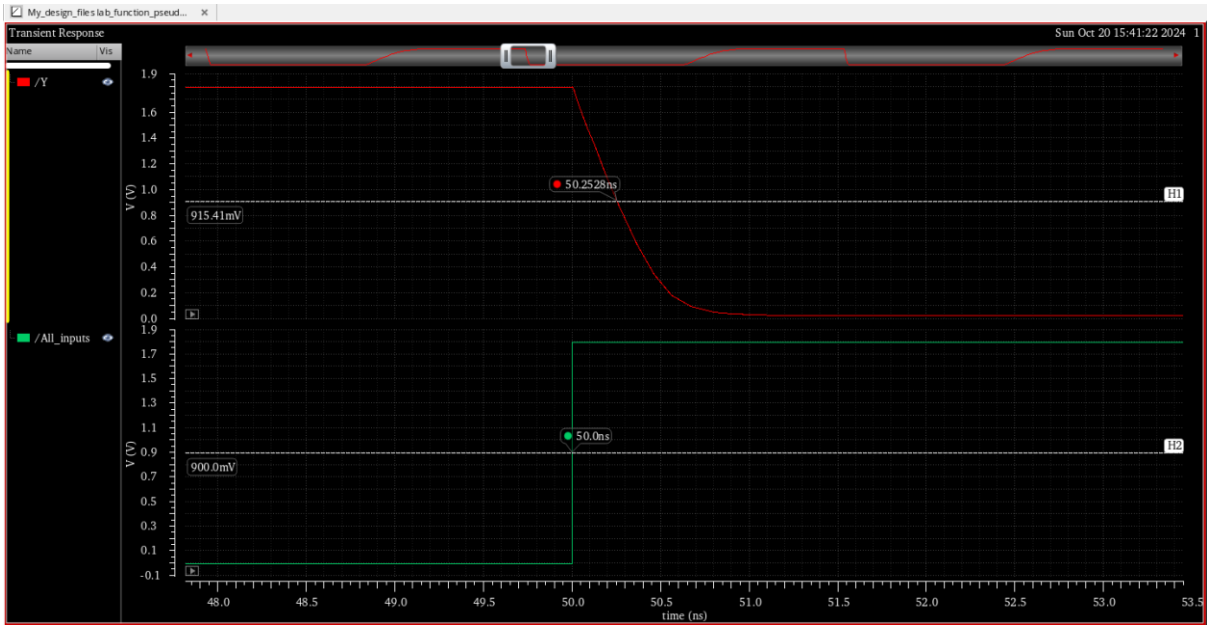


Fig11. Best case t_{pHL} for rising input at all pins

Since the PMOS transistor is always ON and independent of inputs, its resultant worst and best-case t_{pLH} will be equal.

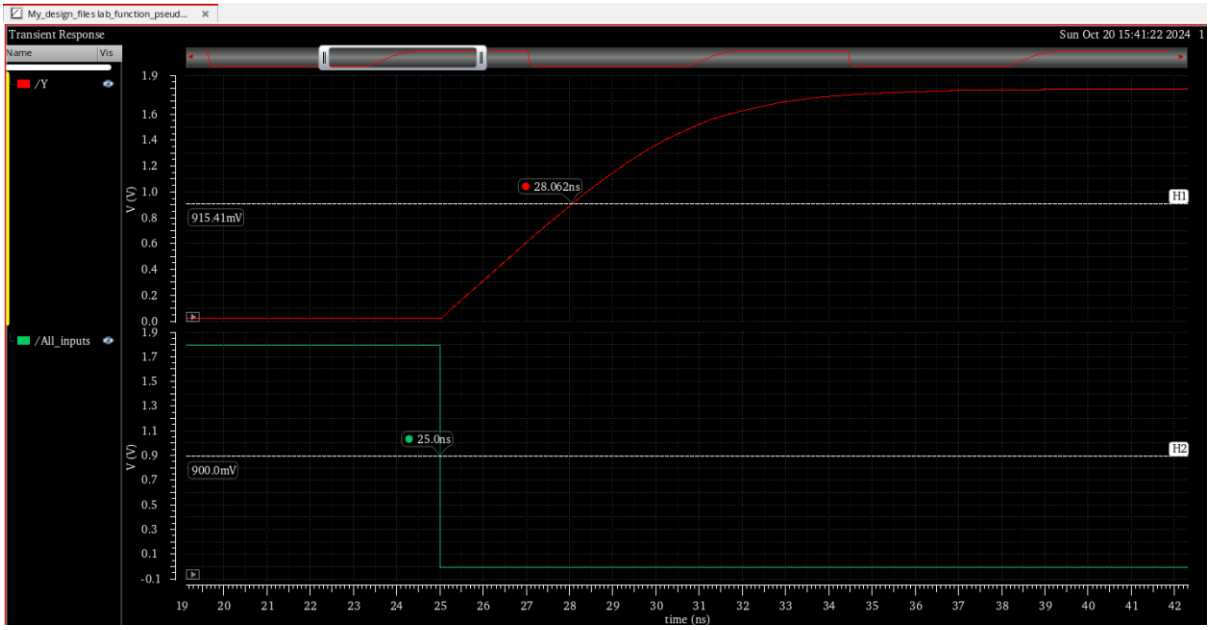


Fig12. Best case delay = worst case $\mathbf{t_{pLH}}$ for falling inputs (NMOS network turns off)

3. Dual and Non-dual XNOR gate implementation

The Dual and CMOS implementations are shown in Figures 13 &14.

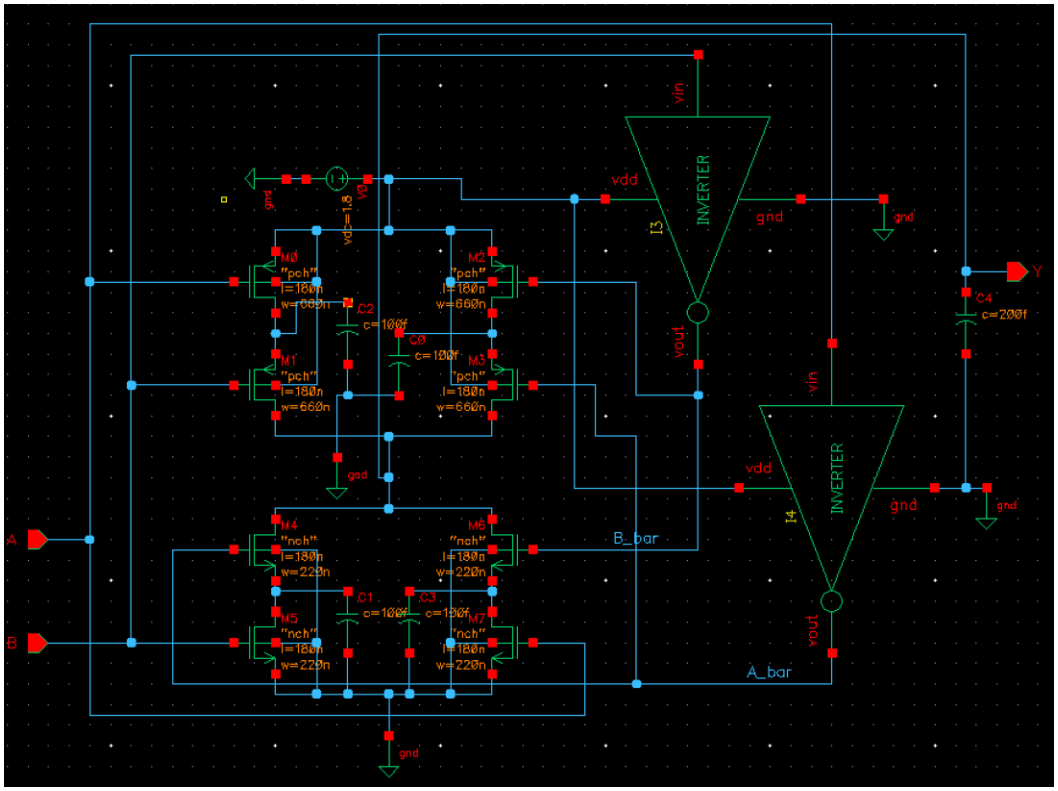


Fig13. Dual implementation of XNOR circuit

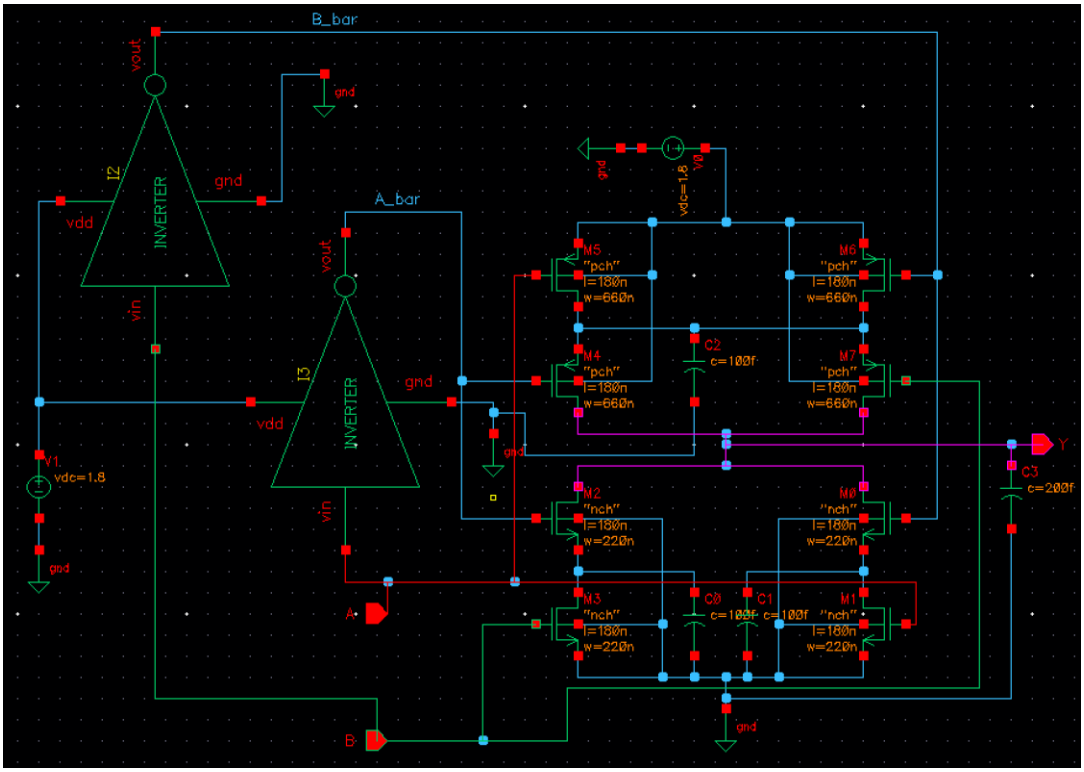


Fig14. CMOS implementation of XNOR circuit

The sizing of the circuits have been done to get equivalent width same as an inverter with $(W/L)_n = 2$ and $(W/L)_p = 6$. Symbols were made for the Dual and CMOS circuits and their test schematics are shown in Fig 15.

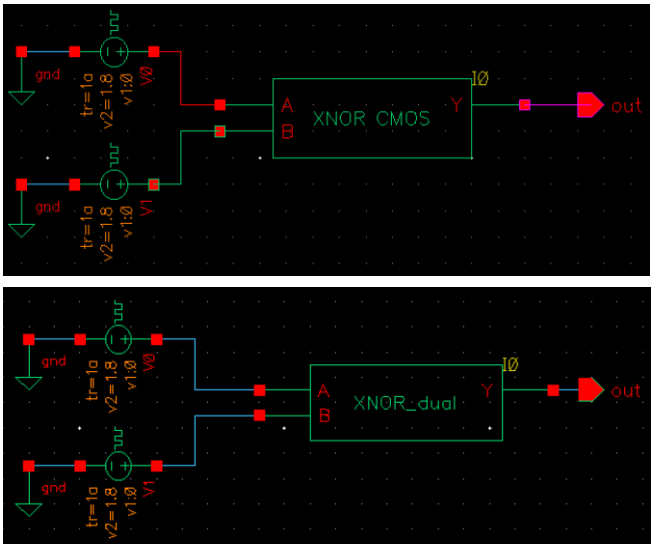


Fig15. Test schematic with circuit symbol for CMOS and Dual XNOR implementations.

The propagation delays waveforms (Fig. 16 and 17) are shown and they are tabulated below. For a given set of input combinations, only TWO transistors can be ON in both the pull-up and pull-down networks of both implementations. The worst case delays are observed when the **inputs of Body Effect transistors** are transitioning.

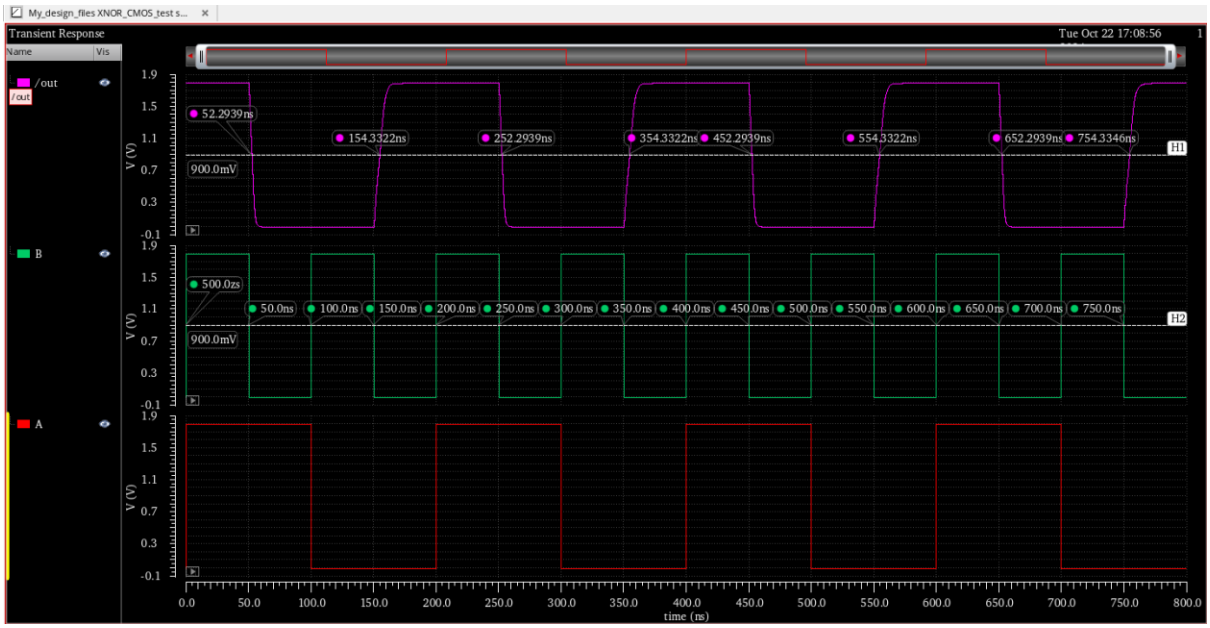


Fig16. CMOS XNOR waveforms

The propagation delays of CMOS implementation are given below.

Pull-down Network	Worst case	A=1, B=1 to 0	t_{pHL}= **2.2939ns**
	Best case	A=1 to 0, B=1	t_{pHL}= **1.6164ns**
Pull-up Network	Worst case	A=1 to 0, B=0	t_{pLH}= **5.1287ns**
	Best case	A=0, B=1 to 0	t_{pLH}= **4.3322ns**

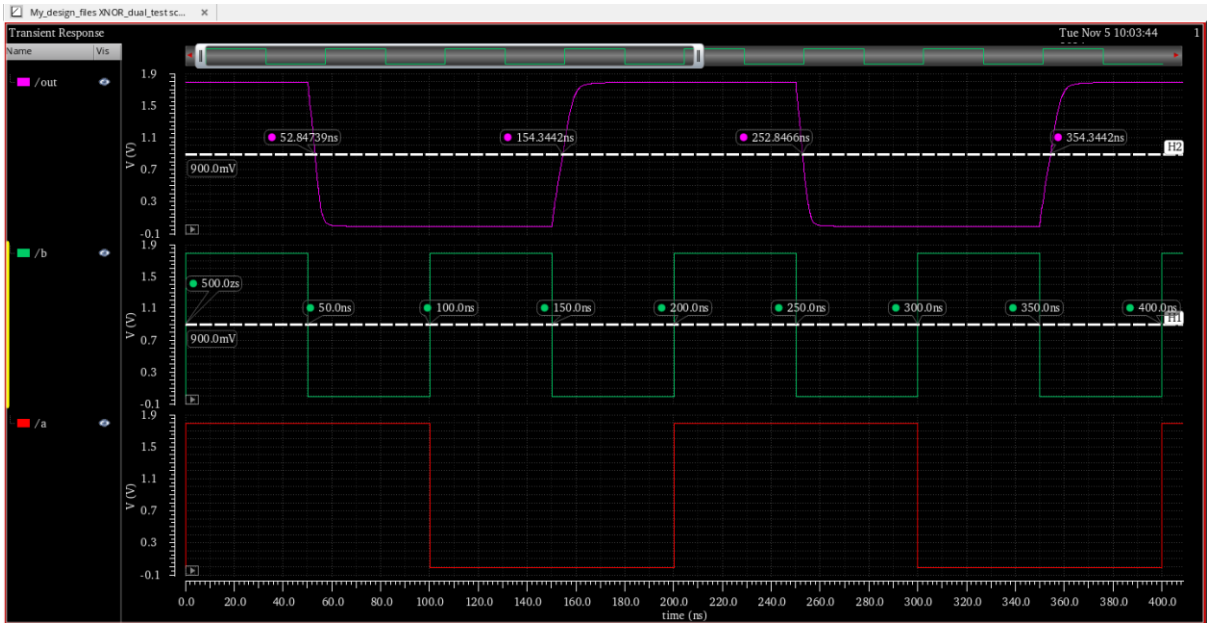


Fig17. Dual XNOR waveforms

The propagation delays of dual implementation are given below.

Pull-down Network	Worst case	A=1, B=1 to 0	t_{pHL}= **2.8473ns**
	Best case	A=1 to 0, B=1	t_{pHL}= **1.6166ns**
Pull-up Network	Worst case	A=1 to 0, B=0	t_{pLH}= **5.1001ns**
	Best case	A=0, B=1 to 0	t_{pLH}= **4.3442ns**

We see that both implementations have nearly identical propagation delays. Through RC delay model analysis, we see that the dual implementation should have better performance.