BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI

I SEMESTER 2024-25, MEL G621 – VLSI DESIGN

LAB ASSIGNMENT – 6

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AIM: To construct the schematics of 2x1 multiplexer using Pass Transistor Logic and Transmission gates and calculate the propagation delays t_{pHL}, t_{pLH} and t_p for various input combinations.

Tools used: Cadence Virtuoso

nMOS parameters

Model name – nch

Length of transistor = 180nm

Width of transistor = 220nm

pMOS parameters

Model name - pch

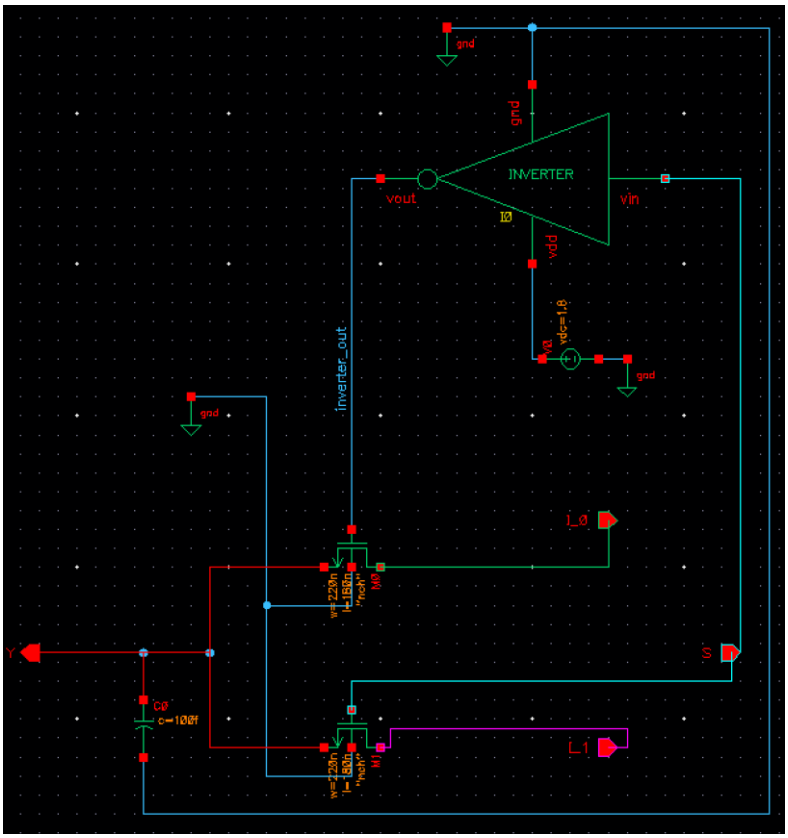
Length of transistor = 180nm

Width of transistor = 220nm

1. Multiplexer using Pass Transistor Logic

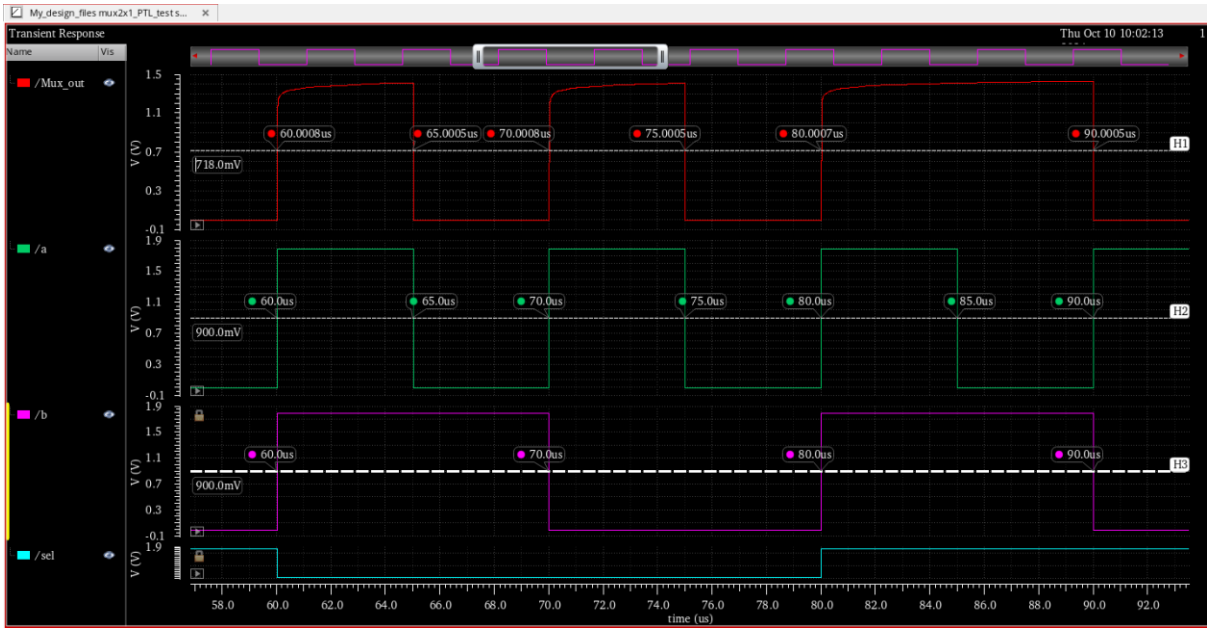
The 2x1 multiplexer is implemented using two nMOS transistors connected in as shown below. An output load capacitance of 100 fF is placed.

Circuit Schematic:



Square waves of different frequencies are fed to the input pins A, B and Sel to get outputs for the various combinations: 20ns, 40ns and 80ns respectively.

Simulation waveforms:

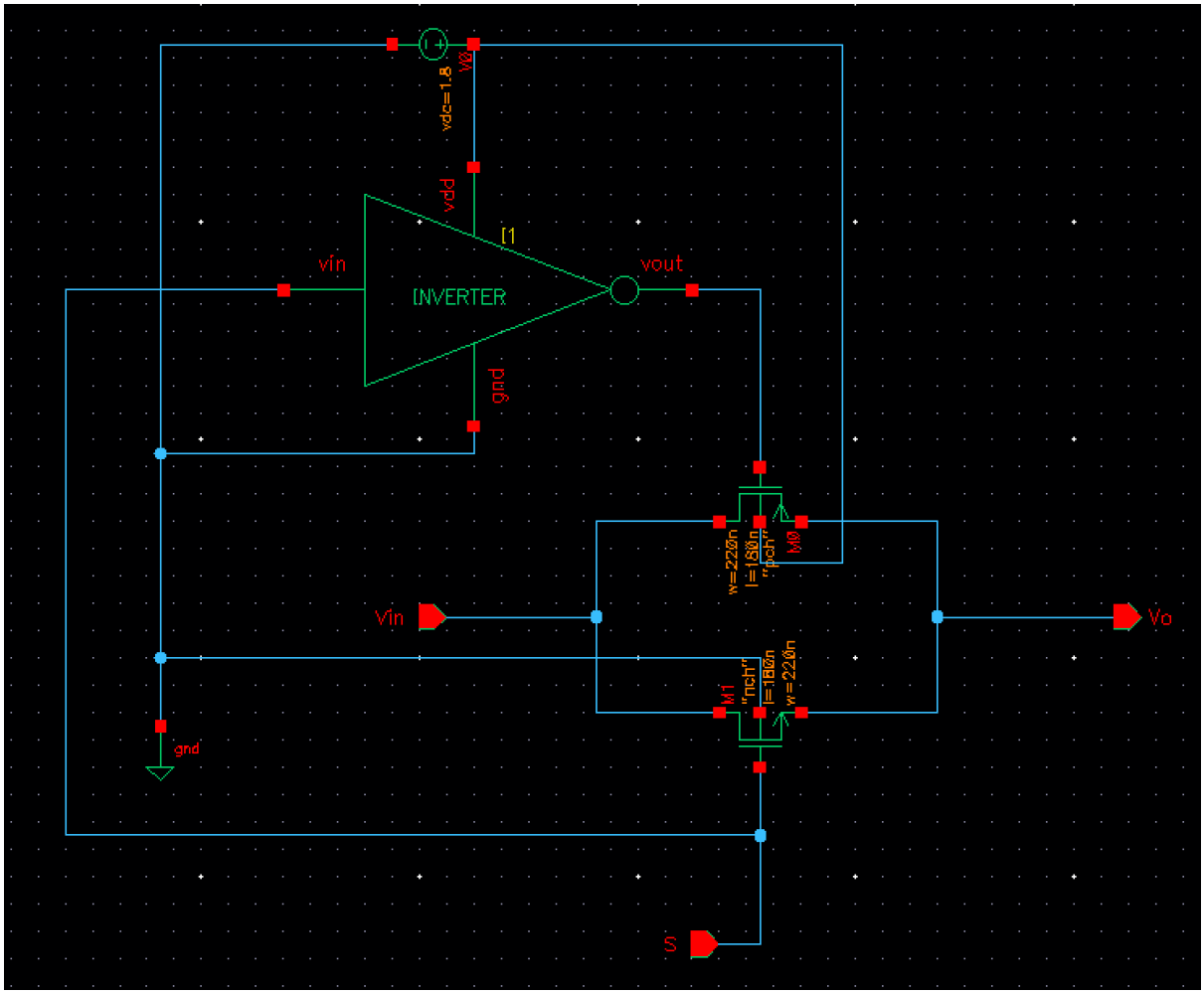


The propagation delays for the input signals A and B with constant select input are tabulated below.

Inputs	t_{pLH}	t_{pHL}	t_p
A	0.7ns	0.5ns	0.6ns
B	0.8ns	0.5ns	0.65ns

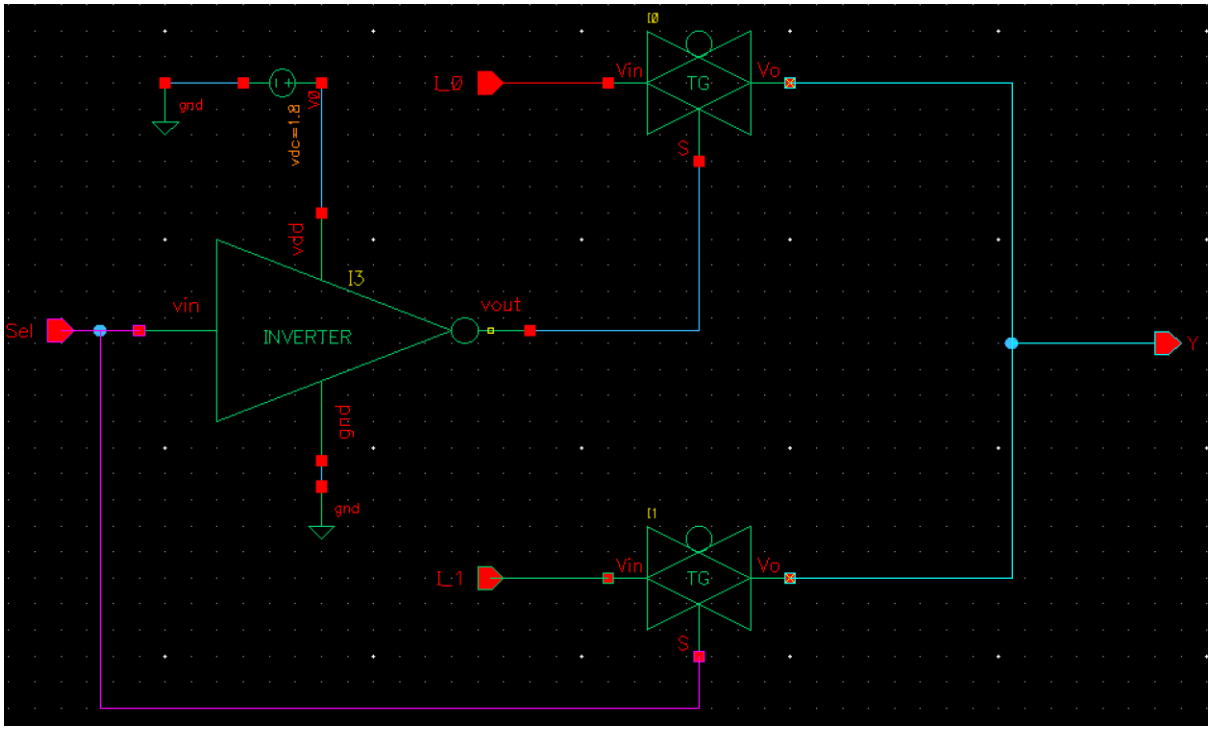
2. Multiplexer using Transmission Gates

The schematic of the transmission gate constructed is shown below, with control signal pin 'S' and internally generated complement S`. Two such transmission gates are used to design a 2x1 multiplexer.

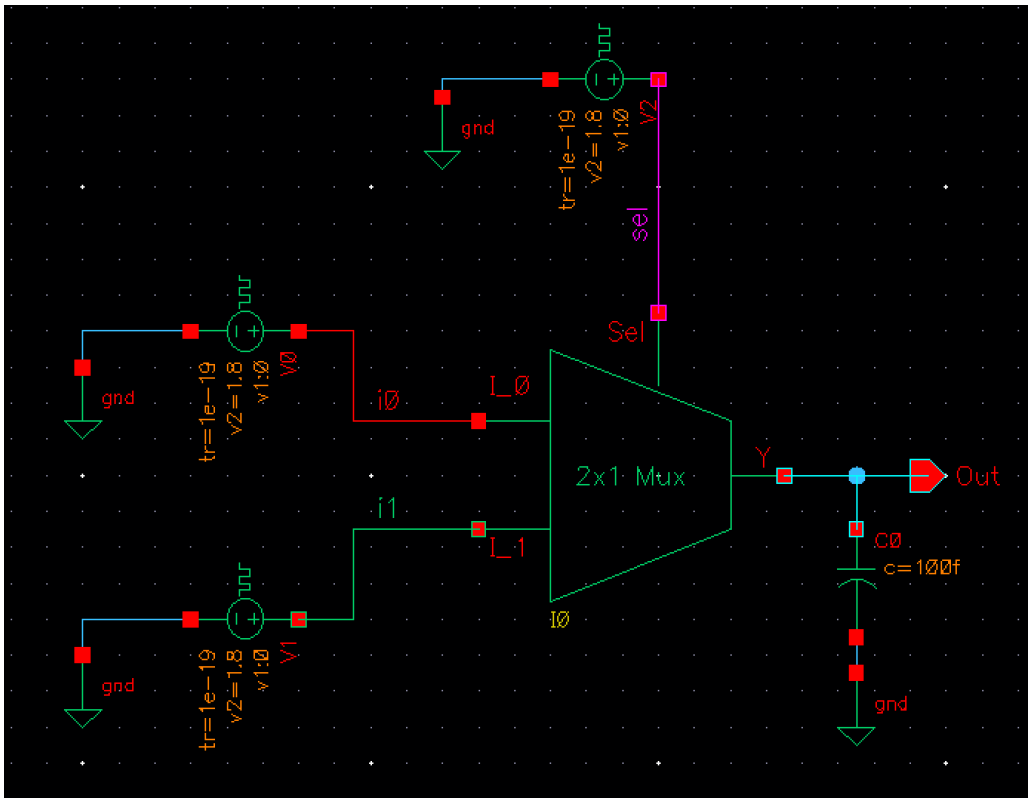


Circuit Schematic:

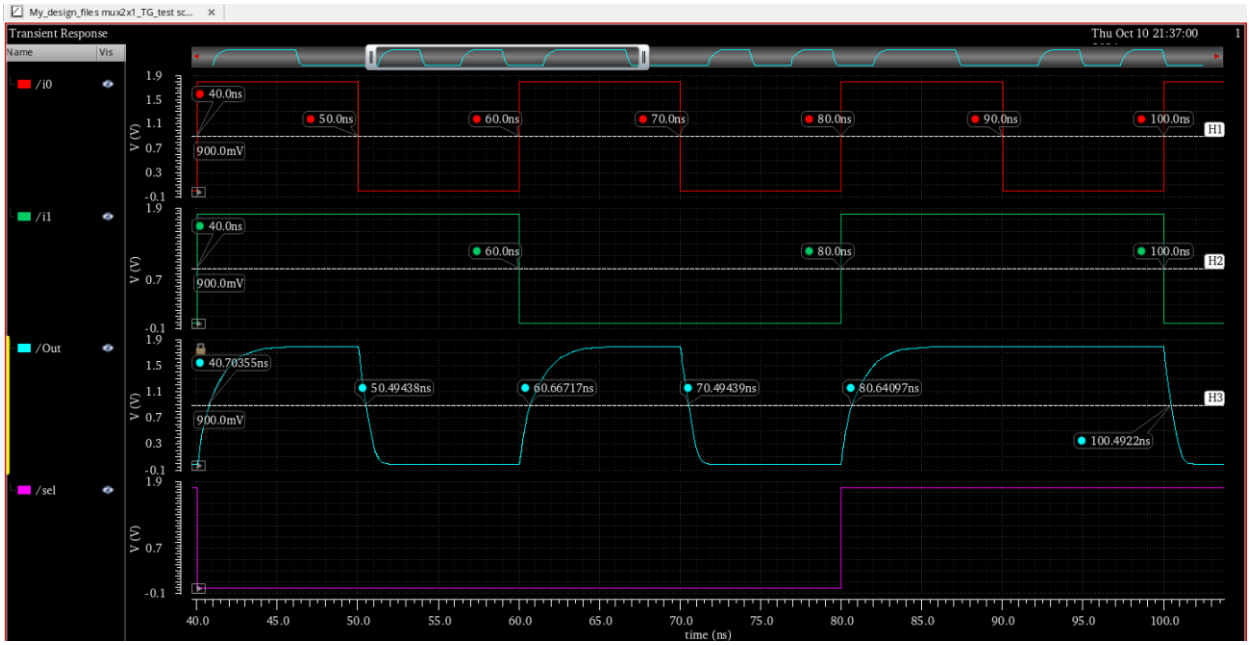
The pin diagram of the 2x1 multiplexer using TGs is shown below.



Square waves of different frequencies are fed to the input pins I0, I1 and Sel to get outputs for the various combinations: 20ns, 40ns and 80ns respectively. A load capacitance of 100fF is placed at the output.



Simulation waveforms:



The propagation delays for the input signals A and B with constant select input are tabulated below.

Inputs	t_{pLH}	t_{pHL}	t_p
I0	0.7ns	0.49ns	0.6ns
I1	0.64ns	0.49ns	0.65ns