**BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI**

**I SEMESTER 2024-25, MEL G621 – VLSI DESIGN**

**LAB ASSIGNMENT – 4**

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**AIM:** To perform transient analysis of Resistive and CMOS inverters and find $t_{pHL}$, $t_{pLH}$ and $t_p$:

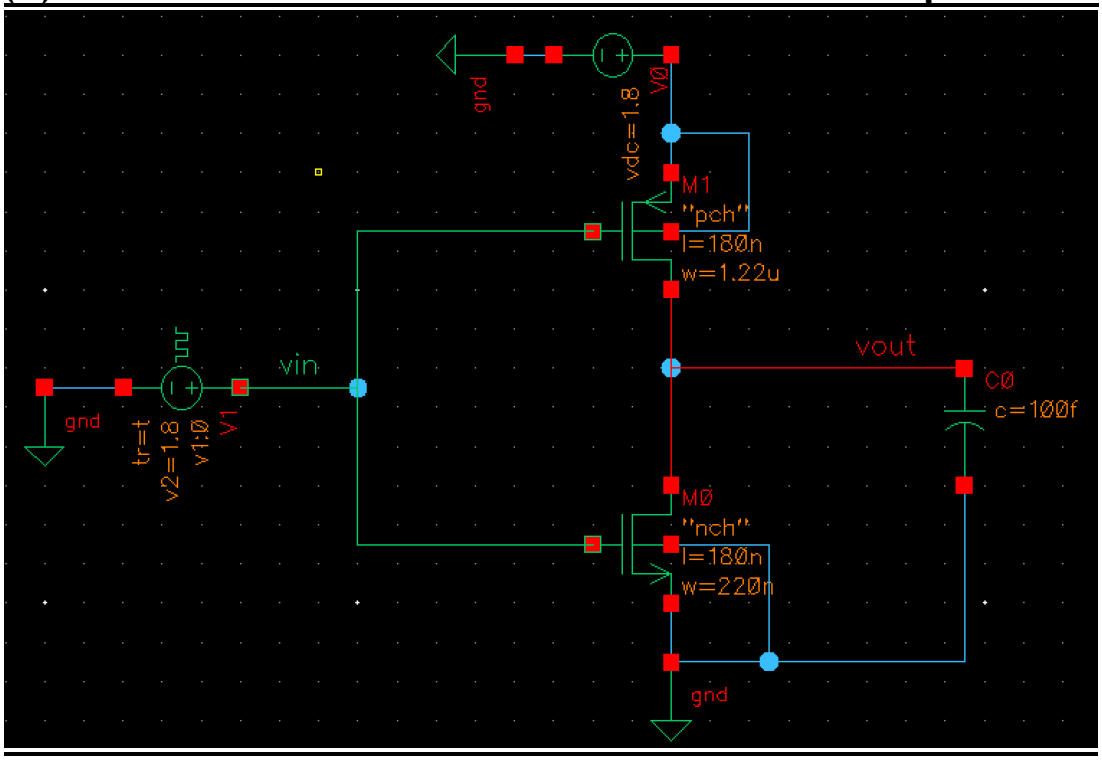
i. While varying rise and fall time of the input square wave from 0ns to 200 ns at steps of 50 ns.
ii. Verify using the average current method.
iii. And design a 5-stage ring oscillator using the designed CMOS inverter and calculate its oscillating frequency.

**Tools used:** Cadence Virtuoso

## Propagation delay:

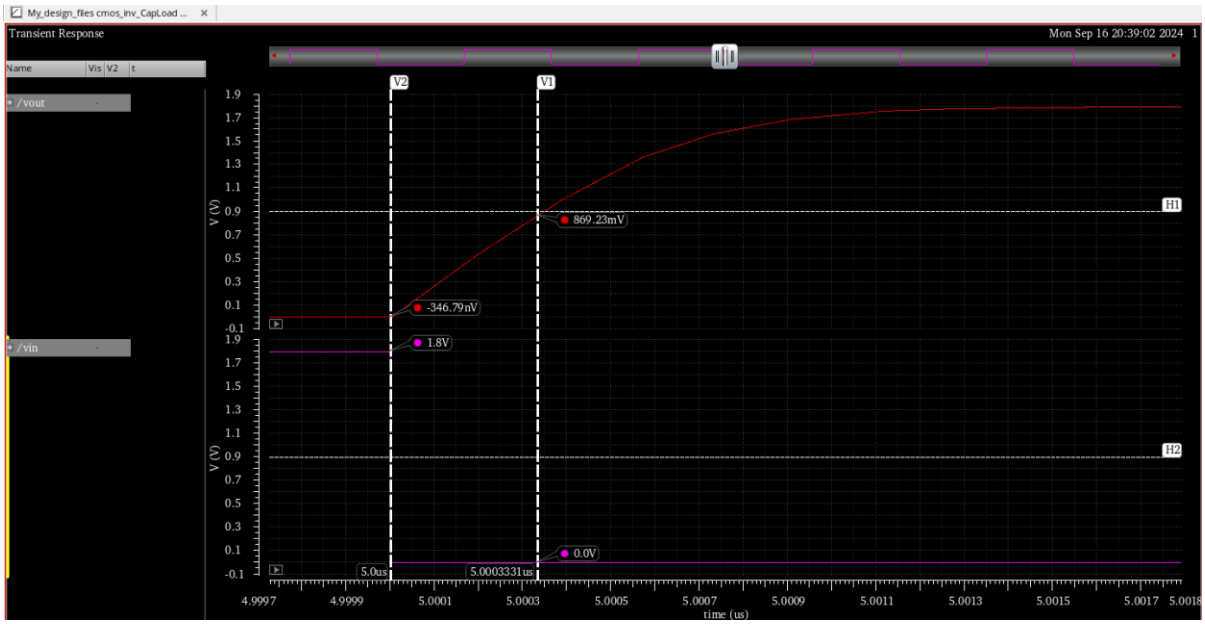
Propagation delay is calculated as the time passed between the input falling/rising to 50% of its final value and the output to rise/fall to 50% of its final value.

## (i.) Circuit Schematic for CMOS inverter with load capacitance:

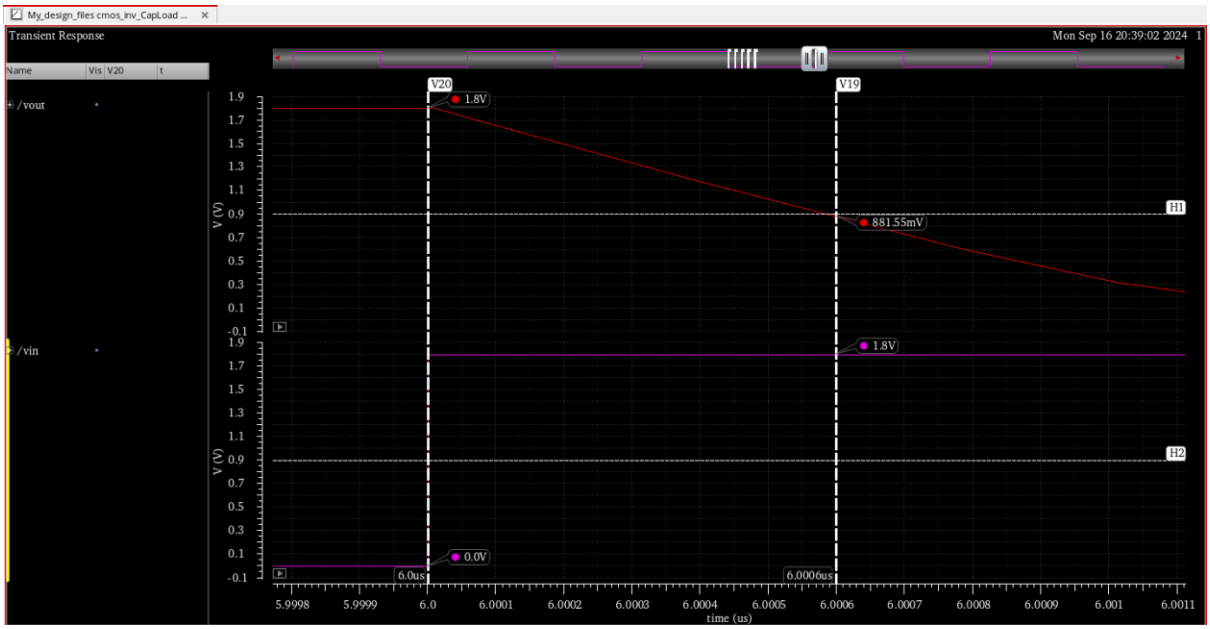


## Transient analysis:

Transient analysis was performed with input waveform of period 2µs and pulse width 1µs. The below graph shows how $t_{pLH}$ was calculated for a 0 ns fall time input.



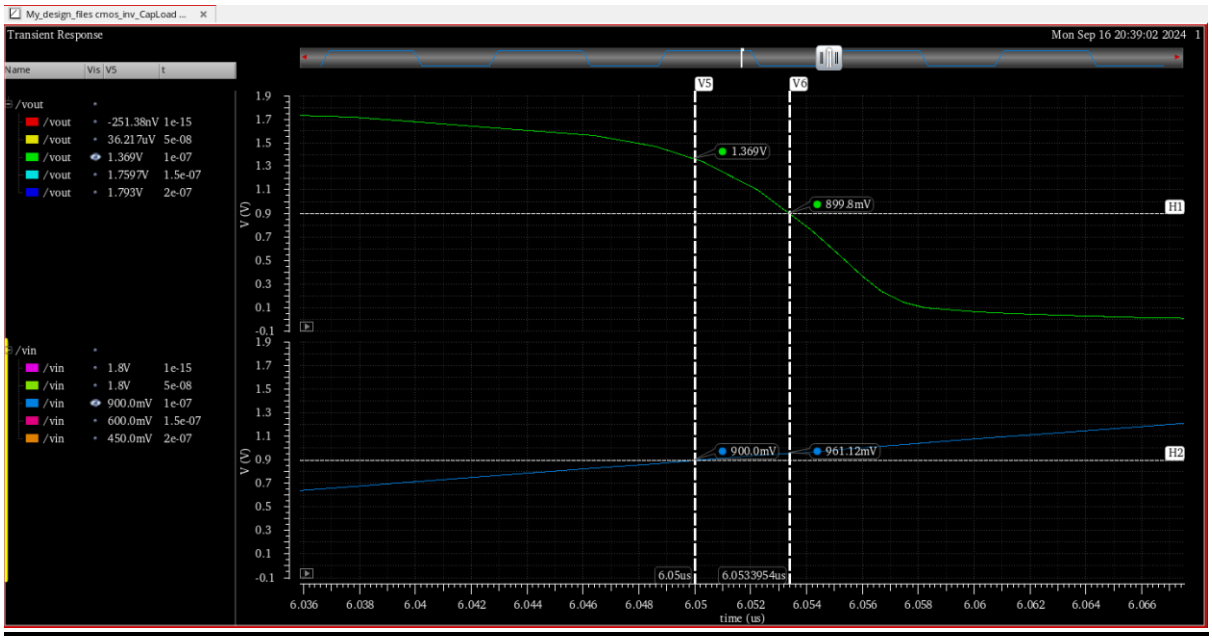

The graph below shows how $t_{pHL}$ was calculated for a 0 ns rise time input.



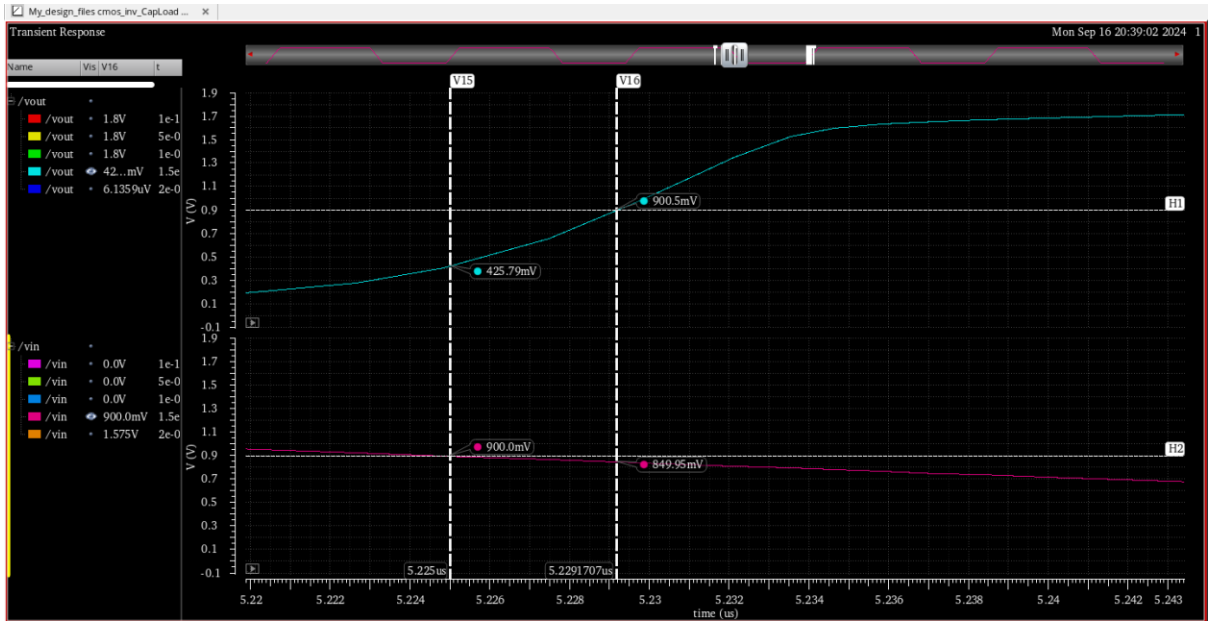
## Parametric analysis with varying $t_r$ and $t_f$

Parametric analysis was performed by varying both rise and fall times from 0 ns to 200 ns at steps of 50 ns. For the CMOS inverter, $V_{out\ 50\%} = 0.9V$.

The below graph shows $t_{pHL}$ for t=100 ns.



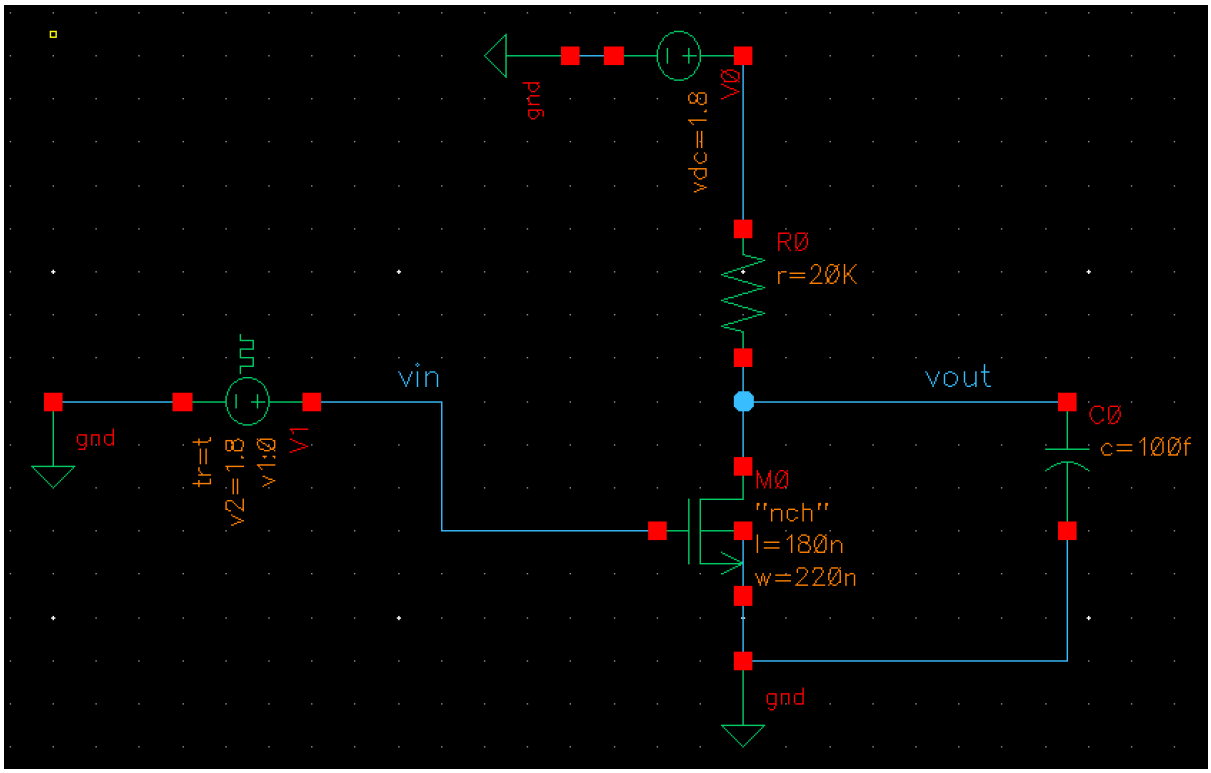

The below graph shows $t_{pLH}$ for t=150 ns.



The propagation delays of the CMOS inverter for varying rise and fall times are tabulated below.

| Input $t_r$ and $t_f$ (t) | $t_{pLH}$ (ns) | $t_{pHL}$ (ns) | $t_p$ (ns) |
|---|---|---|---|
| 0 ns | 0.33 | 0.6 | 0.465 |
| 50 ns | 2.8 | 2.867 | 2.8335 |
| 100 ns | 3.652 | 3.395 | 3.5235 |
| 150 ns | 4.17 | 3.8 | 3.985 |
| 200 ns | 4.6 | 4.158 | 4.379 |

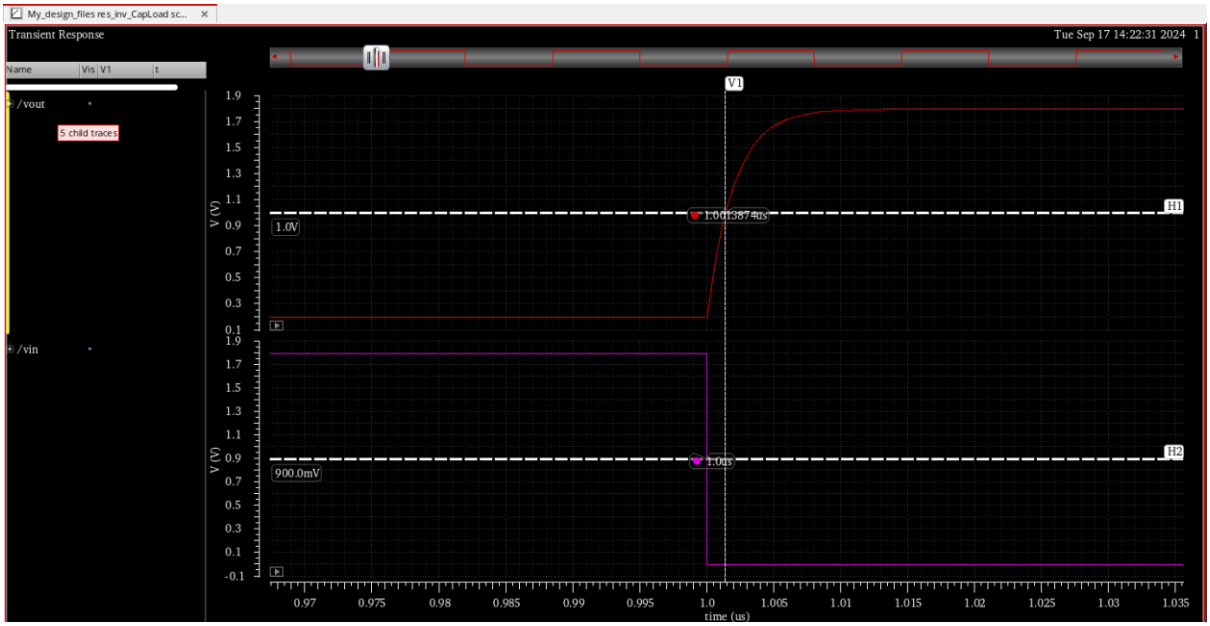
## Circuit Schematic for Resistive inverter with load capacitance:



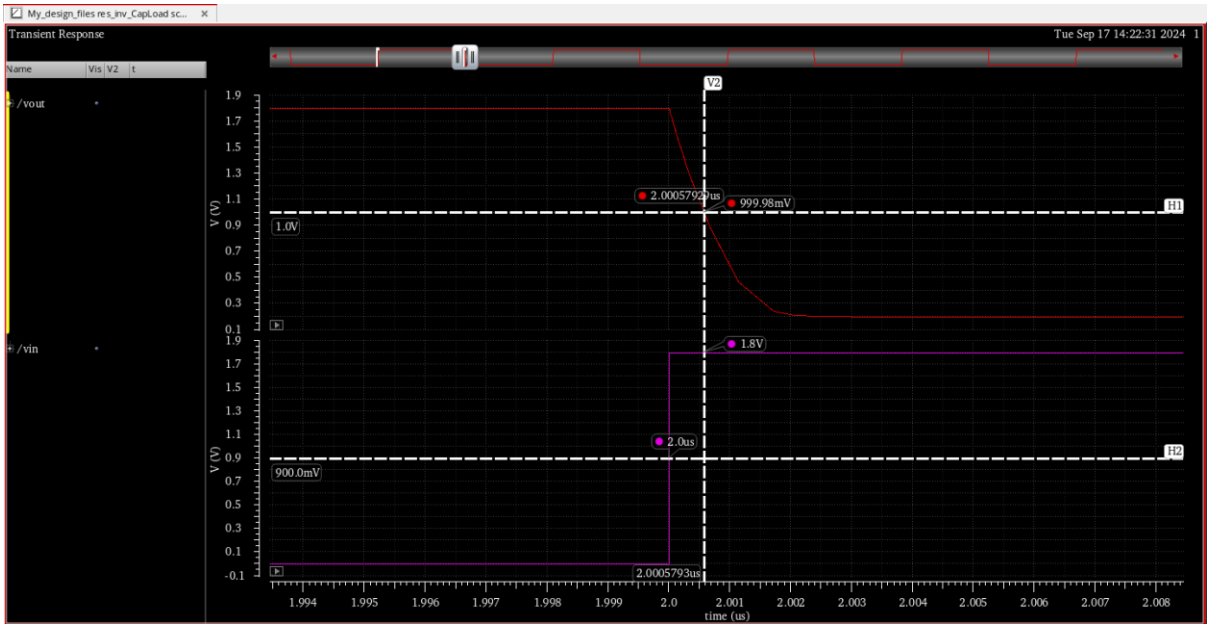

## Transient analysis:

Transient analysis was performed with input waveform of period 2µs and pulse width 1µs. For the resistive, $V_{OL} \neq 0V$. Thus, we get $V_{out\ 50\%} = 1V$.

The below graph shows how $t_{pLH}$ was calculated for a 0 ns fall time input.

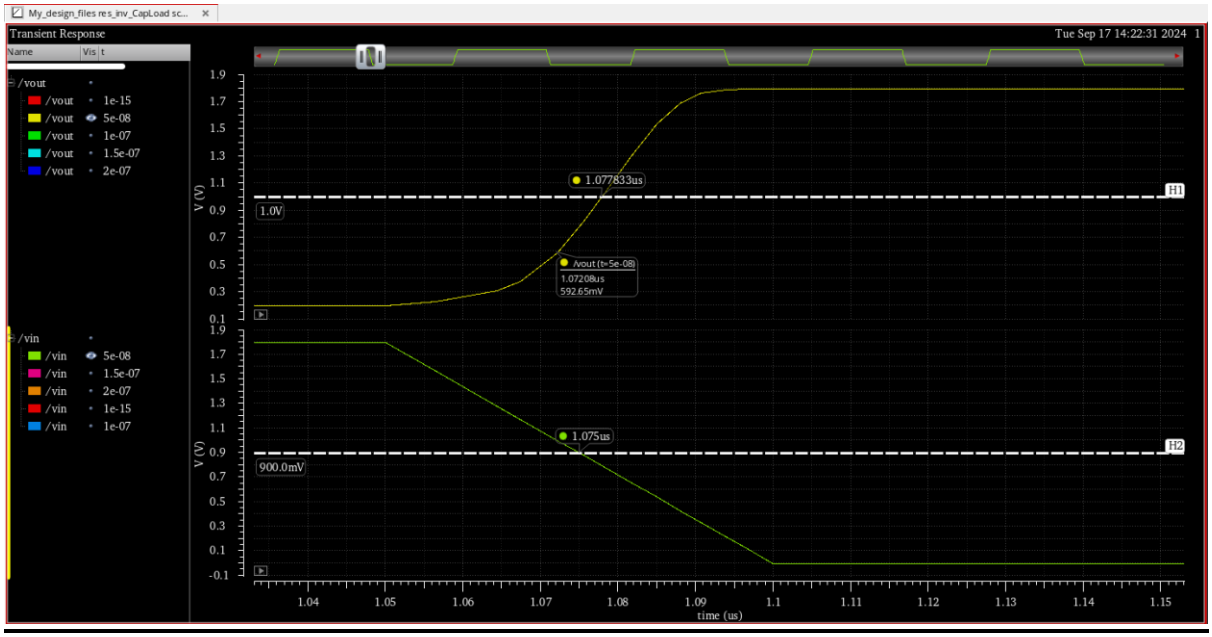



The graph below shows how $t_{pHL}$ was calculated for a 0 ns rise time input.

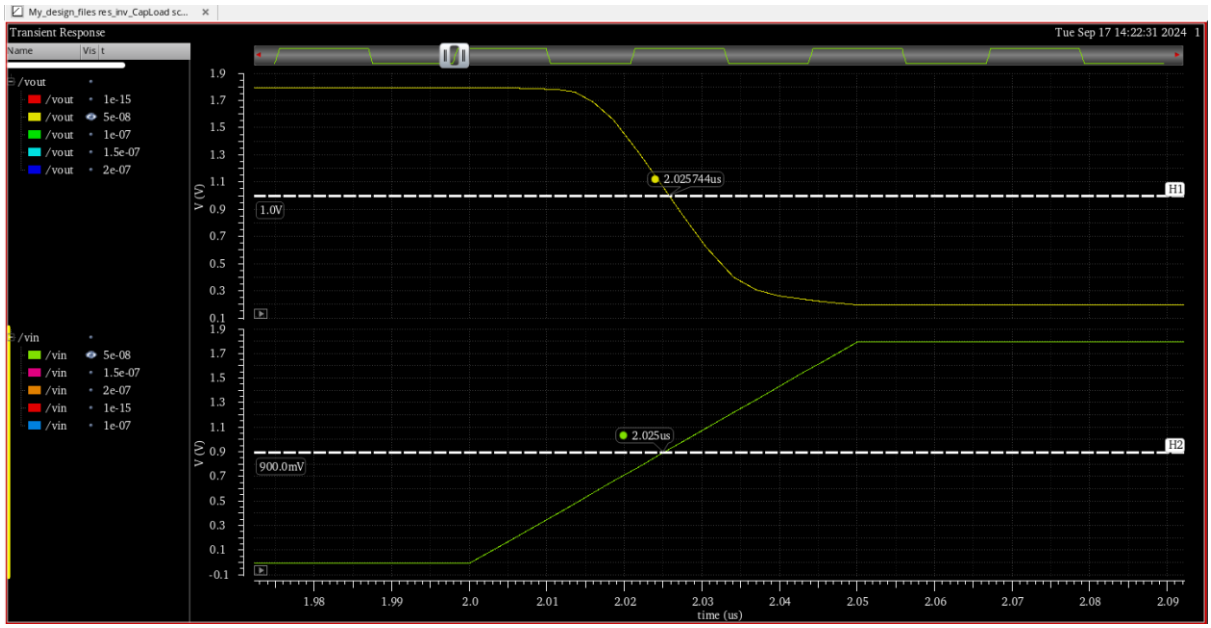


## Parametric analysis with varying $t_r$ and $t_f$

The below graph shows $t_{pLH}$ for $t_r = t_f = 50$ ns.




The below graph shows $t_{pHL}$ for for $t_r = t_f = 50$ ns.



The propagation delays of the resistive inverter for varying rise and fall times is tabulated below.

| Input $t_r$ and $t_f$ (t) | $t_{pLH}$ (ns) | $t_{pHL}$ (ns) | $t_p$ (ns) |
|---|---|---|---|
| 0 ns | 1.38 | 0.579 | 0.9795 |
| 50 ns | 2.88 | 0.744 | 1.812 |
| 100 ns | 3.95 | -0.327 | 1.8115 |
| 150 ns | 5.006 | -1.399 | 1.8035 |
| 200 ns | 6.101 | -2.499 | 1.801 |

## ii. Average current method for CMOS inverter

$k_n = 446.52\ \mu A/V^2$ ; $W_n = 220nm$, $L_n = 180\ nm$

$k_p = 625.34\ \mu A/V^2$ ; $W_p = 1220nm$, $L_p = 180\ nm$

$\tau_{PLH}$ → Average of $\underbrace{I_D(V_{OL}, V_{OL})}_{\text{Saturation}}$ and $\underbrace{I_D(V_{OL}, V_{50\%})}_{\text{Linear.}}$

$$I_{avg} = \frac{1}{2}\left[ I_{D_p}(V_{OL}, V_{OL}) + I_{D_p}(V_{OL}, V_{50\%}) \right]$$

$$= \frac{1}{2}\left[ \frac{k_p}{2}(V_{GS} - V_{tp})^2 + k_p\left\{ V_{DS}(V_{GS} - V_{tp}) - V_{DS}^2/2 \right\} \right]$$

$$= \frac{k_p}{2}\left[ \frac{(-0.504)^2}{2} + \left\{ (-0.9)(-(-0.504)) - \frac{(-0.9^2)}{2} \right\} \right]$$

$$= \frac{k_p}{2}\left[ 0.839 + 0.761 \right]$$

$$= 500.272\ \mu A$$

$$\tau_{PLH} = \frac{C_L(V_{50\%} - V_{OL})}{I_{avg}} = \frac{100 \times 10^{-15} \times 0.9}{500.27 \times 10^{-6}}$$

$$\boxed{\tau_{PLH} = 0.179\ ns}$$

$\tau_{P_{HL}}$ → Average of $I_D(V_{OH}, V_{OH})$ (Saturation) and $I_D(V_{OH}, V_{50\%})$ (Linear)

$$I_{avg} = \frac{1}{2}\left[I_{D_n}(V_{OH}, V_{OH}) + I_{D_n}(V_{OH}, V_{50\%})\right]$$

$$= \frac{1}{2}\left[\frac{k_n}{2}(V_{GS}-V_{tn})^2 + k_n\left\{(V_{GS}-V_{tn})V_{DS} - V_{DS}^2/2\right\}\right]$$

$$= \frac{k_n}{2}\left[\frac{(1.8-0.432)^2}{2} + \left\{(1.8-0.432)(0.9) - (0.9^2/2)\right\}\right]$$

$$= \frac{k_n}{2}\left[0.9368 + 0.8262\right] = 393.428\,\mu A$$

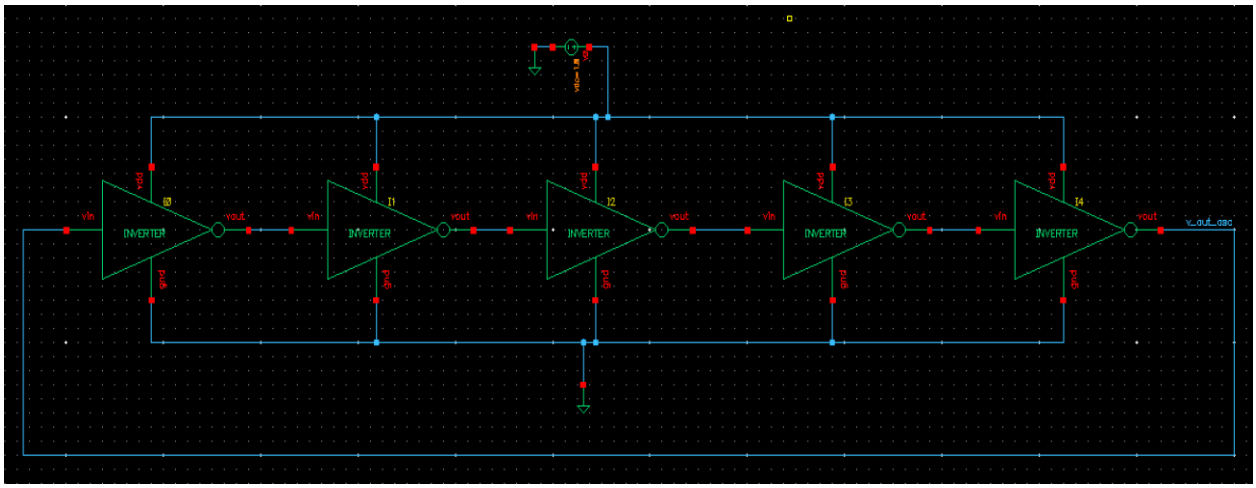
$$\therefore \tau_{P_{HL}} = \frac{C_L \times (V_{OH} - V_{50\%})}{I_{avg}} = \frac{100 \times 10^{-15} \times 0.9}{393.42 \times 10^{-6}}$$

$$\boxed{\tau_{P_{HL}} = 0.228\ ns}$$

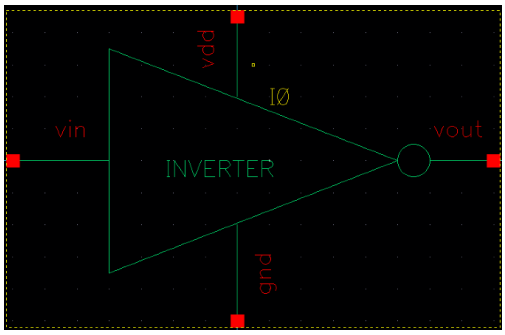
$$\Rightarrow \tau_P = \frac{\tau_{P_{HL}} + \tau_{P_{LH}}}{2} = \boxed{0.2035\ ns} \rightarrow \text{Average Propagation Delay.}$$

## iii. 5-Stage Ring Oscillator

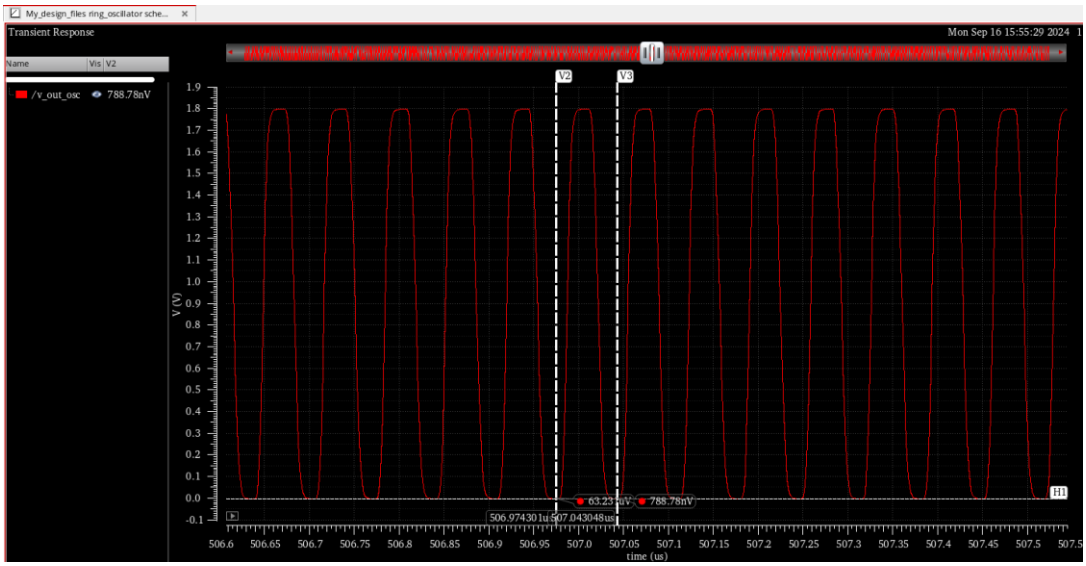
A ring oscillator consists of an odd number of inverters connected in cascade and the output of the last inverter is connected to the input of the first inverter. The inverter used the same CMOS inverter used in part (i) of this experiment with a load capacitance of 100f F.



The symbol of the CMOS inverter is shown below.




To find the frequency of oscillation, we need to find the time period of oscillation.




The time period comes out to be 0.0687µs for a load capacitance of 100f F at the output node of the CMOS inverter. The frequency is the reciprocal of the time period which is **140.73 MHz**.