BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI

I SEMESTER 2024-25, MEL G621 – VLSI DESIGN

LAB ASSIGNMENT – 3

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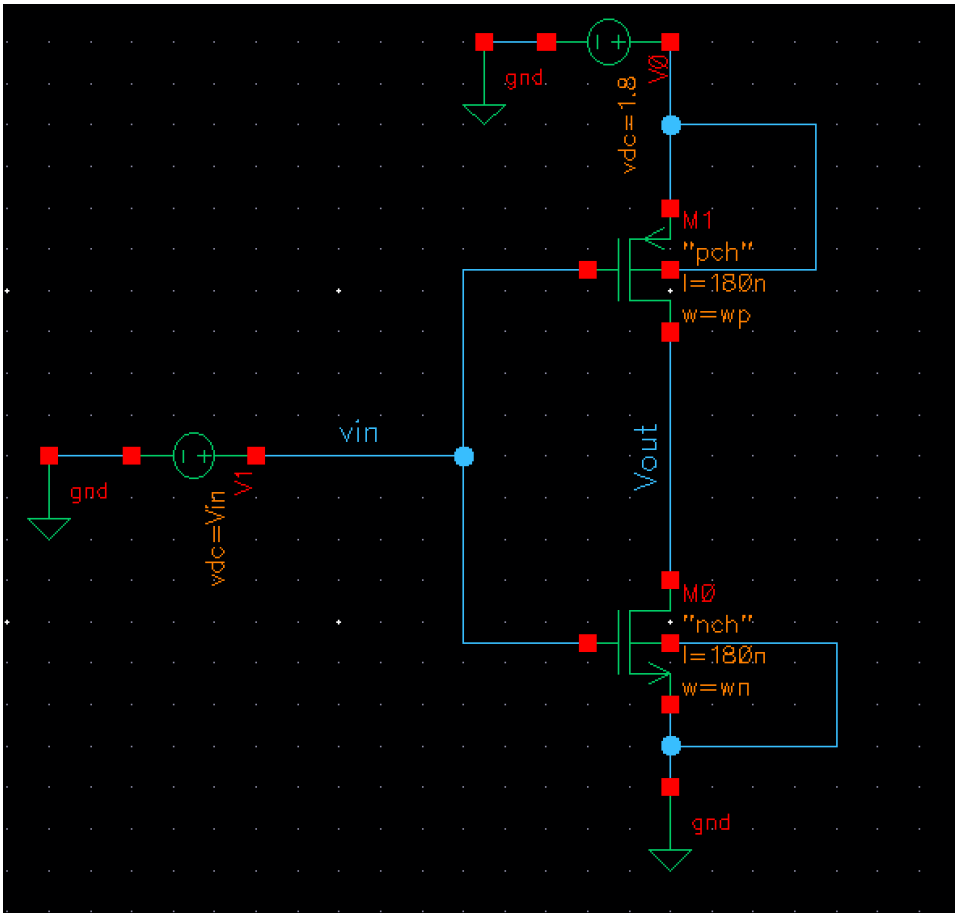
AIM: To draw the schematic of CMOS inverter and plot its Voltage Transfer Characteristics (VTC) for varying NMOS & PMOS transistor width and

i. determining the value of critical points, noise margins and switching threshold for each case.
ii. determining the value of w_p and hence mobility ratio for which the switching threshold becomes $V_{DD}/2$.

Tools used: Cadence Virtuoso

Circuit Schematic:



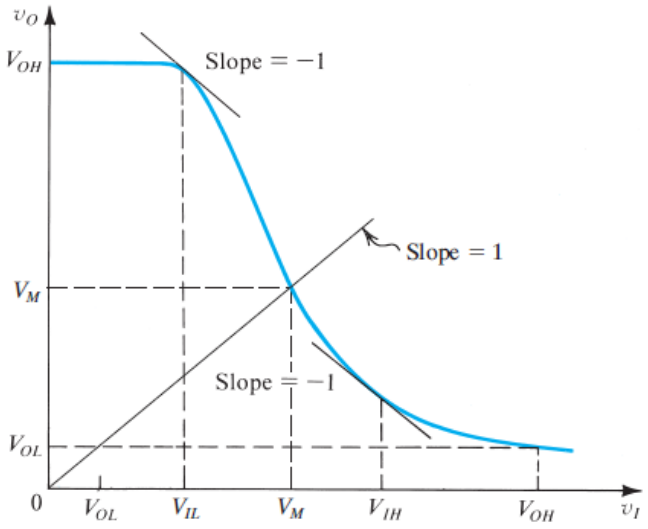
VOLTAGE TRANSFER CHARACTERISTICS:

A typical VTC plot for a CMOS inverter is shown below with clearly marked critical points. Noise margins were calculated using the formula:

$$NM_L = V_{OH} - V_{IH}$$

$$NM_H = V_{IL} - V_{OL}$$

The switching threshold of the inverter is the point where $V_{in} = V_{out}$. For a symmetric inverter, it is equal to $V_{DD}/2$. This indicates that both the pull-up and pull-down networks are equally powerful.



NMOS Transistor parameters:

Model name– 'nch'

Transistor width (w_n) = 220nm

Transistor length = 180nm

PMOS Transistor parameters:

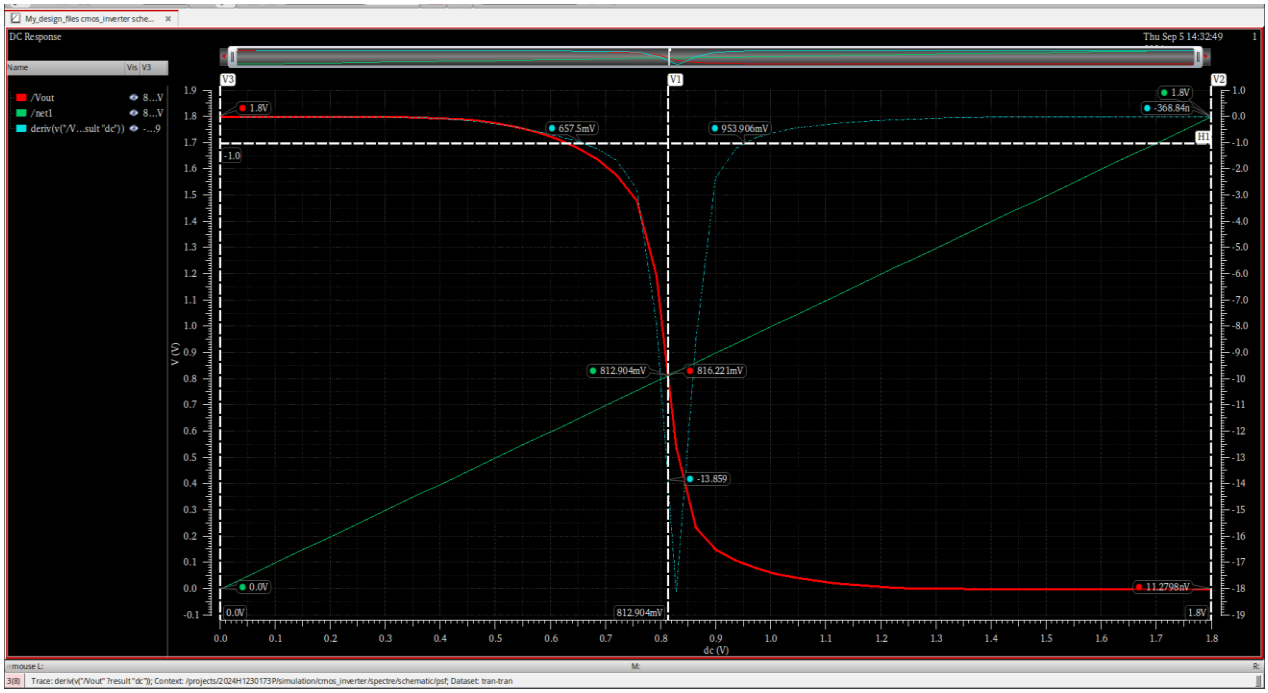
Model name– 'pch'

Transistor width (w_p) = 660nm

Transistor length = 180nm

1. Voltage transfer characteristics

VTC is plotted by measuring changes in V_{out} as V_{in} is swept from 0 to 1.8V. Below graph shows the VTC for above mentioned parameters.



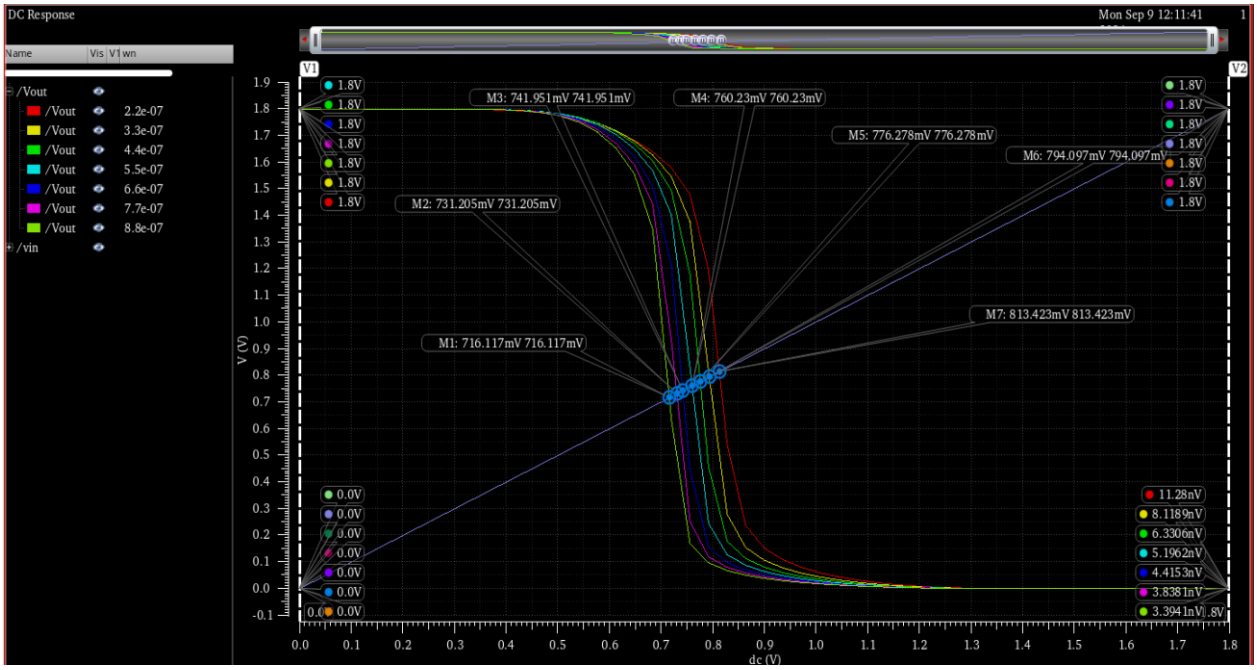
Derivative of the curve is plotted (in cyan above) using 'deriv' function to get the slope of VTC. V_{IL} and V_{IH} were marked where slope of the curve was '-1'. Corresponding V_{OL} and V_{OH} were found.

V_{IL}(mV)	V_{IH}(mV)	V_{OL}(nV)	V_{OH}	V_{th}(mV)	NM_L(mV)	NM_H(mV)
657.5	953.91	11.27	1.8	812.904	657.5	846.09

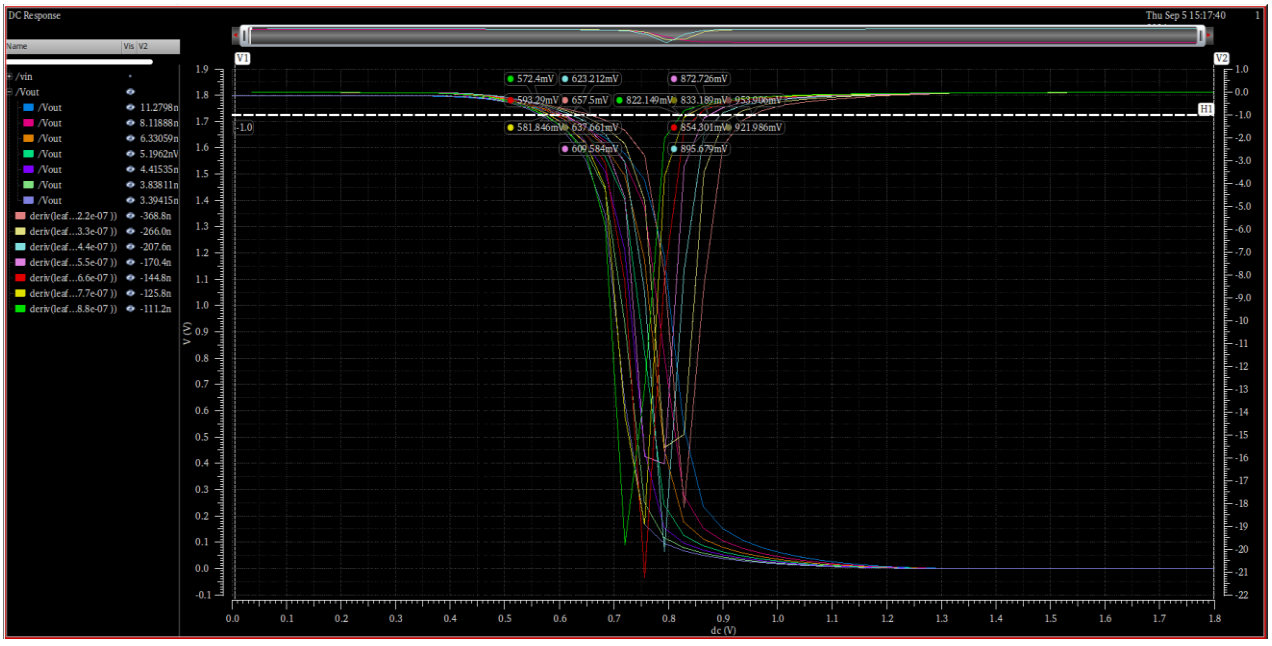
2. VTC with varying transistor width 'w_n'

Parametric analysis was performed by sweeping V_{in} from 0 to 1.8V for different values of w_n to observe the critical points and noise margins.

The VTCs for w_n varied from 220nm to 880nm at steps of 110nm is plotted. The below plot shows the critical points V_{OL} & V_{OH}. The switching thresh-olds points are marked at the intersection point of the VTC and V_{in} curves. w_p was kept at 660nm.



The below plot shows the V_{IL} and V_{IH} values for the corresponding VTC's derivatives. The points are marked where slope = -1.



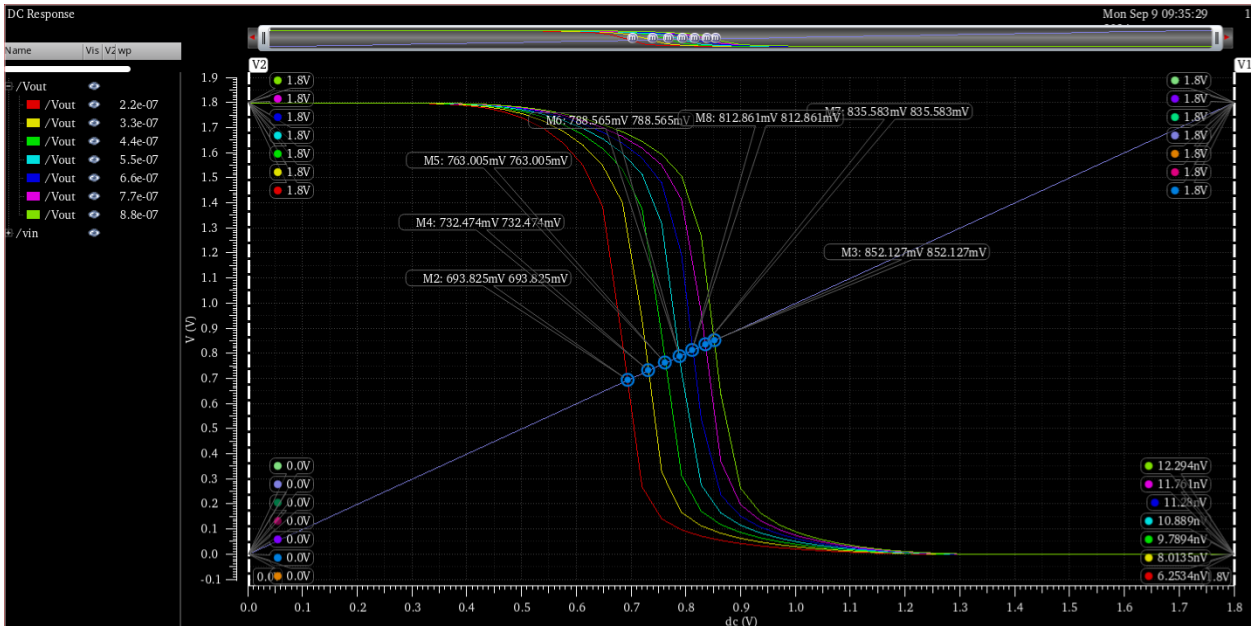
The data from w_n parametric analysis is tabulated below.

W_n(nm)	V_{IL}(mV)	V_{IH}(mV)	V_{OL}(nV)	V_{OH}(V)	V_{th}(mV)	NM_L(V)	NM_H(V)
220	657.5	953.906	11.27	1.8	812.904	657.5	846.09
330	637.661	921.986	8.11	1.8	794.097	637.661	878.01
440	623.212	895.679	6.33	1.8	776.278	623.212	904.32
550	609.212	872.726	6.259	1.8	760.230	609.212	927.27
660	593.29	854.301	5.31	1.8	741.951	593.29	945.7
770	581.846	833.189	4623	1.8	731.205	581.846	966.81
880	572.4	822.149	4.088	1.8	716.117	572.4	977.85

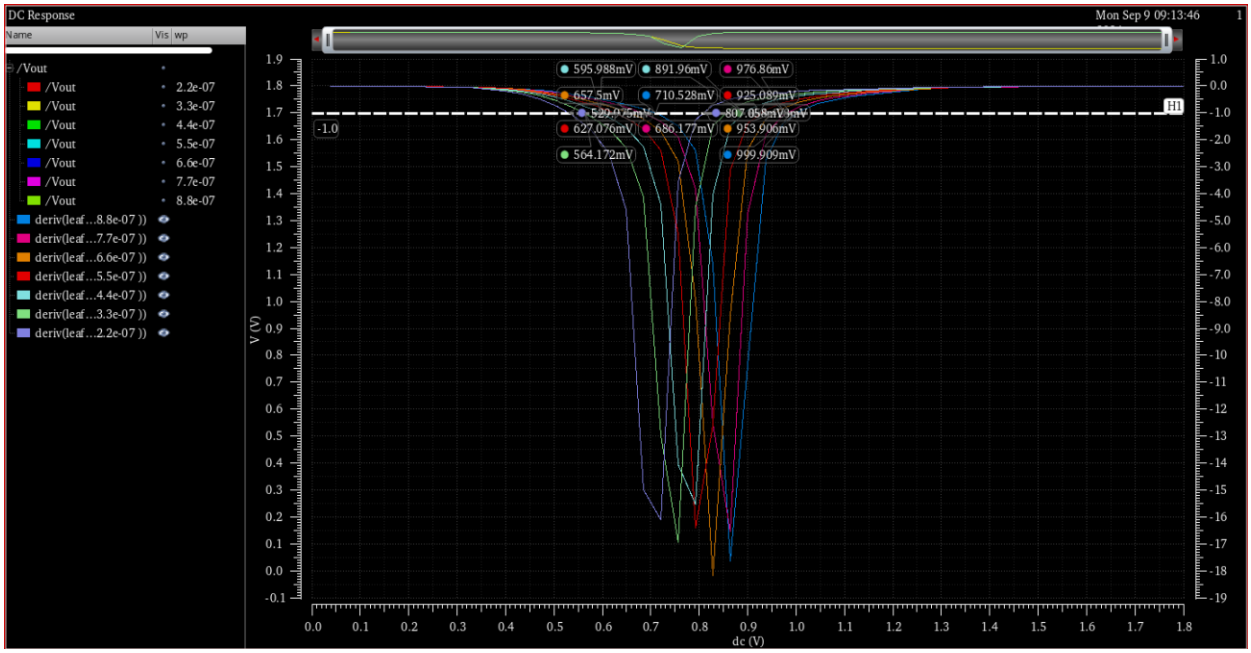
3. VTC with varying transistor width 'w_p'

Parametric analysis was performed by sweeping V_{in} from 0 to 1.8V for different values of w_p to observe the critical points and noise margins.

The VTCs for w_p varied from 220nm to 880nm at steps of 110nm is plotted. w_p was kept at 220nm. The below plot shows the critical points V_{OL} & V_{OH}. The switching thresholds points are marked at the intersection point of the VTC and V_{in} curves.



The below plot shows the V_{IL} and V_{IH} values for the corresponding VTC's derivatives. The points are marked where slope = -1.

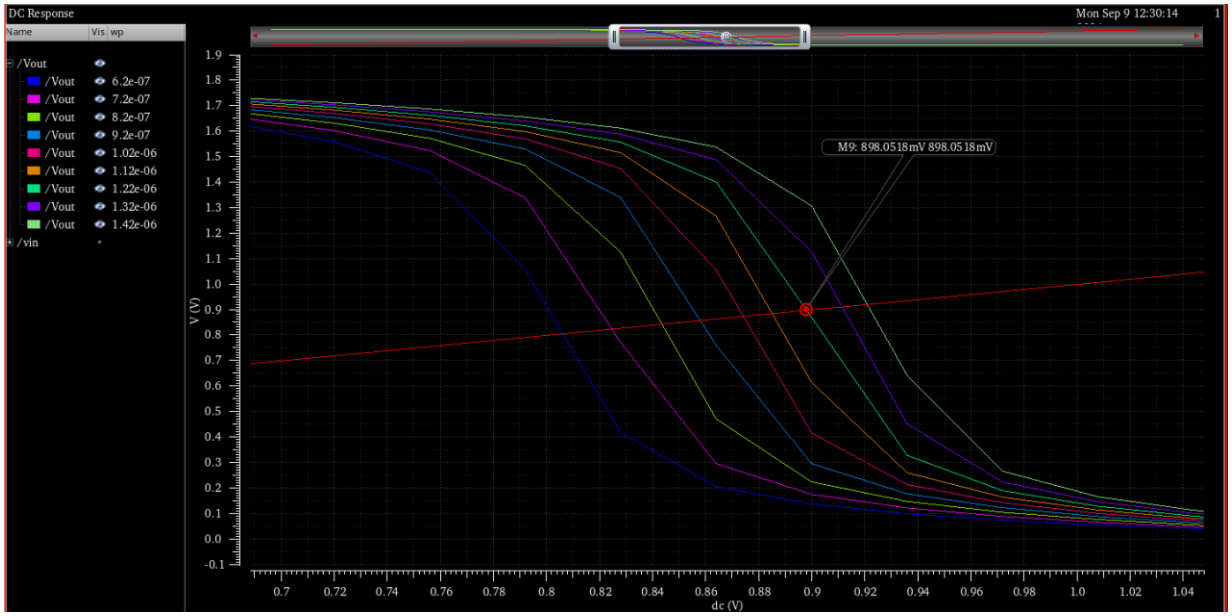


W_p(nm)	V_{IL}(mV)	V_{IH}(mV)	V_{OL}(nV)	V_{OH}(V)	V_{th}(mV)	NM_L(V)	NM_H(V)
220	529.975	807.058	6.253	1.8	693.825	529.975	992.94
330	564.172	854.428	8.014	1.8	732.474	564.172	945.57
440	595.988	891.96	9.789	1.8	763.581	595.988	908.04
550	627.076	925.089	10.889	1.8	788.565	627.076	874.91
660	657.5	953.906	11.28	1.8	812.861	657.5	846.09
770	686.117	976.86	11.761	1.8	835.583	686.117	823.14
880	710.528	999.909	12.294	1.8	825.127	710.528	800.09

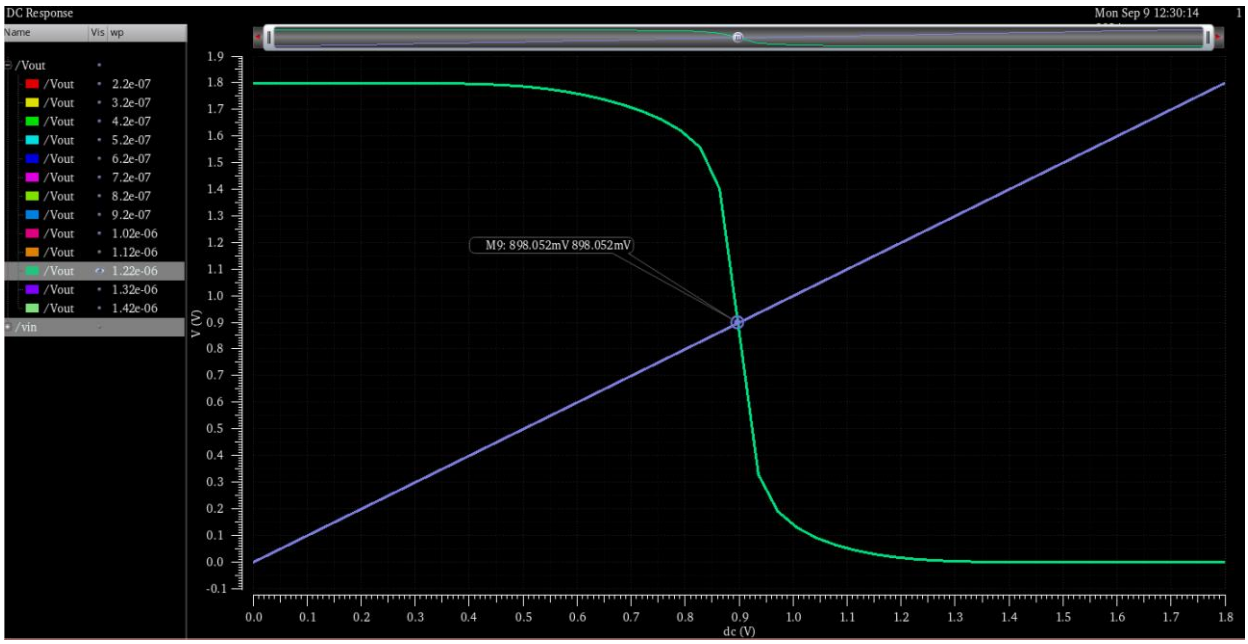
4. w_p for symmetric response of Inverter

An inverter is said to have a symmetric response if switching threshold is $V_{DD}/2$. From above table, we see that V_{th} is 825mV for w_p = 880nm. Thus, to get to 0.9V, we need to further increase the width of PMOS. VTCs are plotted for w_p varied from 620nm to 1420nm. The plots are shown below.

The plot with w_p = 1220nm is noted to have switching threshold closest to $V_{DD}/2$ = 0.9V at 898.05mV. (marker shown below)



The response of this symmetric inverter is shown below.



We know that:

$$\mu_n / \mu_p = w_p / w_n = 1220nm/220nm = 5.54$$

$$\mathbf{\mu_n = (5.54)\ \mu_p}$$

The mobility of electrons is about 5.54 times that of holes. Thus w_p must be made 5.54 times of w_n to get equally strong pull-up and pull-down networks.

Inference:

The critical points and noise margins for varying transistor widths w_p and w_n were calculated. From the tabulations, we observe that:

i. As w_n is increased, the VTC curve starts shifting to the left, i.e., the NMOS transistor's strength increases. The pull-down network becomes stronger.
ii. As w_p is increased, the VTC curve starts shifting to the right, i.e., the PMOS transistor's strength increases. The pull-up network becomes stronger.
iii. Due to lower mobility of holes, the PMOS must be sized appropriately to get a symmetric response from the inverter.