BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI

I SEMESTER 2024-25, MEL G621 – VLSI DESIGN

LAB ASSIGNMENT – 8

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AIM: In this experiment, we are to:

1. To implement a NAND-2 gate with load capacitance 10fF using dynamic logic.

2. To implement a full adder using static CMOS logic and:

i. Optimize the transistor sizes for best performance.

ii. Identify the critical path.

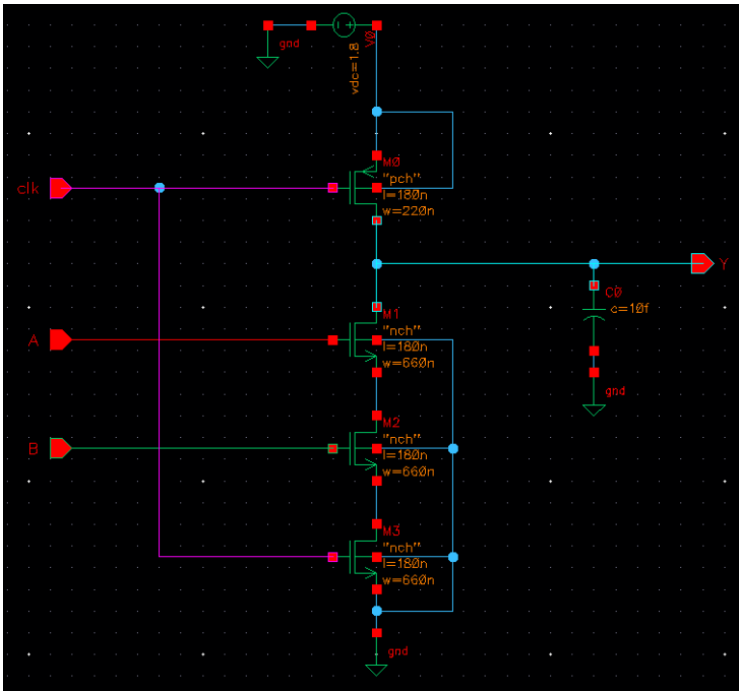
iii. Calculate the propagation delays.

3. To implement a full subtractor using static CMOS logic and calculate the propagation delay.

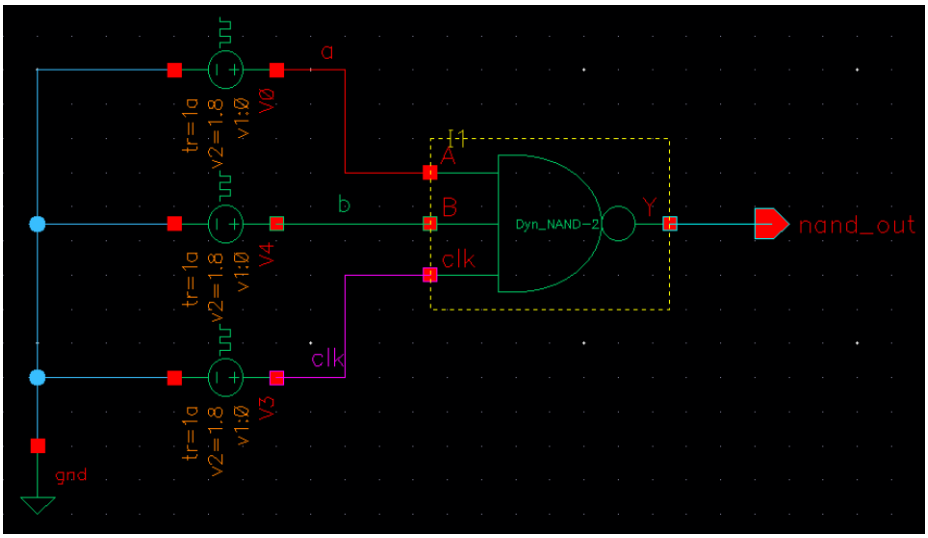
Tools used: Cadence Virtuoso

1. NAND-2 using dynamic logic

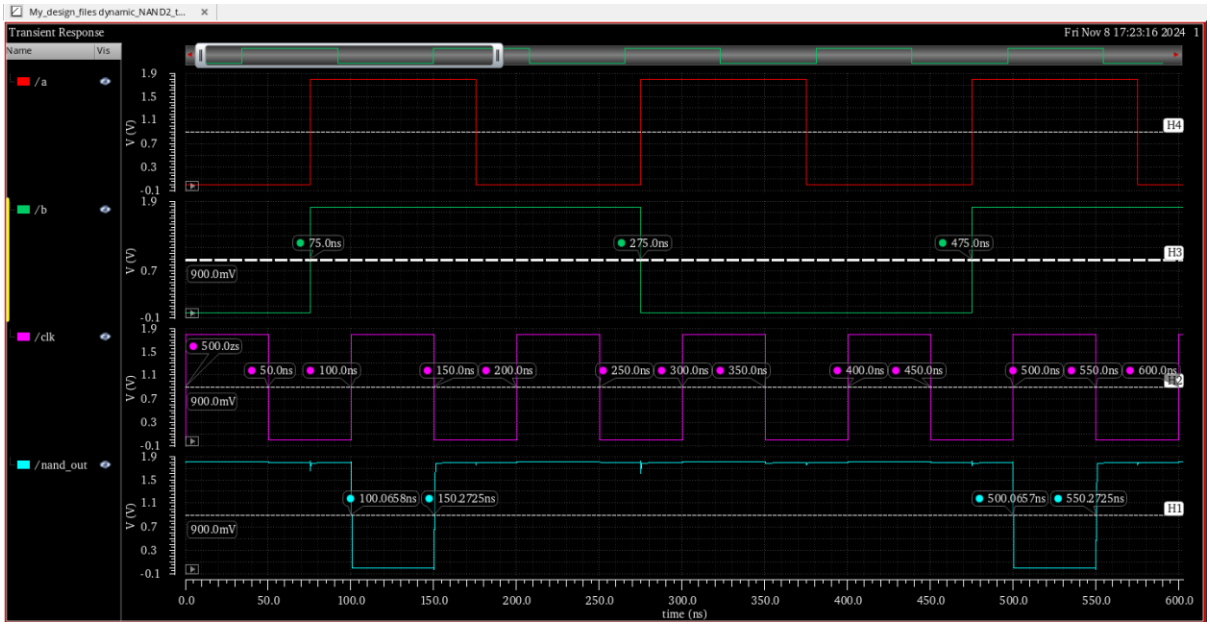
The circuit schematic with sized with respect to 2:1 inverter is shown below.



A symbol was created for the design. Test circuit is shown below.



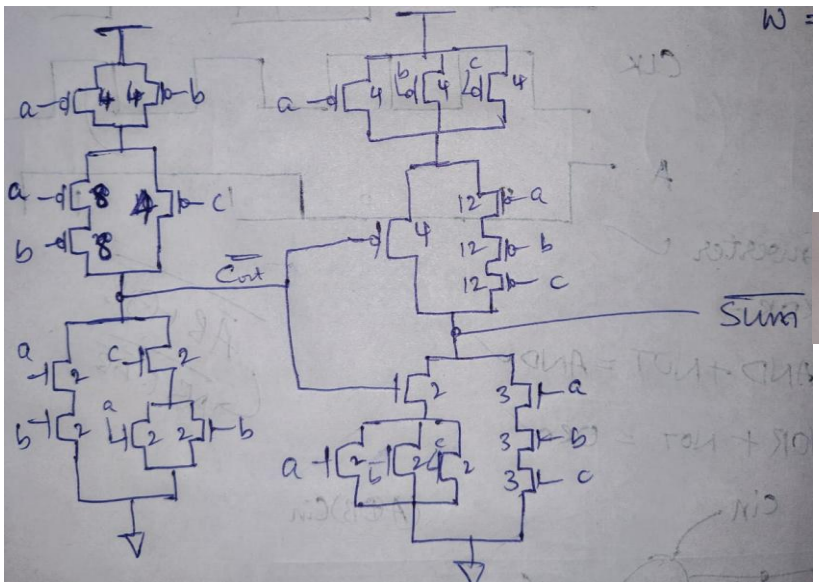
The simulation waveforms are shown below. The inputs can affect the output only during the evaluation phase. During the evaluation phase, the output can either remain at V_{DD} (maintained from pre-charge) or fall to 0. So, its rise time is not defined (=0).



The circuit functionality has been verified. From the waveforms, we observe the t_{pHL} = 0.0658ns (C_L = 10f F).

2. Full adder using static CMOS logic

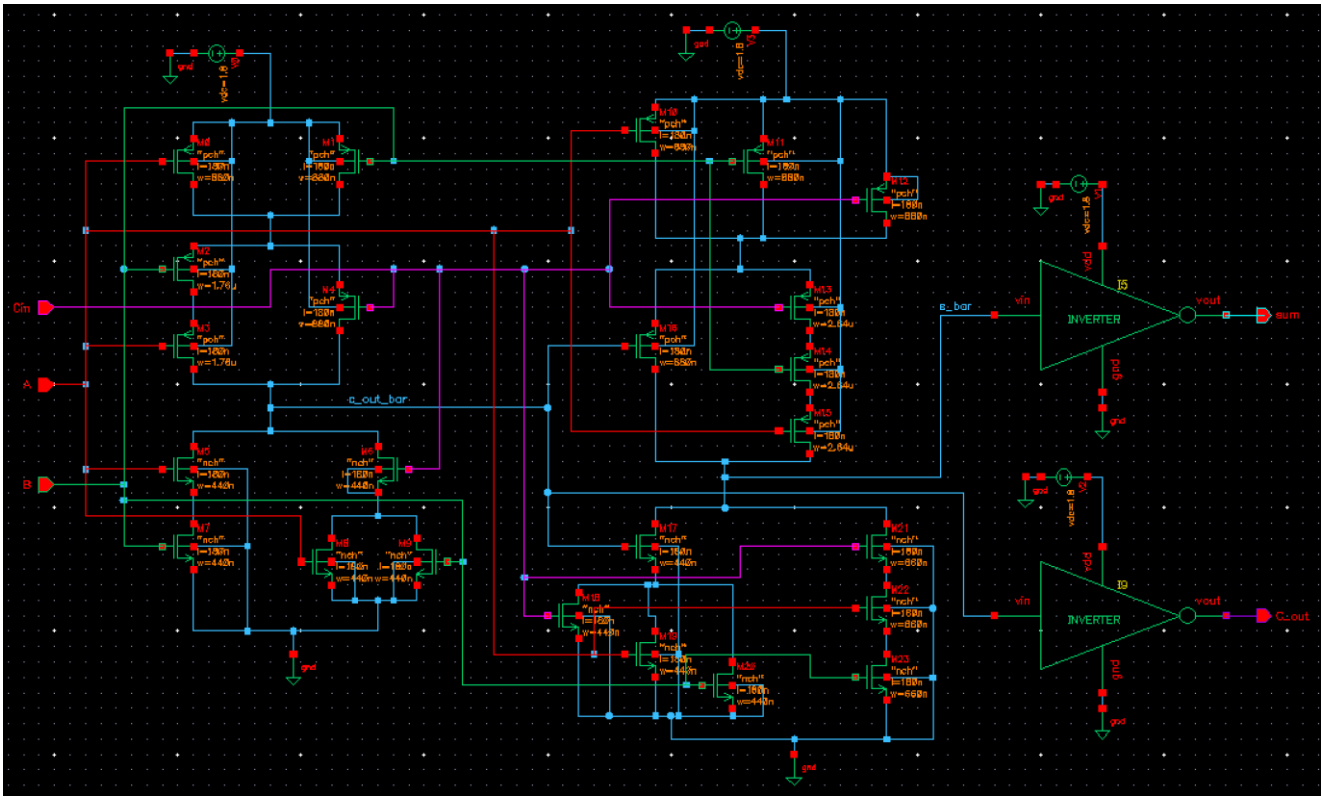
The full adder is realized by generating the carry first, and then use the carry to generate sum. This is done to optimize the time and number of transistors involved in the design of the traditional XOR to realize the sum operation. The circuit sized according to 2:1 inverter is shown below.



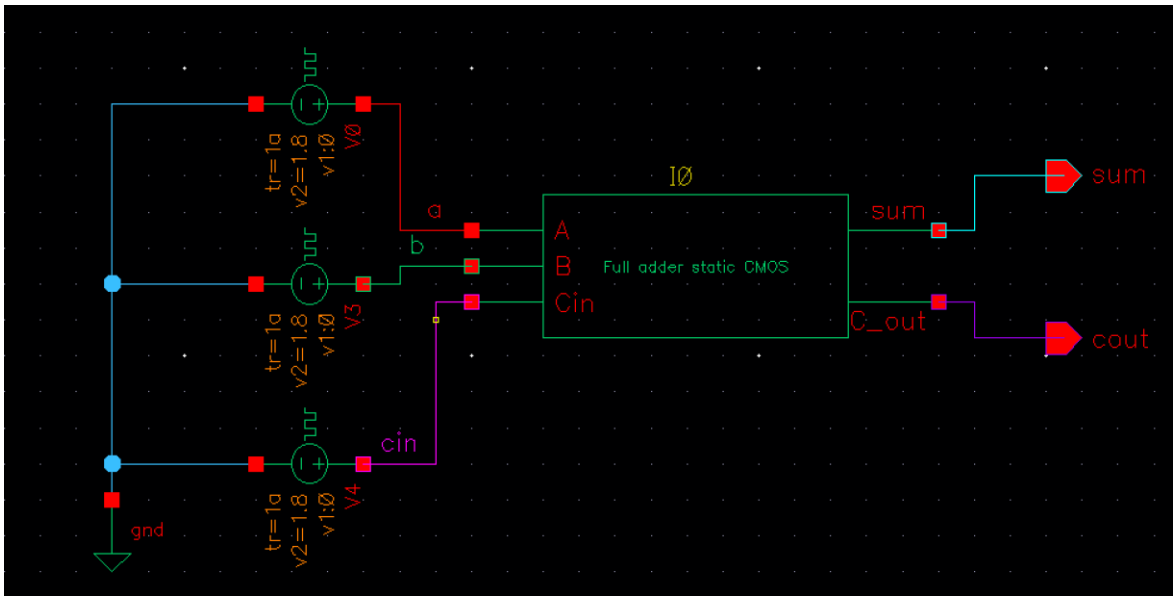
$$\overline{C_{out}} = \overline{a.b + c.(a+b)}$$

$$\overline{Sum} = \overline{a.b.c + (a+b+c).C_{out}}$$

The circuit schematic is shown below.



A symbol was created for the design and its test circuit is shown below.



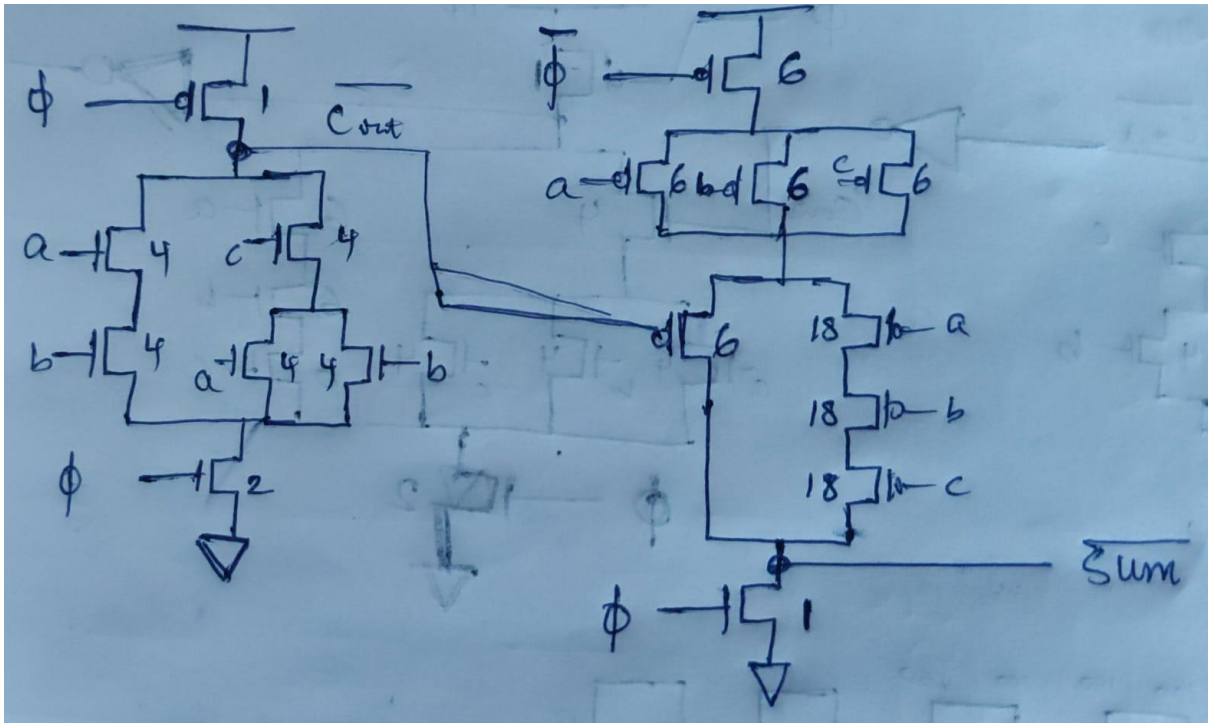
The simulation waveforms to test for functionality are shown below.

The 8 possible cases of the full adder are verified. From the above figure, best- and worst-case propagation delays are given in the table below.

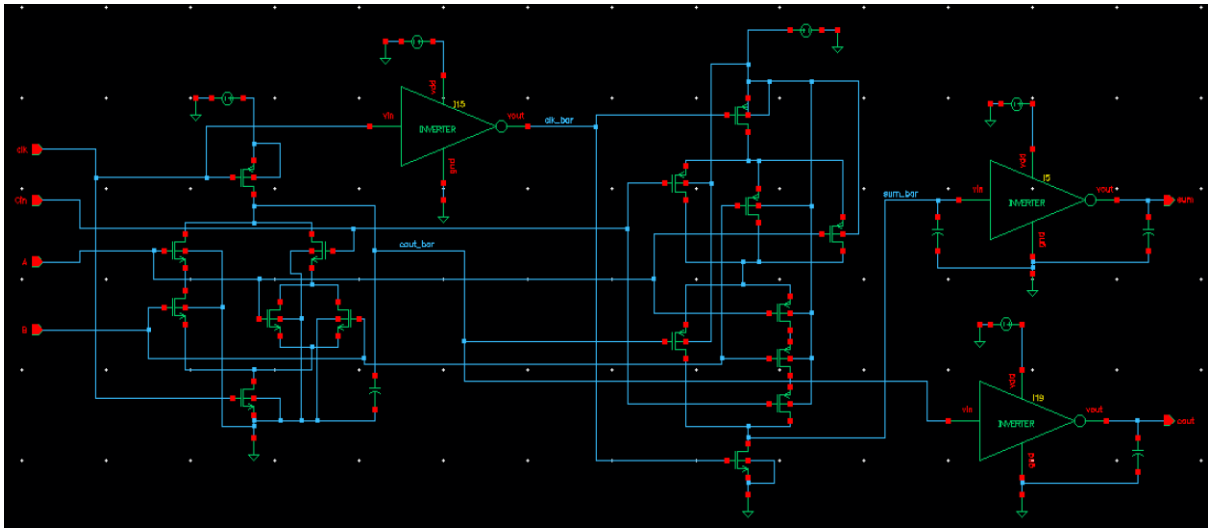
Sum Circuit	Worst case	t_{pLH} =0.309ns	t_{pHL} =0.328ns
	Best case	t_{pLH} =0.171ns	t_{pHL} =0.1693ns
Carry circuit	Worst case	t_{pLH} =0.176ns	t_{pHL} =0.234ns
	Best case	t_{pLH} =0.089ns	t_{pHL} =0.197ns

3. Full adder using dynamic logic

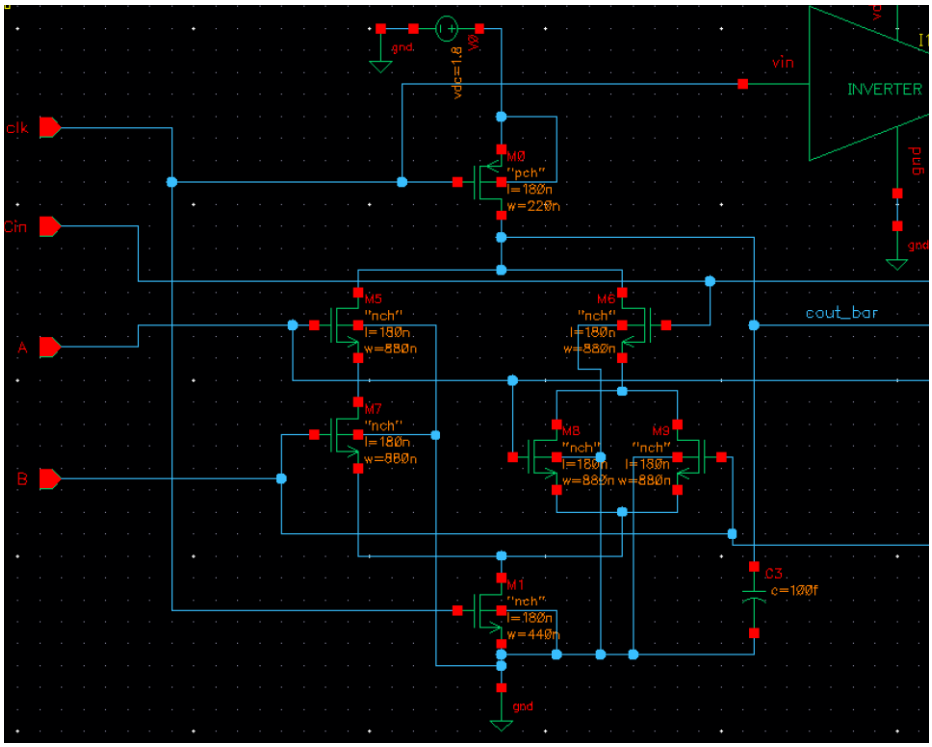
The dynamic logic circuit is realized using NORA logic, since there is cascading of sum circuit after the carry circuit. The carry is a n-dynamic and the sum is designed using p-dynamic circuit. 100fF capacitance is taken at output. The circuit sized according to 2:1 inverter is shown below.



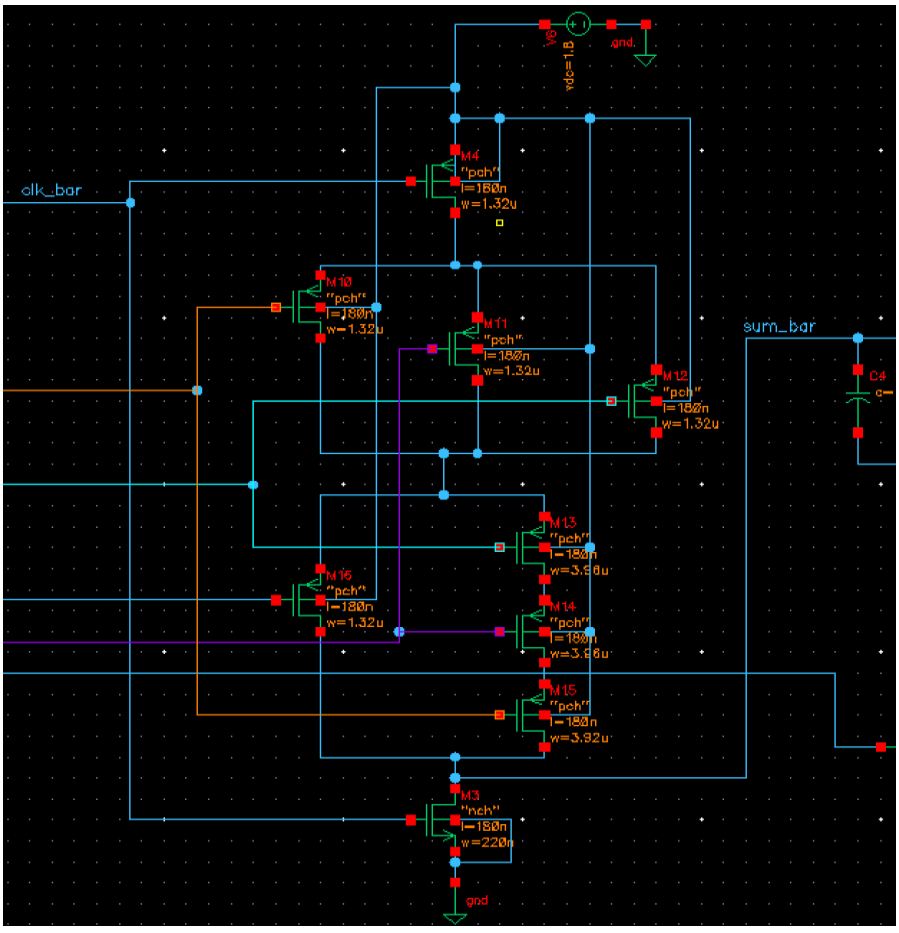
The circuit schematic is shown below.



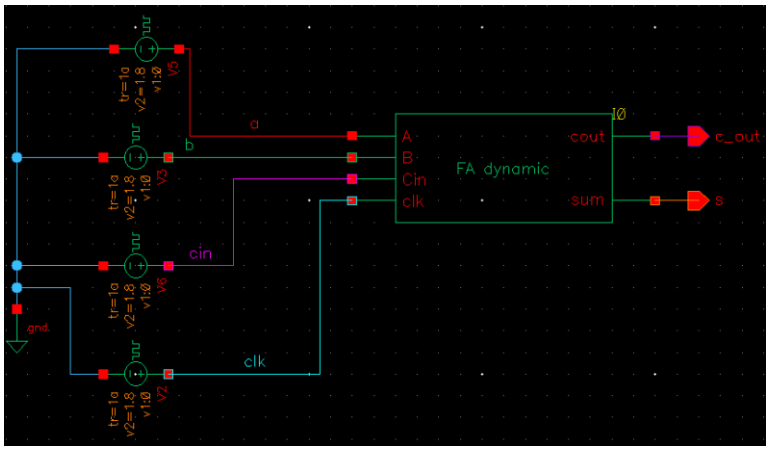
Carry circuit is shown below.



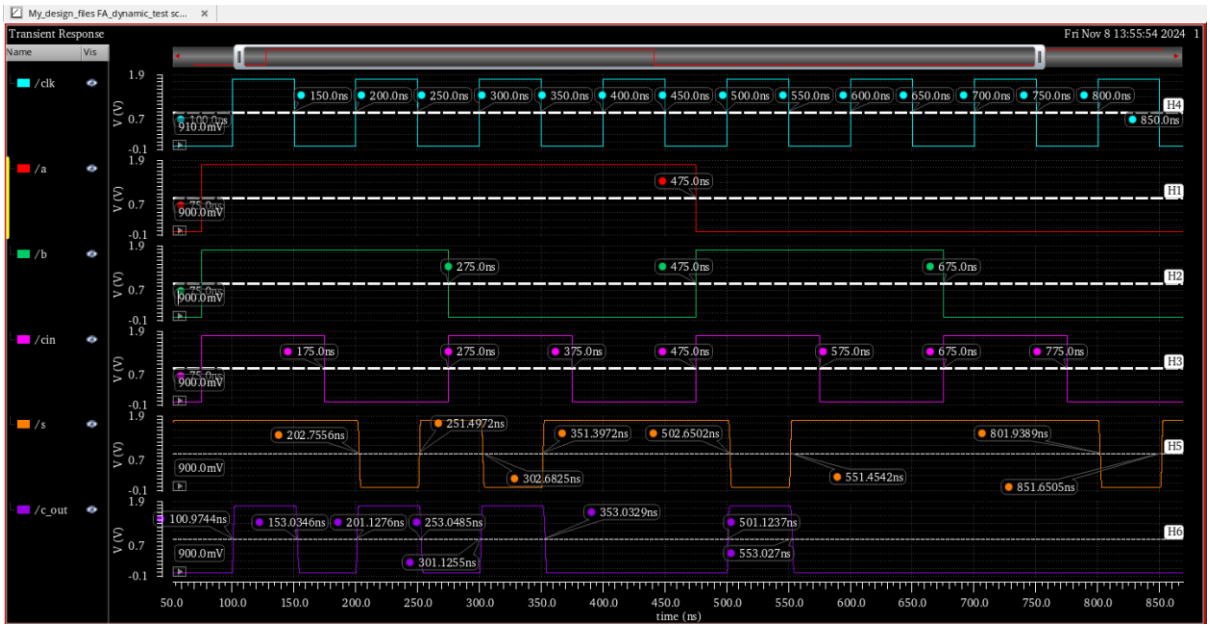
The sum circuit is shown below.



A symbol was created for the design and its test circuit is shown below.



The simulation waveforms are shown below for 8 clock cycles verifying the 8 output cases for a full adder. The outputs are reflected during the evaluate phase (positive level of the clock).

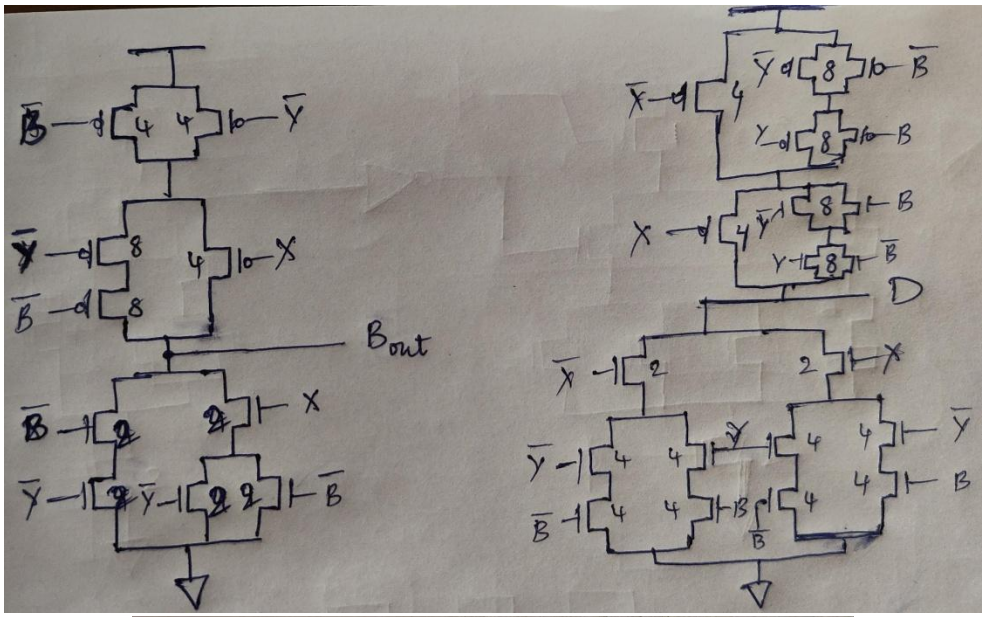


From the above figure, best- and worst-case propagation delays are given in the table below. The sum is a p-dynamic circuit with inverter at the output, so its output rise time cannot be defined. Similarly, the carry is a n-dynamic circuit with inverter at the output, so its fall time cannot be defined (=0).

Sum Circuit	Worst case	t_{pHL} =2.755ns
	Best case	t_{pHL} =1.397ns
Carry circuit	Worst case	t_{pLH} =1.123ns
	Best case	t_{pLH} =0.974ns

4. Full subtractor using static CMOS logic

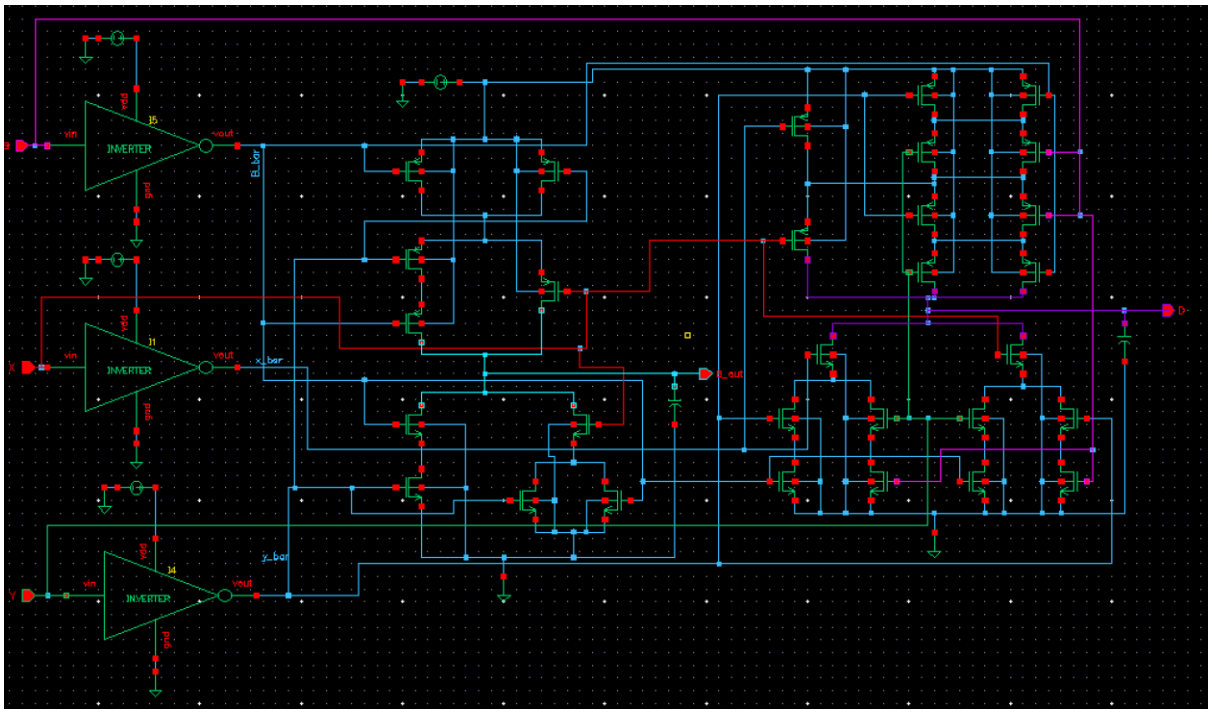
The circuit sized according to 2:1 inverter is shown below.



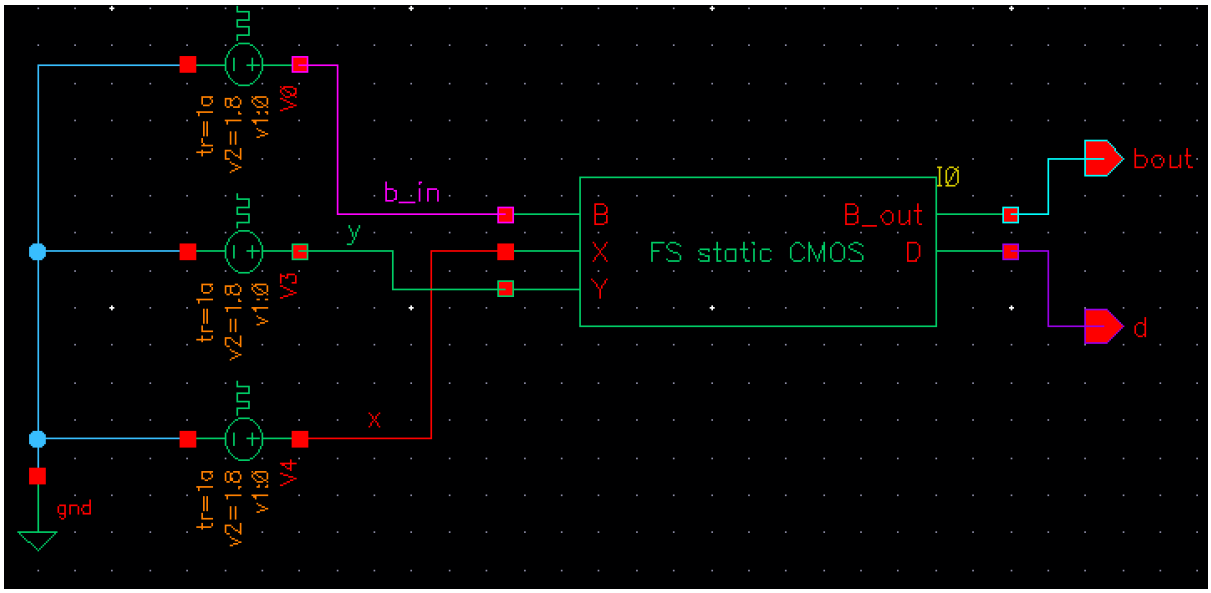
$$D = \overline{\bar{X}.(\bar{Y}\bar{B} + YB) + X.(\bar{Y}B + Y\bar{B})}$$

$$B_{out} = \overline{\bar{B}.\bar{Y} + X.(\bar{Y} + \bar{B})}$$

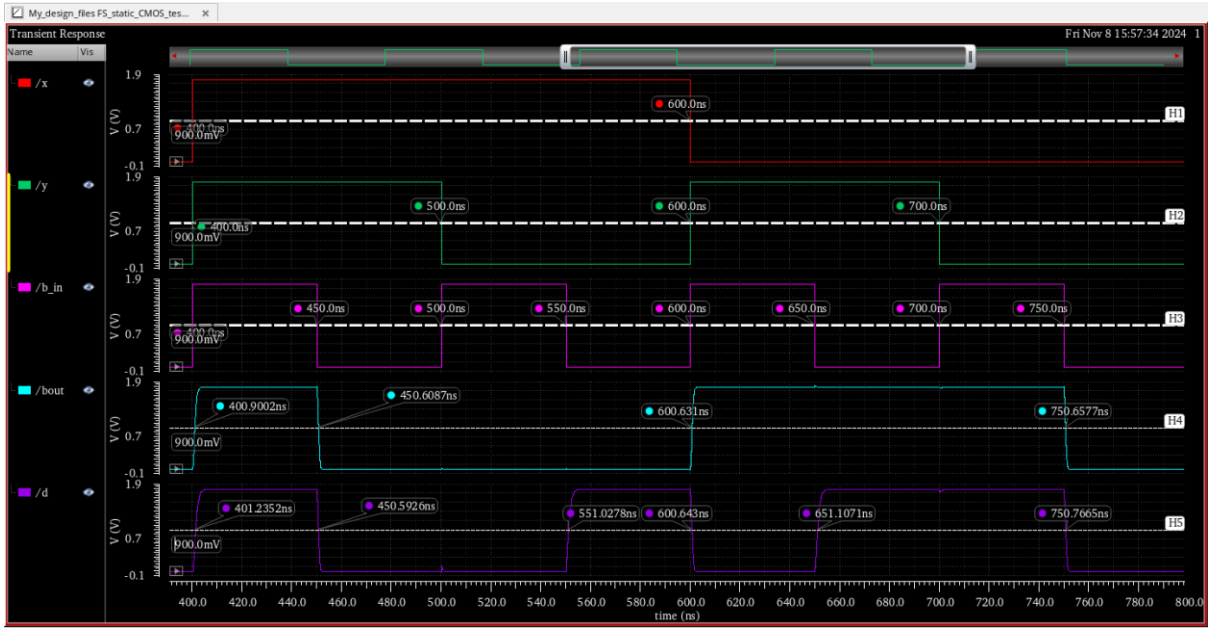
The schematic is shown below.



A symbol was created for the design and its test circuit is shown below.



The simulation waveforms to test for functionality are shown below.

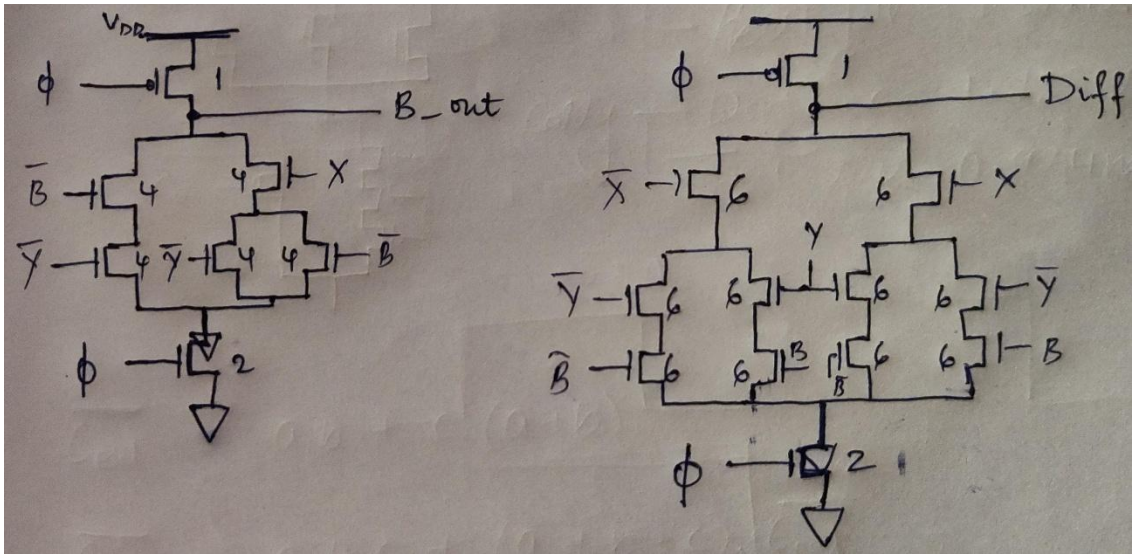


The 8 possible cases of the full subtractor are verified. From the above figure, best- and worst-case propagation delays are given in the table below.

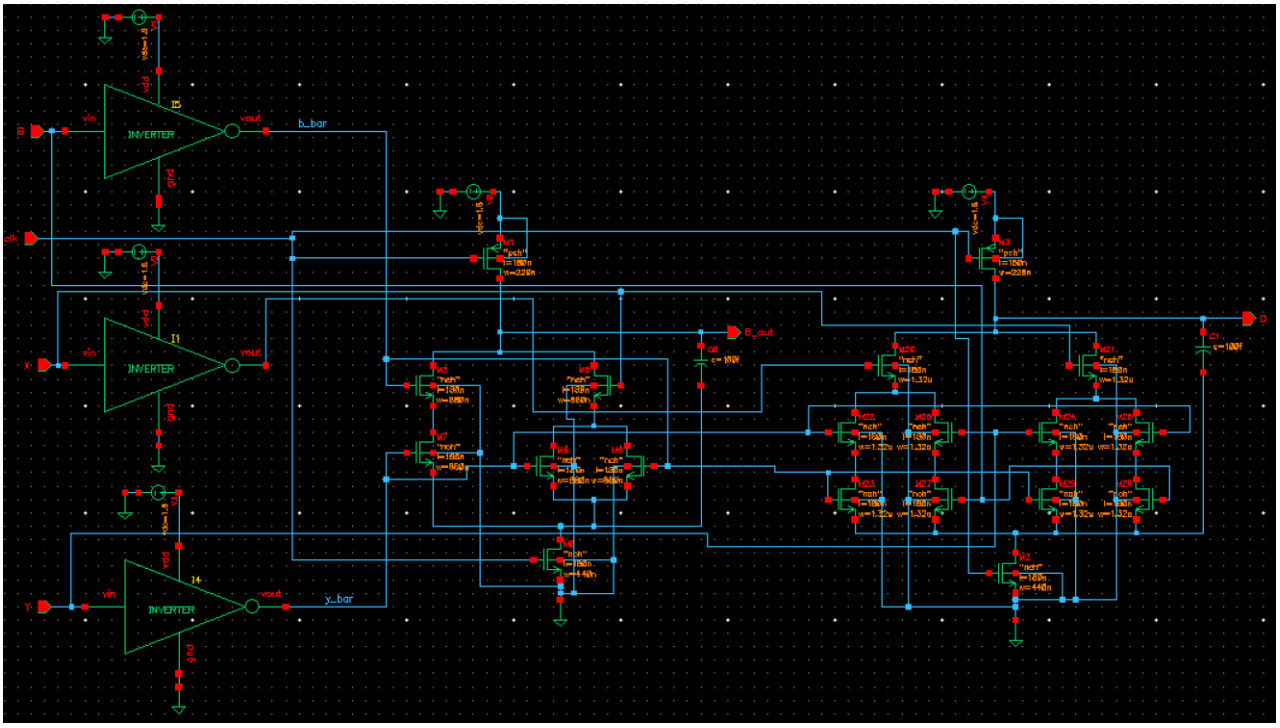
Difference Circuit	Worst case	t_{pLH} =1.235ns	t_{pHL} =0.766 ns
	Best case	t_{pLH} =1.027ns	t_{pHL} =0.592 ns
B_out circuit	Worst case	t_{pLH} =0.9002 ns	t_{pHL} =0.657 ns
	Best case	t_{pLH} =0.631 ns	t_{pHL} =0.608 ns

5. Full subtractor using dynamic logic

The circuit sized according to 2:1 inverter is shown below. Since no cascading of stages is seen, we don't need to use NORA or domino logic.

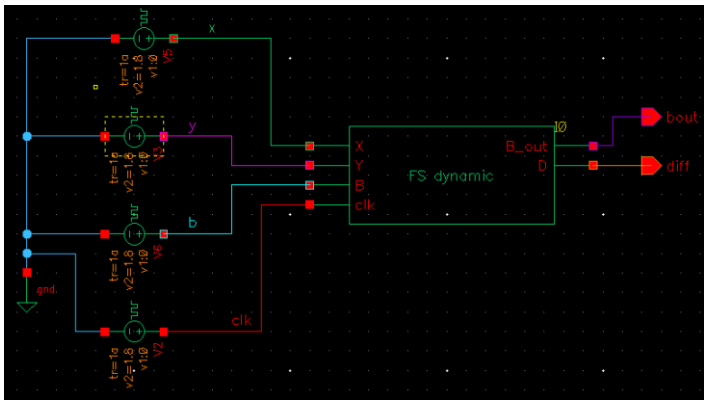


The schematic is shown below.

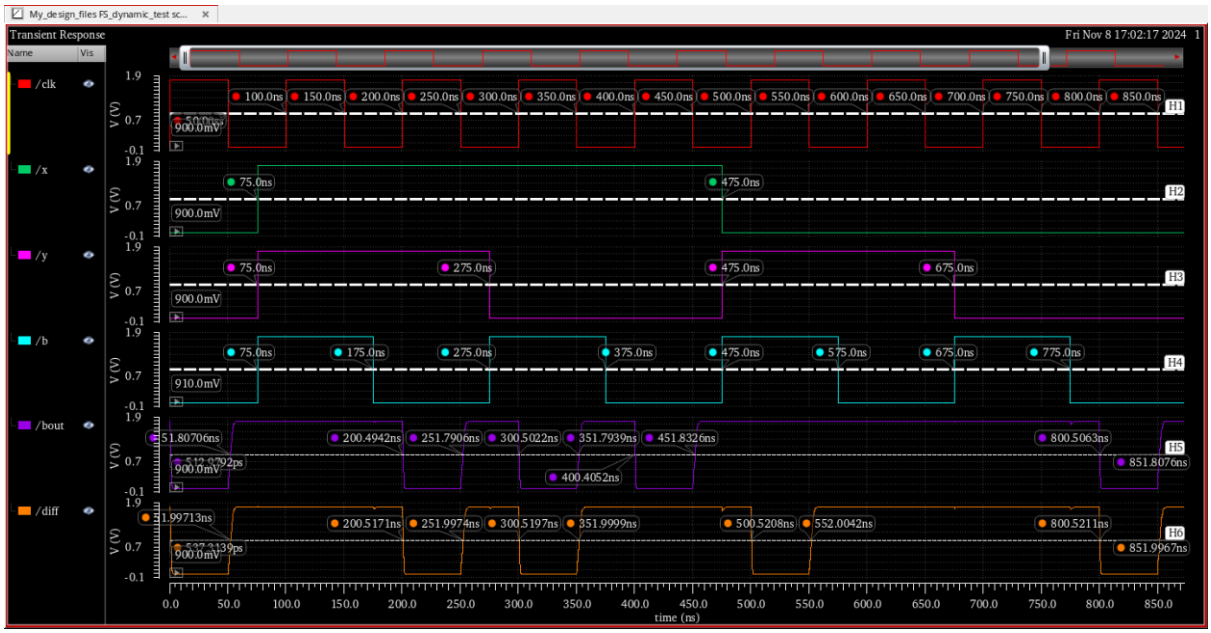


The borrow out circuit is on the left while the difference circuit is on the right. The outputs are reflected during the evaluate phase (positive level of the clock).

A symbol was created for the design and its test circuit is shown below.



The simulation waveforms are shown below for 8 clock cycles verifying the 8 output cases for a full subtractor.



From the above figure, best- and worst-case propagation delays are given in the table below. The circuits are n-dynamic circuits. During the evaluation phase, the output can either remain at V_{DD} (maintained from pre-charge) or fall to 0. So, its rise time is not defined (=0).

Difference Circuit	Worst case	t_{pHL} =0.5211 ns
	Best case	t_{pHL} =0.5171 ns
B_out circuit	Worst case	t_{pHL} =0.5063 ns
	Best case	t_{pHL} =0.4052 ns