VLSI Architecture Lab - 4
CORDIC algorithm implementation

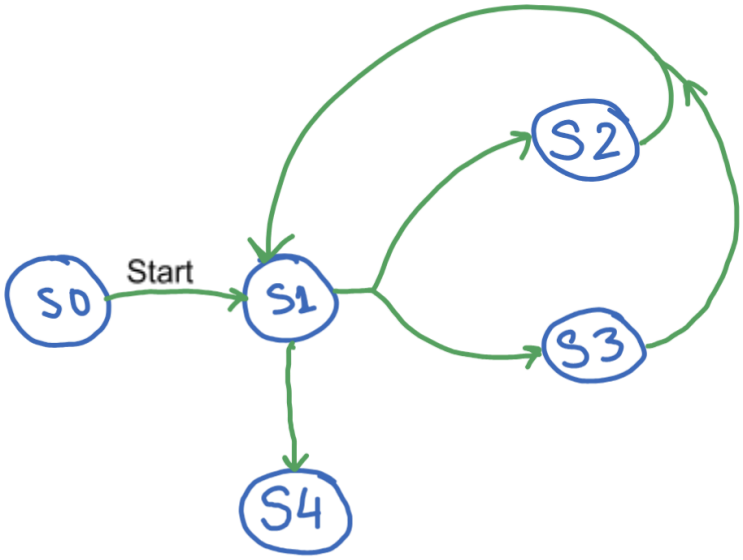
Inputs:

1. Angle argument in 2.14 fixed point format (in radian)
2. Start signal
3. Clock
4. Synchronous active high Reset signal

Outputs:

1. Done signal to indicate completion
2. Sine value in 2.14 fixed point format
3. Cosine value in 2.14 fixed point format

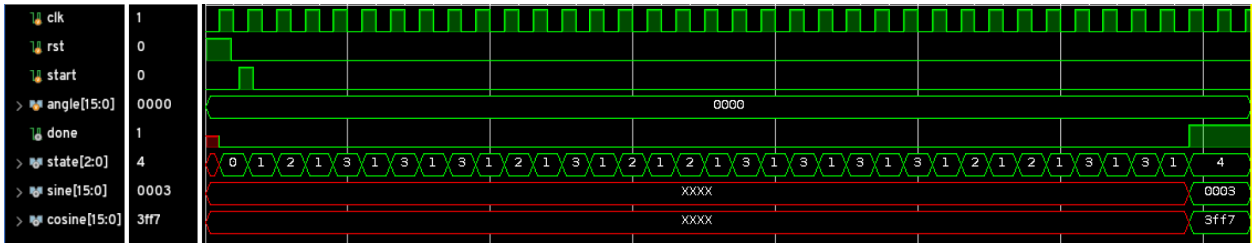
1. State diagram (Moore FSM)



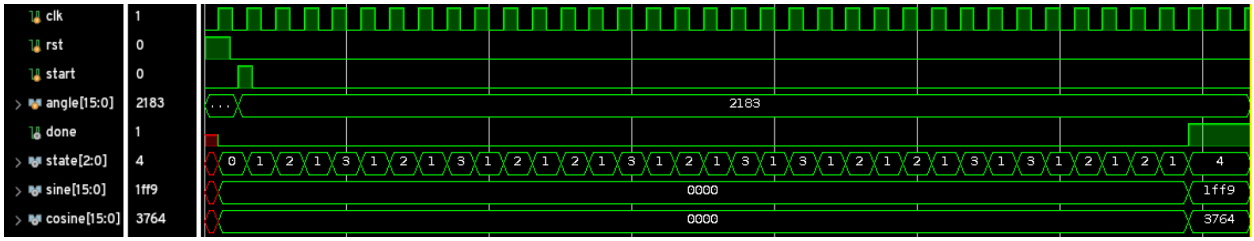
S0: Initial/idle state - Resets all registers to zero. It is the default state.
S1: Check state - Check if the number of state iterations (16 times) are done.
S2: Greater than argument state - Increments alpha and updates x & y accordingly.
S3: Less than argument state - Decrements alpha and updates x & y accordingly.
S4: Done state - Indicates the completion of the process by making done = 1 & showing final sine and cosine values.

2. Simulation results

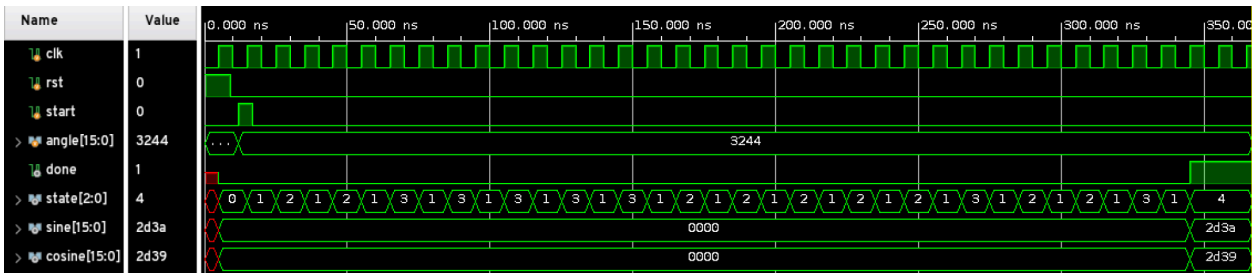
Timing diagram for argument = 0 deg = 0 rad



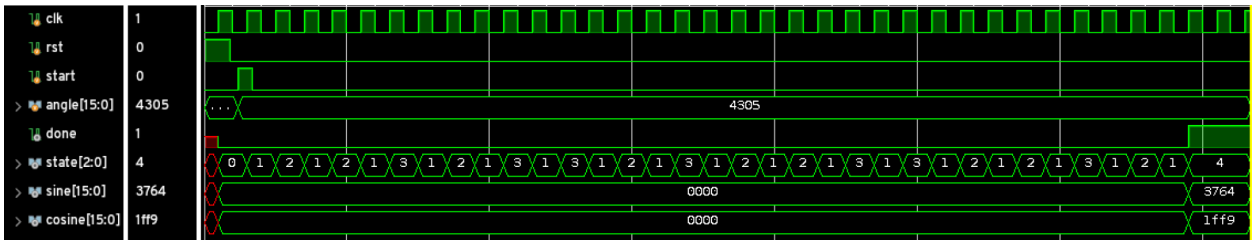
Timing diagram for argument = 30 deg = 0.5235 rad



Timing diagram for argument = 45 deg = 0.7859 rad



Timing diagram for argument = 60 deg = 1.047197 rad



The input argument and the final values in sine and cosine are in Hexadecimal format.

3. **Tabulated results for sine and cosine functions**

Argument (degree)	Actual sine value	Obtained sine value
0	0	0.000183105
30	0.5	0.499572753
45	0.707106	0.70666503
60	0.866025	0.86547851

Argument (degree)	Actual cosine value	Obtained cosine value
0	1	0.999450683
30	0.866025	0.86547851
45	0.707106	0.706604003
60	0.5	0.499572753