Simulation of Half Adder Using GDI Logic in eSim

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***Abstract*— This paper discusses the design and implementation of a half adder using Gate Diffusion Input (GDI) logic, focusing on its advantages in terms of area and power efficiency compared to conventional methods. The half adder is a fundamental building block in digital circuits, and its efficient design is crucial for the performance of larger integrated systems. The GDI technique is explored as a means to achieve lower power consumption and a reduced transistor count, addressing the challenges posed by traditional CMOS, pass transistor, and transmission gate logics.**

***Keywords*—** Half adder; GDI logic; low power; area efficiency; digital circuits.

I. INTRODUCTION

The half adder is a basic digital circuit that performs the addition of two binary digits. It generates two outputs: the sum and the carry. Efficient design techniques for the half adder are essential for improving the overall performance of digital systems, especially as the demand for low power and high performance circuits increases day by day. Various implementations of half adders have been explored, including CMOS, pass transistor logic, and transmission gate logic. This paper focuses on the GDI technique, which promises significant advantages in power and area efficiency over these conventional methods.

II. PRINCIPLE OF GENERATION

The GDI technique utilizes a combination of NMOS and PMOS transistors to achieve the required logic functions with fewer components. The fundamental logic for the half adder is represented as follows:

- Sum (S) = A ⊕ B (XOR of inputs A and B)
- Carry (C) = A · B (AND of inputs A and B)

In this implementation, the GDI method reduces the number of transistors required, which directly contributes to lower power consumption and smaller area on the chip.

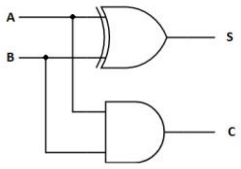

Fig. 1 Circuit Diagram of Half Adder

Fig. 2 Waveform of Half Adder

III. IMPLEMENTATION

A GDI circuit made in eSim has been presented:

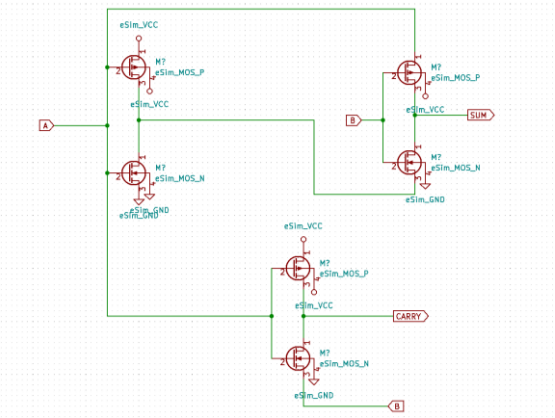

Fig. 3 GDI implementation of Half Adder in eSim

While exploring various logic styles, I also examined pass transistor logic and transmission gate logic. Pass transistor logic uses NMOS transistors to pass signals based on control inputs, resulting in fewer transistors but at the cost of weaker output levels. Transmission gate logic combines NMOS and PMOS transistors to create a bidirectional switch, enhancing the drive strength but requiring more transistors compared to GDI. However, GDI effectively combines the benefits of both methods while minimizing their drawbacks, making it a superior choice for this implementation. The half adder circuit is implemented using GDI logic to achieve efficient performance.

IV. ISSUES & IMPROVEMENTS

While the GDI technique provides benefits in area and power efficiency, it faces challenges compared to other methods like CMOS, pass transistor logic, and transmission gate logic. In GDI circuit, switching speeds might be slower due to output capacitance, whereas transmission gates offer faster performance but at the cost of increased area and power consumption. The complexity of GDI design and simulation further necessitates improved methodologies for effective implementation.

V. CONCLUSION & FUTURE SCOPE

This paper presented the design and implementation of a half adder using Gate Diffusion Input (GDI) logic, highlighting its advantages in area and power efficiency compared to conventional methods like CMOS, pass transistor, and transmission gate logics. The GDI technique successfully reduces transistor count while maintaining effective performance, addressing the growing demand for low-power digital circuits.

VI. REFERENCES

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