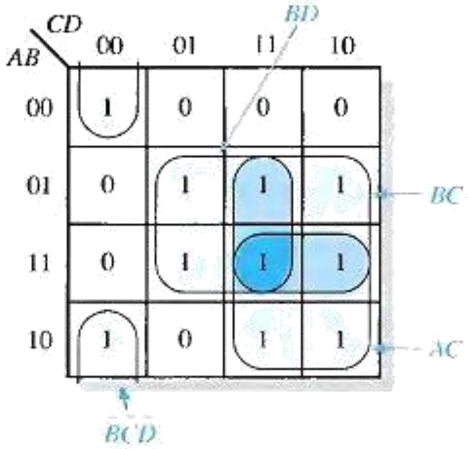


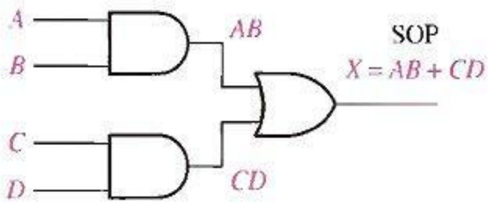

(c) Minimum SOP: $AC + BC + BD + \overline{B}\overline{C}\overline{D}$

## Implimentation of logical circuit using NAND and NOR gates:

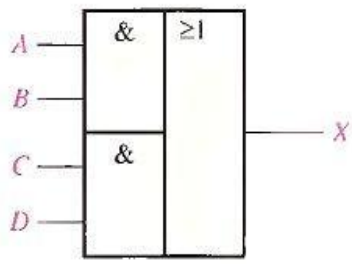
### 1- AND-OR Logic

Fig.(6-1)(a) shows an AND-OR circuit consisting of two 2-input AND gates and one 2-input OR gate; Fig.(6-1)(b) is the ANSI standard rectangular outline symbol. The Boolean expressions for the AND gate outputs and the resulting SOP expression for the output X are shown in the diagram. In general, all AND-OR circuit can have any number of AND gates each with any number of inputs.

The truth table for a 4-input AND-OR logic circuit is shown in Table 6-1. The intermediate AND gate outputs ( AB and CD columns) are also shown in the table.




**(a) Logic diagram**




**(b) ANSI standard rectangular outline symbol.**

**Fig.(6-1)**

**For a 4-input AND-OR logic circuit, the output X is HIGH (1) if both input A and input B are HIGH (1) or both input C and input D are HIGH (1).**

## 2-AND-OR-Invert Logic

When the output of an AND-OR circuit is complemented (inverted), it results in an AND-OR-Invert circuit. Recall that AND-OR logic directly implements SOP expressions. POS expressions can be implemented with AND-OR-Invert logic. This is illustrated as follows, starting with a POS expression and developing the corresponding AND-OR-Invert expression.

**Table 6-1**

| INPUTS | | | | | | OUTPUT |
|---|---|---|---|---|---|---|
| A | B | C | D | AB | CD | X |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

$$X = (\overline{A}+\overline{B})(\overline{C}+\overline{D}) = (\overline{AB})(\overline{CD}) = \overline{\overline{(\overline{AB})(\overline{CD})}} = \overline{\overline{\overline{AB}} + \overline{\overline{CD}}} = \overline{AB+CD}$$

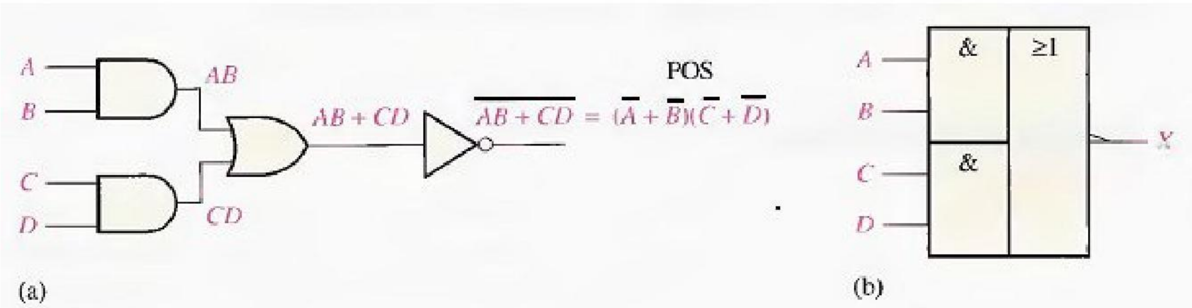



**Fig.(6-2)**

**For a 4-input AND-OR-Invert logic circuit, the output X is LOW (0) if both input A and input B are HIGH (1) or both input C and input D are HIGH (1).**

## 3-Exclusive-OR logic

The exclusive-OR gate was introduced before. Although, because of its importance, this circuit is considered a type of logic gate with its own unique symbol it is actually a combination of two AND gates, one OR gate, and two inverters, as shown in Fig.(6-3)(a). The two standard logic symbols are shown in parts (b) and (c).

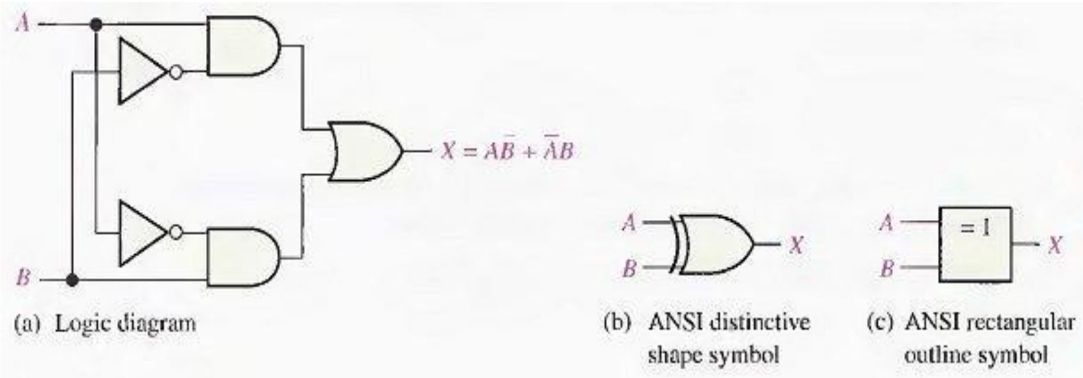



**Fig.(6-3)**

The output expression for the circuit in Fig.(6-3) is

$$X = A\overline{B} + \overline{A}B$$

Can be written as $X = A \oplus B$

**Table 6-2 Truth table for an exclusive-OR.**

| A | B | X |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

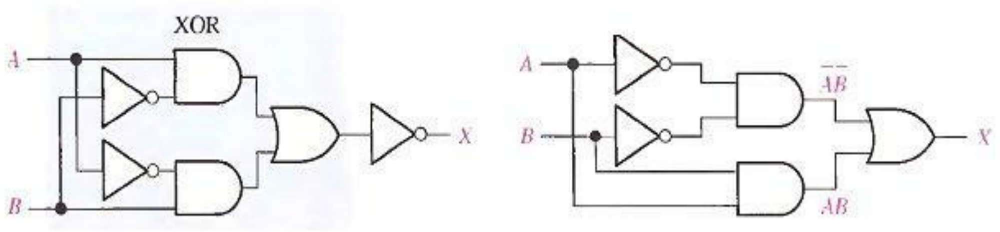
## 4- Exclusive-NOR Logic

As you know, the complement of the exclusive-OR function is the exclusive-NOR, whichis derived as follows:

X = AB + AB = (AB) (AB) = (A + B)(A + B) = AB + AB

Notice that the output X is HIGH only when the two inputs, A and B, are at the same level.

The exclusive-NOR can be implemented by simply inverting the output of an exclusive- OR, as shown in Fig(6-4)(a), or by directly implementing the expression AB + AB, as shown in part (b).




(a) $X = \overline{A\bar{B} + \bar{A}B}$ (b) $X = \bar{A}\bar{B} + AB$

**Fig.(6-4)**

**Example**

Develop a logic circuit with four input variables that will only produce a 1 output when exactly three input variables are 1s. Fig.(6-5) shows the circuit.

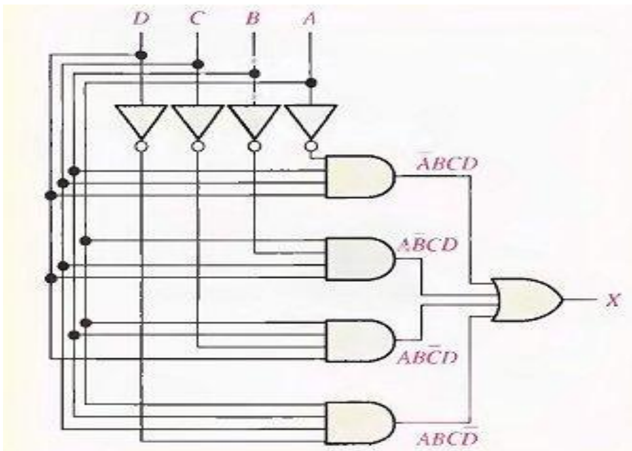



Fig.(6-5)

## Example

Reduce the combinational logic circuit in Fig.(6-6) to a minimum form.

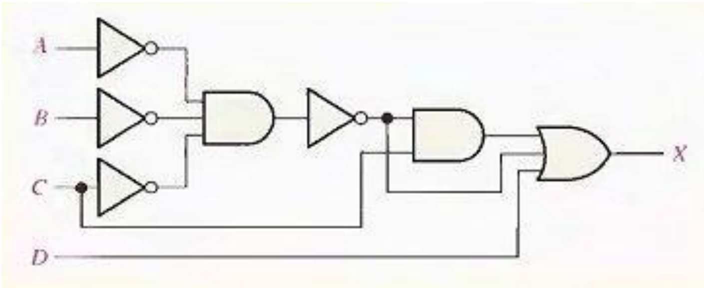



**Fig.(6-6)**

## Solution

The expression for the output of the circuit is

*X* = (A B C) C + ABC + D

Applying DeMorgan's theorem and Boolean algebra,

$$
\begin{aligned}
X &= (\bar{\bar{A}} + \bar{\bar{B}} + \bar{\bar{C}})C + \bar{\bar{A}} + \bar{\bar{B}} + \bar{\bar{C}} + D \\
&= AC + BC + CC + A + B + C + D \\
&= AC + BC + C + A + B + \cancel{C} + D \\
&= C(A + B + 1) + A + B + D \\
X &= A + B + C + D
\end{aligned}
$$

The simplified circuit is a 4-input OR gate as shown in Fig.(6-7).

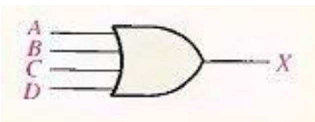



**Fig.(6-7)**