Exploration of Negative Capacitance in Gate-All-Around Si Nanosheet Transistors

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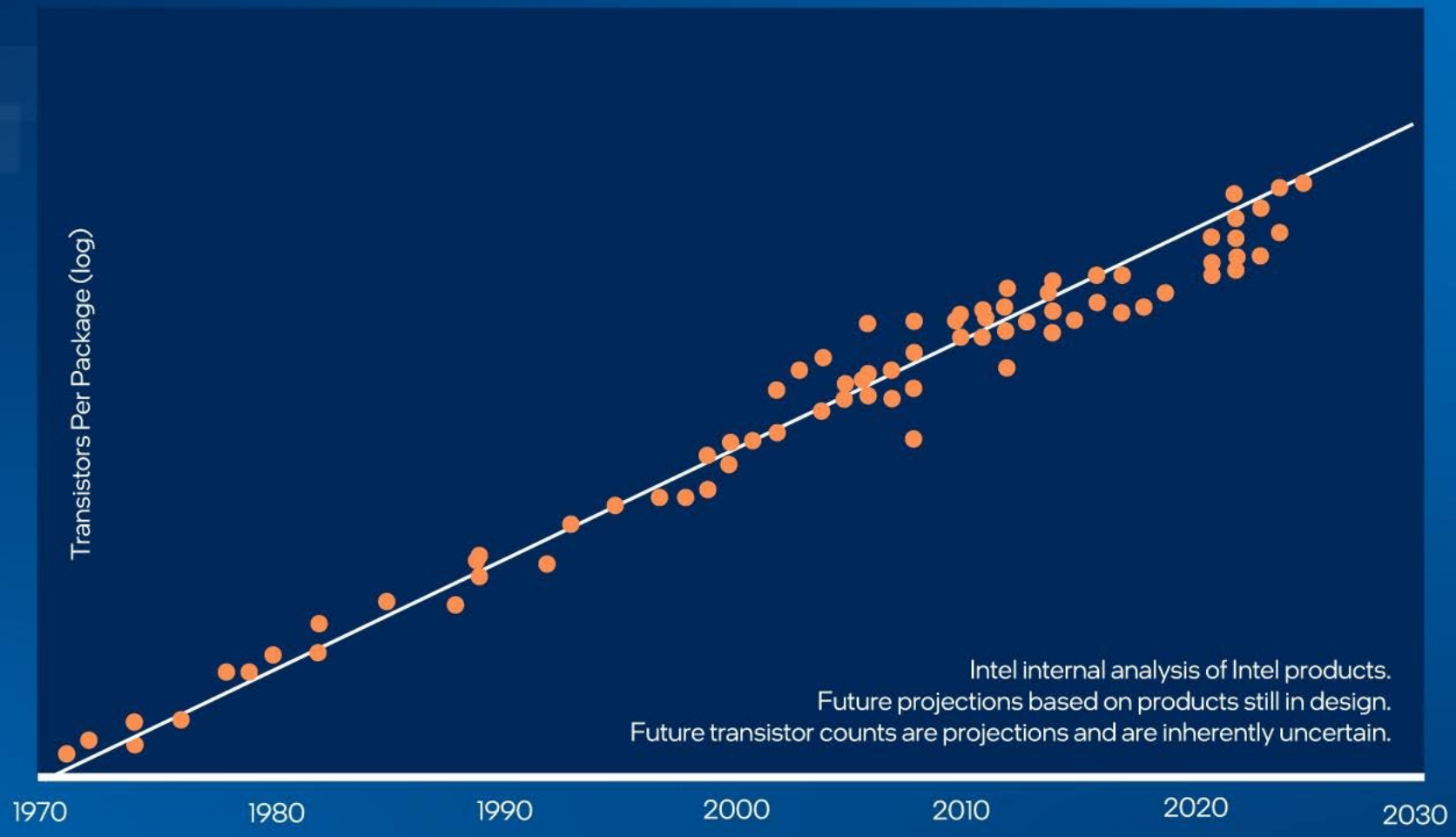
Introduction

- **a. Topic Overview:-** The paper explores **Negative Capacitance in Gate-All-Around (GAA) Nanosheet Transistors**, a key innovation in semiconductor scaling. It addresses the growing need for energy-efficient and high-performance devices in IoT and advanced computing.

- **b. Problem Statement:-** Traditional transistors like FinFETs face scalability, short-channel effects, and high power issues. This paper proposes integrating negative capacitance in GAA nanosheet transistors to overcome these challenges.

- **c. Objective:-** To analyze and optimize **NC-GAA nanosheet transistors** for sub-60 mV/decade switching and benchmark their performance against existing architectures.

- **d. Motivation:-** The demand for ultra-low power, compact, and scalable devices drives the need for NC-based transistors to meet industry and sustainability goals.



Aspiring to

1 Trillion

transistors in 2030

- ✓ RibbonFET
- ✓ PowerVia
- ✓ High NA
- ✓ 2.5D/3D packaging

intel

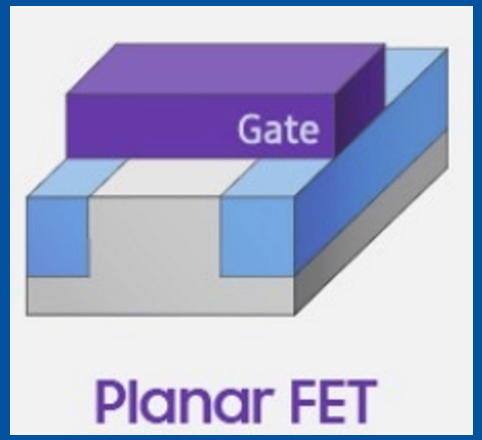
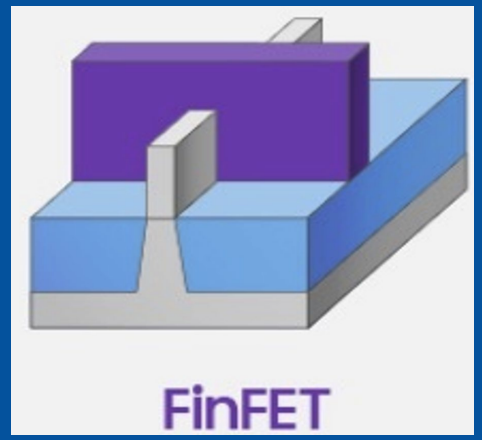
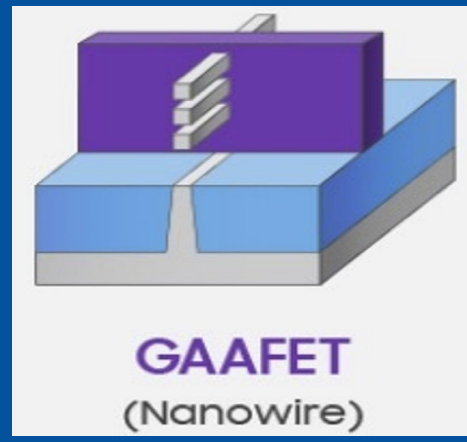
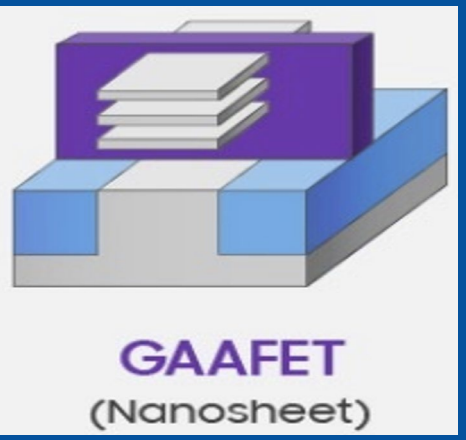
*Source : intel press kit

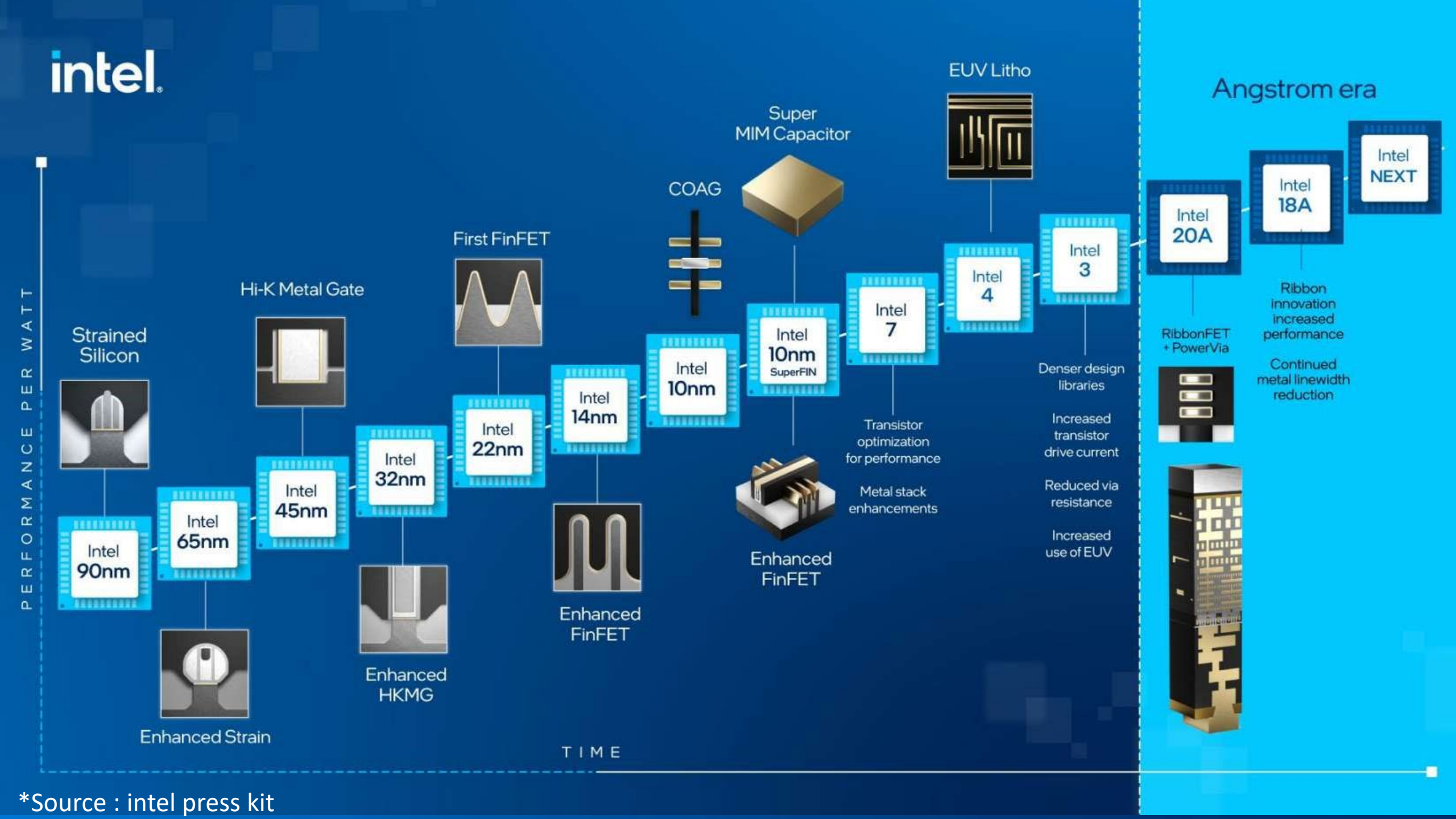
Problems in Scaling Down Transistor Size

- **Short-Channel Effects**: Increased leakage and performance degradation.
- **Quantum Effects**: Tunneling and reliability issues at nanoscale.
- **Heat Management**: Higher density causes thermal challenges.
- **Fabrication Complexity**: Advanced and expensive manufacturing processes.
- **Material Limits**: Need for alternatives to silicon.
- **Variability**: Greater process variations impact performance.
- **Interconnect Delays**: Resistance and capacitance dominate signal propagation.
- **Gate Control**: Poor control requires innovations like FinFETs and GAA transistors

Impact on Operating Voltage

- **Lower Supply Voltage**: To reduce power and control leakage.
- **Reduced Threshold Voltage**: Increases leakage and noise susceptibility.
- **Power Dissipation**: Dynamic power decreases, but leakage power rises.
- **Reliability Issues**: Lower noise margins lead to higher error risk.
- **Performance Trade-offs**: Lower voltages reduce speed.
- **Signal Integrity**: Harder to differentiate logic levels.

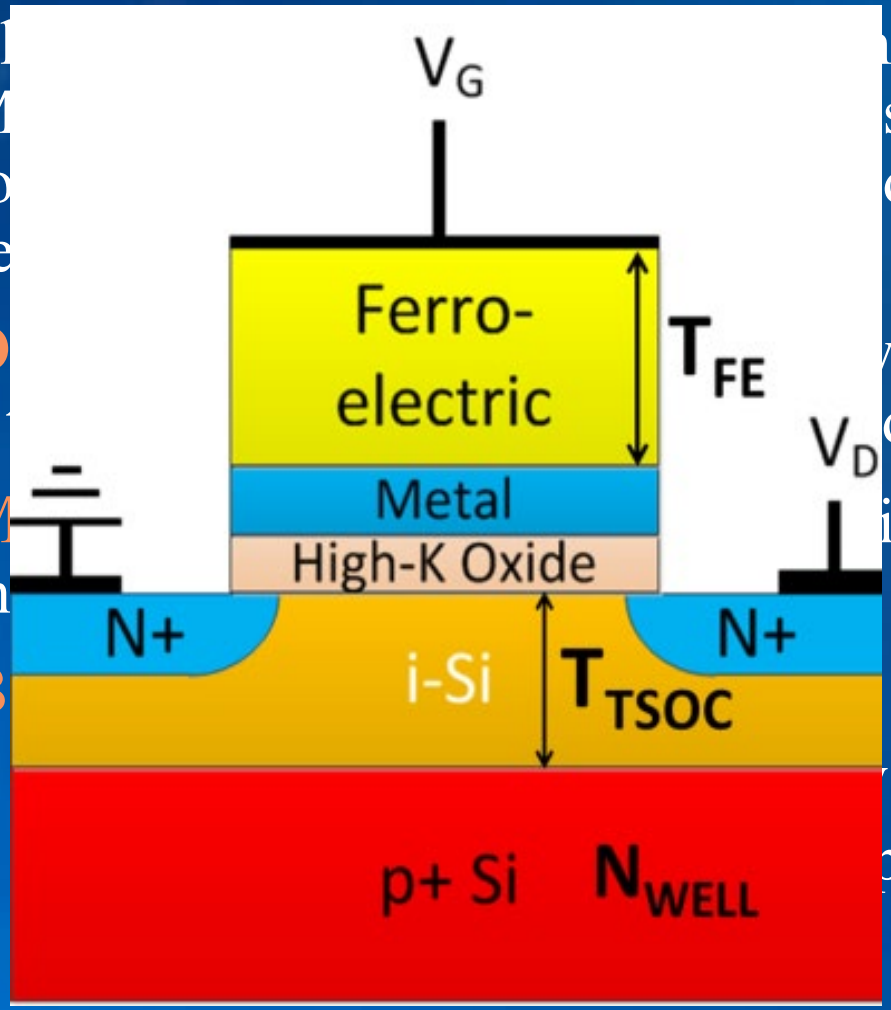
Feature	MOSFETs	FinFETs	Nanowire FETs (NWFETs)	Nanosheet FETs (NSFETs)
Advantages				
	 Planar FET	 FinFET	 GAAFET (Nanowire)	 GAAFET (Nanosheet)
Disadvantages				

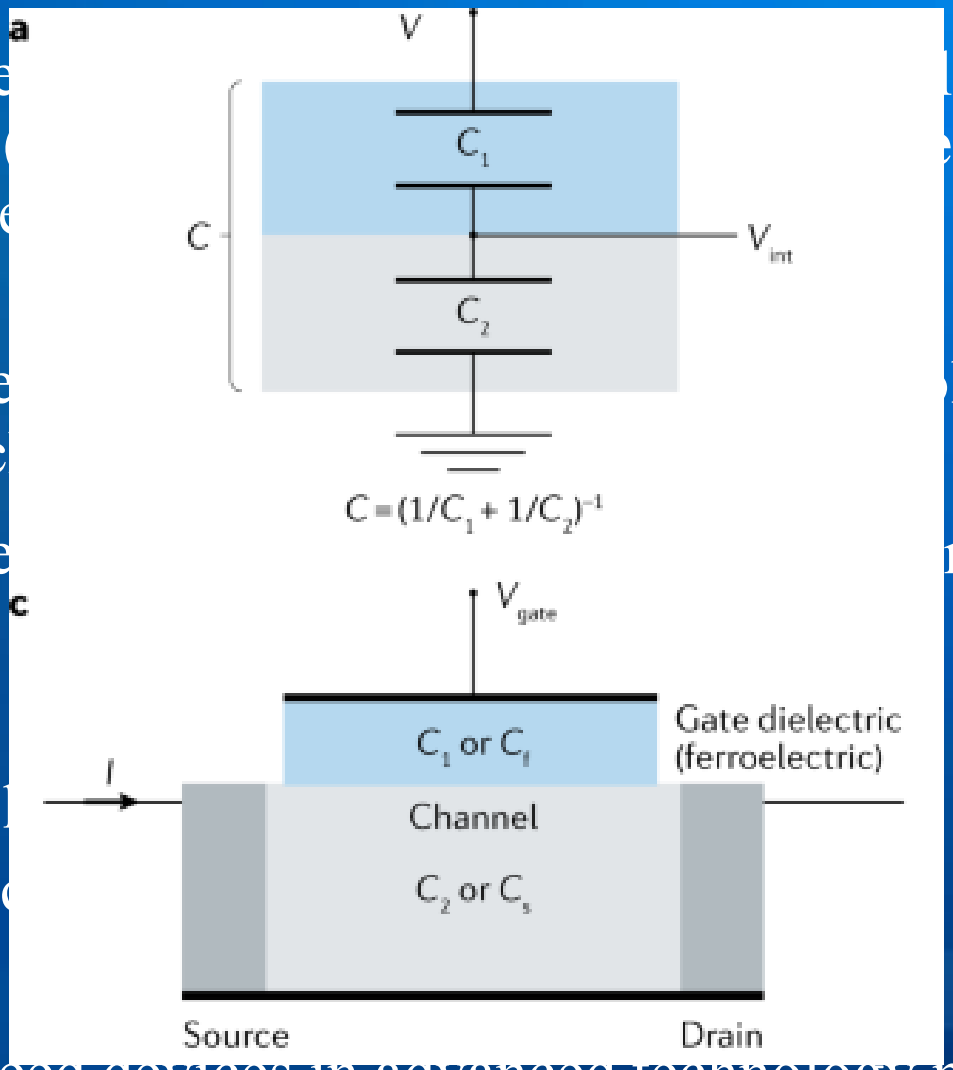


*Source : intel press kit

Negative capacitance

- **Boltzmann Limit**
- Th… …damental the… …shold swing … at ro… …due to the the… se…
- **D**… …where a ferroe… …ltage in a … …decade switc…
- **M**… …ing a ferroele… …reating in…
- **B**… … enabling vo… …peed and effi…
- **Applications**: Ideal for low-power and high-speed devices in advanced technology nodes (sub-5nm).





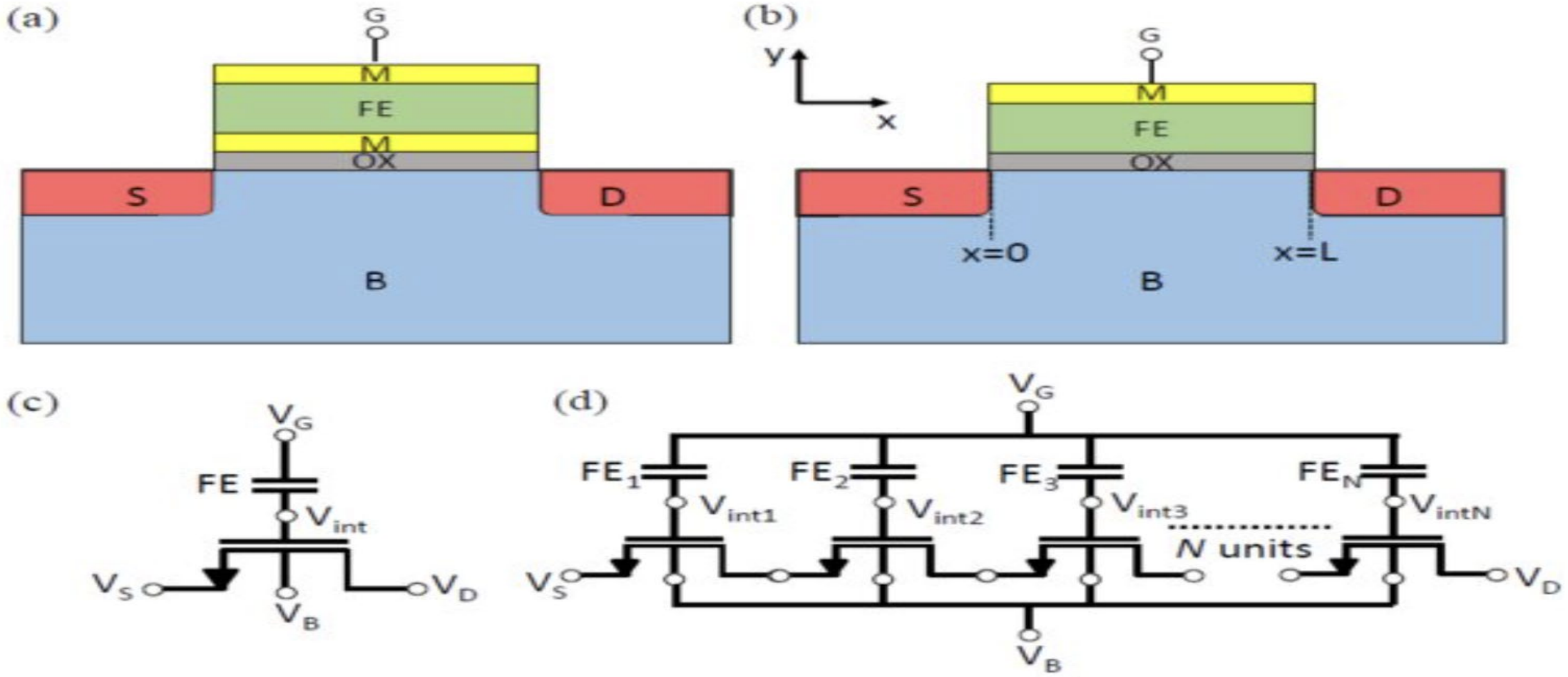


Fig. 1. Different NCFET structures: (a) MFMIS and (b) MFIS. Circuit equivalents of (c) MFMIS and (d) MFIS. Each unit in the MFIS equivalent network represents an MFMIS structure. V_{int} denotes internal voltage at the ferroelectric-oxide interface. For MFIS, V_{int} varies along the longitudinal direction when a non-zero drain bias is applied and hence, it has been modeled by the arrangement shown.

Literature review

Paper	Citation	Issue Handled	Base Idea	Strength	Limitations
Paper 1	Singh, J., et al., "14-nm FinFET technology for analog and RF applications," IEEE Transactions on Electron Devices, vol. 65, no. 1, pp. 31-37, Jan. 2018. doi:10.1109/TED.2017.2776838	Demonstrated the advantages of FinFET technology for analog and RF applications, highlighting its improved short-channel effects and scaling capabilities.	FinFETs provide excellent short-channel control and scalability for advanced nodes.	Superior performance in analog and RF domains with excellent scaling properties.	Challenges in further scaling beyond sub-10 nm nodes.
Paper 2	Razavieh, A., Zeitzoff, P., and Nowak, E. J., "Challenges and limitations of CMOS scaling for FinFET and beyond architectures ," IEEE Transactions on Nanotechnology, vol. 18, no. 4, pp. 999-1004, Sep. 2019. doi:10.1109/TNANO.2019.2942456	Highlighted the challenges of CMOS scaling for FinFETs, including process control and cost at advanced nodes.	CMOS scaling is becoming increasingly challenging for FinFET architectures.	Provides a comprehensive overview of the limitations of FinFET scaling.	Does not propose concrete solutions for overcoming scaling challenges.
Paper 3	Loubet, N., et al., "Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET," in Proceedings of the IEEE Symposium on VLSI Technology, Jun. 2017, pp. 230-231. doi:10.23919/VLSIT.2017.7998183	Proposed stacked nanosheet GAA transistors as a scalable alternative to FinFETs, offering improved electrostatics and short-channel control.	GAA nanosheet transistors provide a path forward for sub-10 nm nodes.	High scalability and excellent electrostatics.	Requires significant advancements in fabrication techniques.
Paper 4	Nagy, D., et al., "FinFET versus gate-all-around nanowire FET: Performance, scaling, and variability," IEEE Journal of the Electron Devices Society, vol. 6, no. 1, pp. 332-340, Feb. 2018. doi:10.1109/JEDS.2018.2804383	Compared FinFETs and GAA nanowire FETs, highlighting the latter's superior electrostatics and variability.	GAA nanowire FETs outperform FinFETs in electrostatics and scaling.	Demonstrates clear advantages in variability and gate control.	Limited drive current compared to nanosheet FETs.

Paper	Citation	Issue Handled	Base Idea	Strength	Limitation
Paper 5	Barraud, S., et al., "Performance and design considerations for gate-all-around stacked-NanoWires FETs," in IEDM Technical Digest, Dec. 2017, p. 29. doi:10.1109/IEDM.2017.8268473	Discussed performance and design considerations for GAA stacked nanowires.	GAA stacked nanowires improve performance through enhanced electrostatics.	Comprehensive analysis of design and performance factors.	challenges related to manufacturabilit y.
Paper 6	Jang, D., et al., "Device exploration of nanosheet transistors for Sub-7-nm technology node," IEEE Transactions on Electron Devices, vol. 64, no. 6, pp. 2707-2713, Jun. 2017. doi:10.1109/TED.2017.2695455	Demonstrated the high drive current capability of nanosheet transistors due to their larger effective channel width compared to NWFETs.	Nanosheet FETs are superior in terms of drive current and scalability.	Excellent current drivability and scalability.	Increased parasitic capacitance compared to nanowire FETs.
Paper 7	Salahuddin, S., and Datta, S., "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," Nano Letters, vol. 8, no. 2, pp. 405-410, Feb. 2008. doi:10.1021/nl071804g	Introduced the concept of negative capacitance (NC) in FETs, enabling sub-60 mV/decade switching.	NC materials can amplify voltage and improve switching efficiency.	Provides a theoretical basis for NC-FETs.	Requires integration of ferroelectric materials, which poses fabrication challenges.
Paper 8	Gaidhane, A. D., et al., "Compact modeling of drain current, charges, and capacitances in long-channel gate-all-around negative capacitance MFIS transistor," IEEE Transactions on Electron Devices, vol. 65, no. 5, pp. 2024-2032, May 2018. doi:10.1109/TED.2018.2813059	Developed compact models for long-channel GAA-NCFETs, emphasizing their benefits for advanced nodes.	Compact modeling enables better understanding and optimization of GAA-NCFETs.	Supports simulation and design of advanced NC devices.	Focuses on long-channel devices, with limited applicability to short-channel effects.

Paper	Citation	Issue Handled	Base Idea	Strength	Limitation
Paper 9	Lee, M. H., et al., "Extremely steep switch of negative-capacitance nanosheet GAA-FETs and FinFETs," in IEDM Technical Digest, Dec. 2018, p. 31. doi:10.1109/IEDM.2018.8614510	Experimentally demonstrated steep switching in NC-GAA nanosheet FETs and compared their performance to FinFETs.	NC integration significantly improves switching characteristics in nanosheet FETs.	Provides experimental validation for NC-FET advantages.	Limited exploration of device stability and reliability.
Paper 10	Pahwa, G., et al., "Numerical investigation of short-channel effects in negative capacitance MFIS and MFMIS transistors: Subthreshold behavior," IEEE Transactions on Electron Devices, vol. 65, no. 11, pp. 5130-5136, Nov. 2018. doi:10.1109/TED.2018.2870519	Investigated short-channel effects in MFMIS and MFIS NCFETs, highlighting their subthreshold behavior.	Short-channel effects can be mitigated in NC-FETs through proper design.	Provides detailed insights into subthreshold behavior.	Does not address experimental challenges in achieving ideal NC effects.
Paper 11	Zhou, J., et al., "Negative differential resistance in negative capacitance FETs," IEEE Electron Device Letters, vol. 39, no. 4, pp. 622-625, Apr. 2018. doi:10.1109/LED.2018.2810071	Explored negative differential resistance (NDR) and its implications in NCFETs.	NDR can be utilized for novel device functionalities.	Highlights unique properties of NCFETs for analog applications.	Limited experimental validation of proposed NDR effects.
Paper 12	Agarwal, H., et al., "Proposal for capacitance matching in negative capacitance field-effect transistors," IEEE Electron Device Letters, vol. 40, no. 3, pp. 463-466, Mar. 2019. doi:10.1109/LED.2019.2891540	Proposed capacitance matching strategies for enhancing NC effects in NCFETs.	Proper capacitance matching enhances the performance of NC devices.	Provides actionable strategies for optimizing NC-FETs.	Does not address scalability challenges in capacitance matching.

Proposed methodology : Device Structure

- The simulated devices are Negative Capacitance Field Effect Transistors (NCFETs) with an **MFMIS (metal–ferroelectric–metal–insulator–semiconductor)** gate stack configuration.
- Aluminum-doped hafnium oxide ($Al:HfO_2$) is used as the ferroelectric (FE) material.
- The metal work function (WF) is 4.65 eV.
- Silicon nitride spacers (10 nm thick) are used to mitigate short-channel effects (SCE), although they are not shown in the diagram.
- The channel is **p-type doped (10^{16} cm^{-3})**, and the source/drain regions are **n-doped (10^{20} cm^{-3})**.

Proposed methodology :Stability Considerations

- MFMIS NCFETs can face stability issues in steady state due to gate leakage through the FE layer.
- Stability can be improved by engineering the work functions of the metals used in the external electrode and intermediate layer.
- Gate leakage is deliberately ignored in this study to focus on performance trends, and MFMIS devices without gate leakage behave similarly to MFIS (metal–ferroelectric–insulator–semiconductor) devices.

Proposed methodology : Simulation Setup

- Simulations were performed using the **Silvaco Atlas** device simulator, which solves Poisson's and current continuity equations to calculate gate charge (QG) and drain current (ID) as functions of gate voltage (VG).
- The ferroelectric capacitor is modeled using the 1-D **Landau–Khalatnikov (L–K) equation**.
- Bulk material parameters for the FE material:
  - $\alpha = -3 \times 10^{-9}$ m/F, $\beta = 6 \times 10^{11}$ m^5/C^{2}F, and $\gamma = 0$.
- Quantum confinement effects are modeled using the **Bohm Quantum Potential (BQP)** model.
- The **Lombardi mobility model** is used to account for mobility degradation due to phonon and Coulomb scattering.

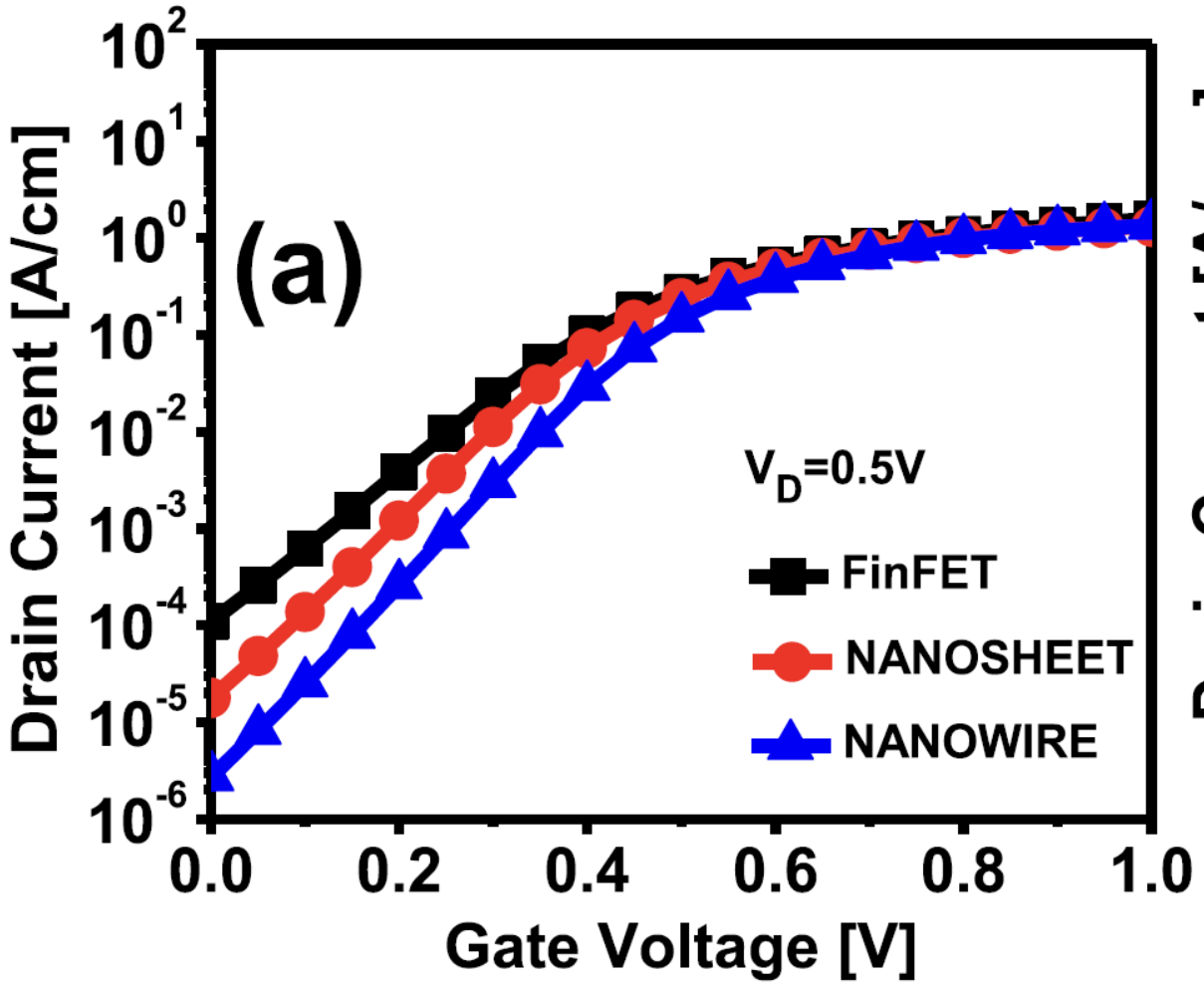
Performance analysis :

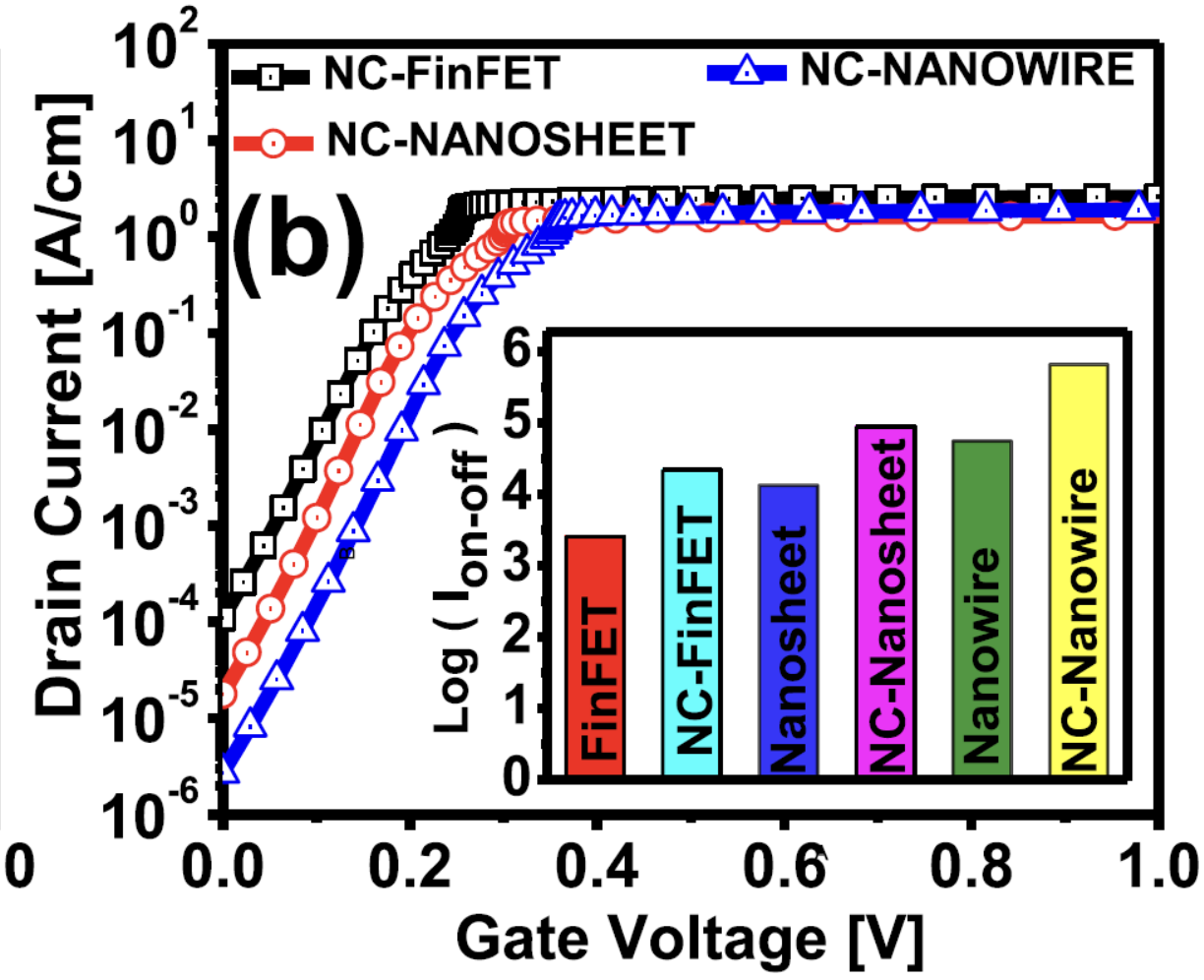
- Devices evaluated: MFMIS NC-NWFET, NC-NSFET, NC-FinFET, and their baseline counterparts.
- Comparable device dimensions and doping profiles were used.
- Simulations utilized parameters listed in Table I.

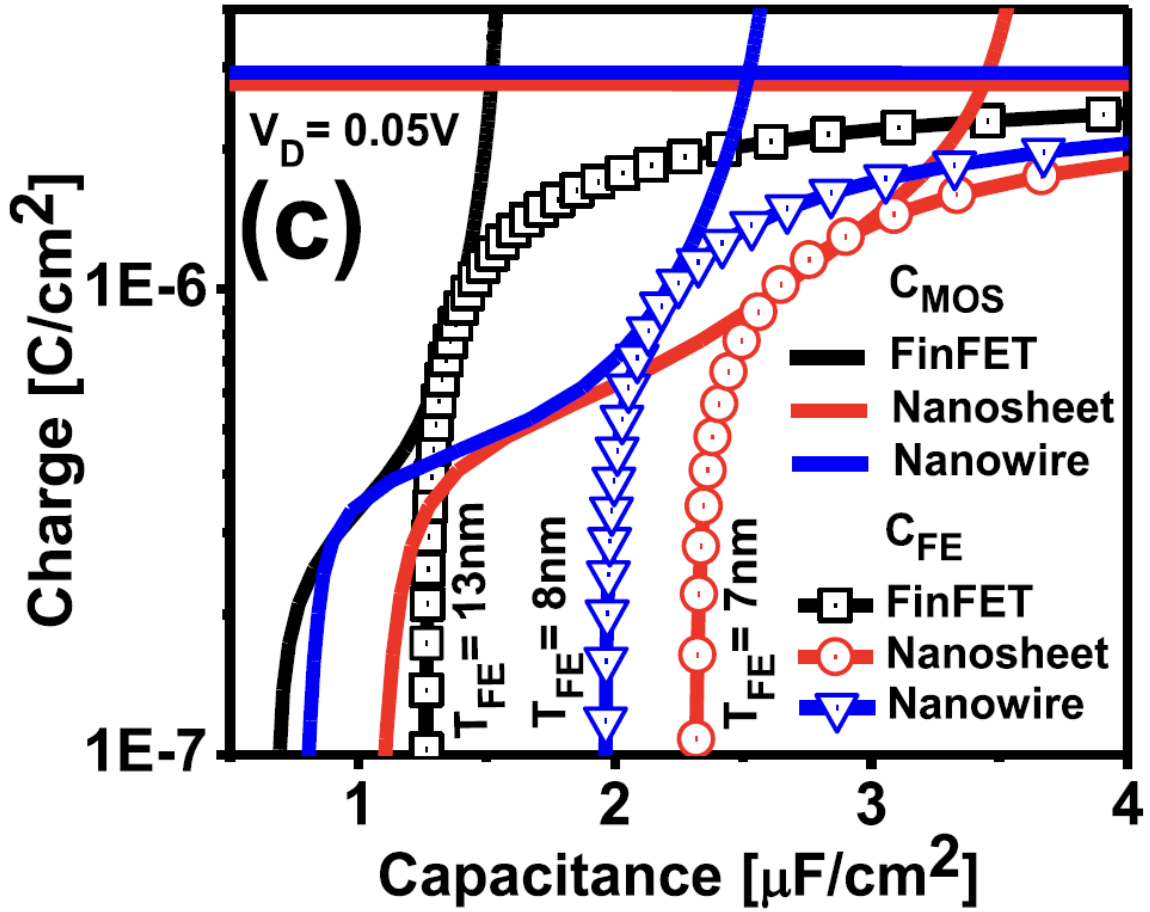
TABLE I
PARAMETERS USED IN DEVICE SIMULATIONS FOR SINGLE CHANNEL NCFETS [FIG. 1(a)]

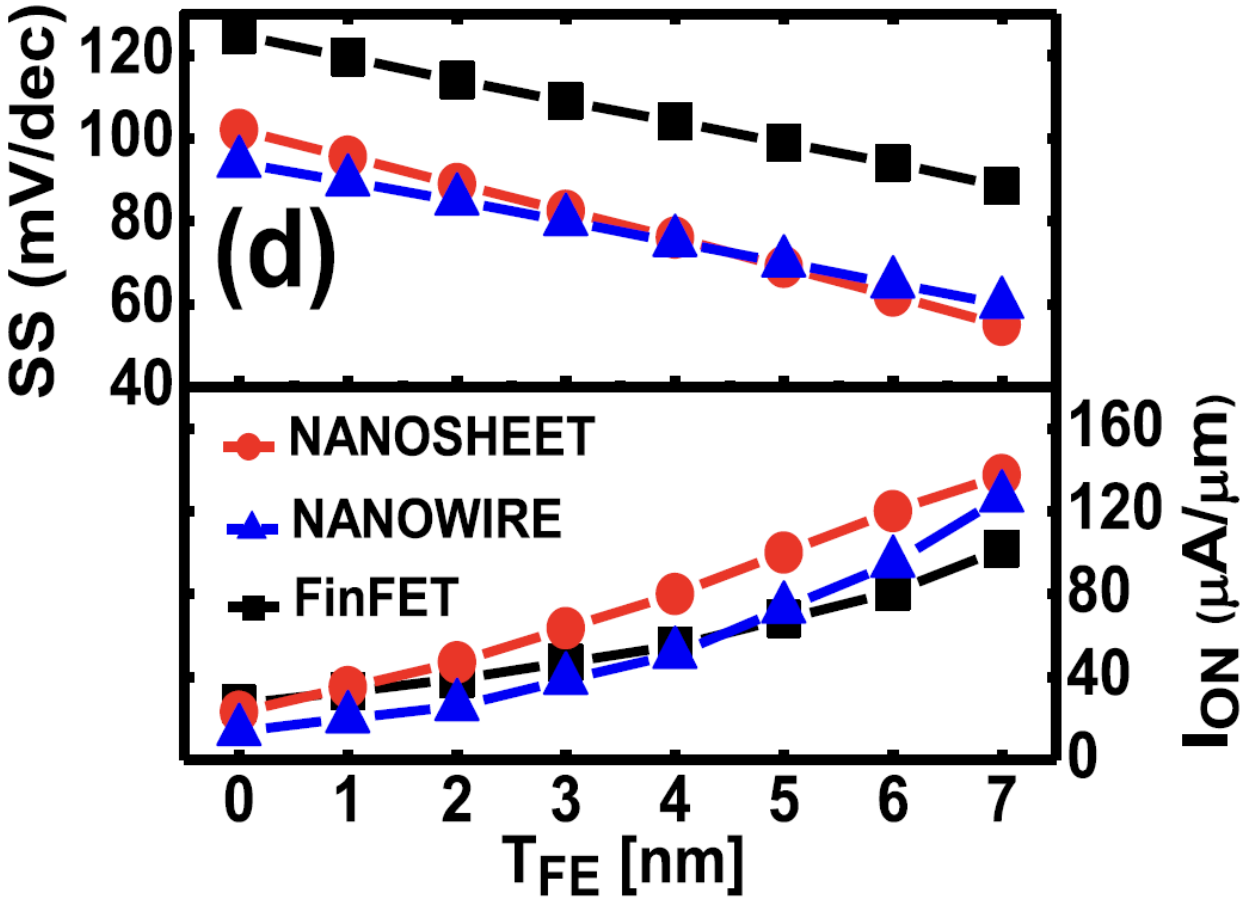
Symbol	Parameter	Value
L_G	Gate Length	25 nm
D_{NW}	Diameter of NW	6 nm
EOT	Effective Oxide Thickness	0.7 nm
T_{NS}	Thickness of NS	5 nm
W_{NS}	Width of NS	20 nm
H_{FIN}	Height of Fin	20 nm
W_{FIN}	Width of Fin	5 nm

Performance analysis : Transfer Characteristics






(c)
V_D= 0.05V
Charge [C/cm^2]
1E-6
1E-7
1
2
3
4
Capacitance [μF/cm^2]
T_{FE}= 13nm
T_{FE}= 8nm
T_{FE}= 7nm
C_{MOS}
FinFET
Nanosheet
Nanowire
C_{FE}
FinFET
Nanosheet
Nanowire


(d)
SS (mV/dec)
120
100
80
60
40
NANOSHEET
NANOWIRE
FinFET
160
120
80
40
0
I_{ON} (μA/μm)
0
1
2
3
4
5
6
7
T_{FE} [nm]

Performance analysis

- **Hysteresis**:
  - Thinner FE layers reduce hysteresis, crucial for scaling NCFETs in advanced technology nodes.
  - NC-NSFET operates hysteresis-free at TFE = 7 nm.
- **Device Comparison at TFE = 7 nm**:
  - NC-NSFET:
    - 38% lower SS than NC-FinFET.
    - 9% lower SS than NC-NWFET.
    - 35% higher Ion than NC-FinFET.
- **SS and Ion Trends**:
  - Higher TFE improves NC performance (lower SS and higher Ion).
  - Maximum TFE limited to 7 nm for all devices to avoid hysteresis.

Single Stack vs. Double Stack NC-NSFET

- **Single Stack NC-NSFET:**
- **Structure:**
  - Contains three stacked nanosheet (NS) channels.
- **Effective Gate Width (W_{exex}):**
  - $W_{exex} = 3 \times (2 \times W_{ns} + 2 \times T_{ns})$.
- **Key Characteristics:**
  - At L_x = 80 nm, each NS in a single stack is 2.5× wider than in a double stack.
  - Achieves up to **25% more I_{on}** than the double stack.
  - Provides **lower Subthreshold Swing (SS)**: 13% lower at VDD = 0.7 V.
  - Offers a similar I_{on}/I_{oex} ratio compared to the double stack.

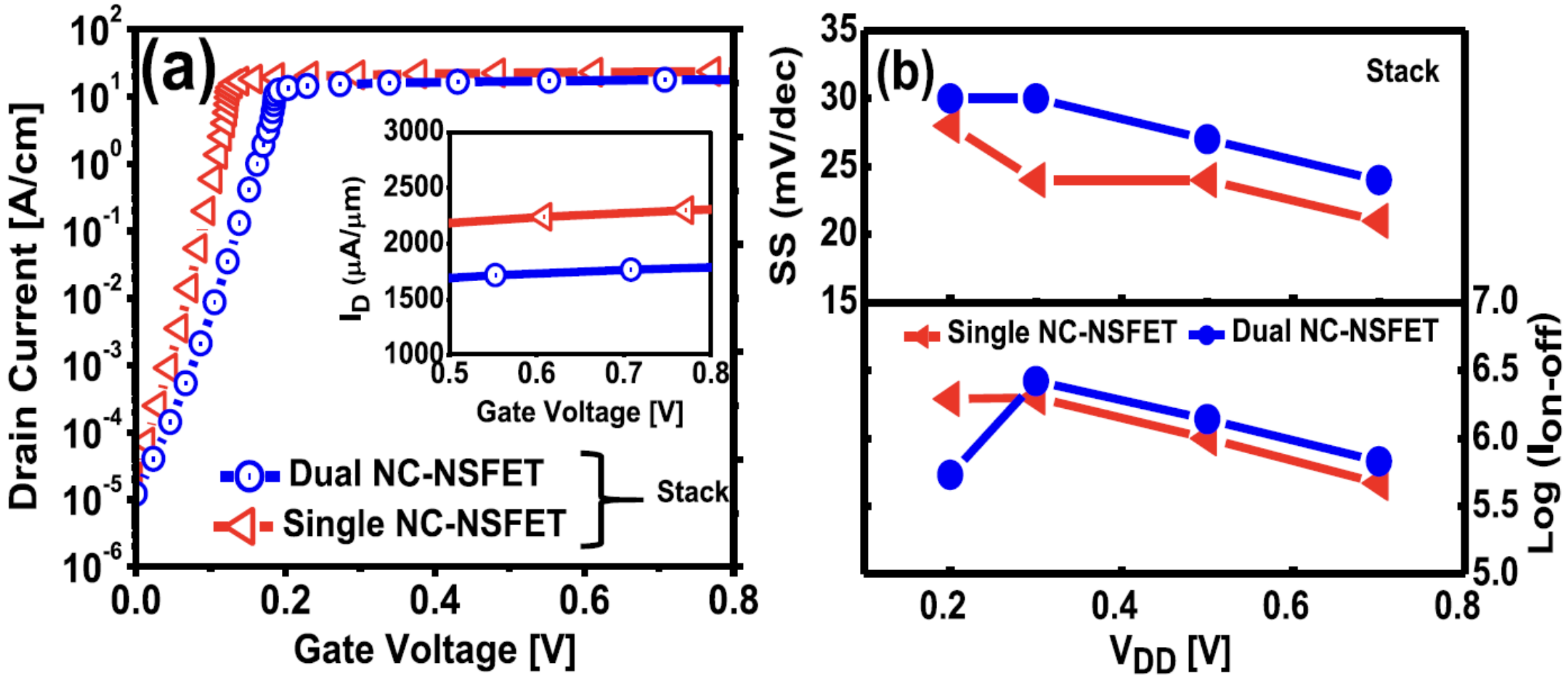


Fig. 4. (a) Transfer characteristics ($I_D - V_G$) of single stack and double stack NC-NSFET having same LF. Inset shows I_{on} enhancement in single stack NC-NSFET. (b) SS and I_{on}/I_{off} ratio at different operating voltage (V_{DD}) for single stack and double stack NC-NSFETs.

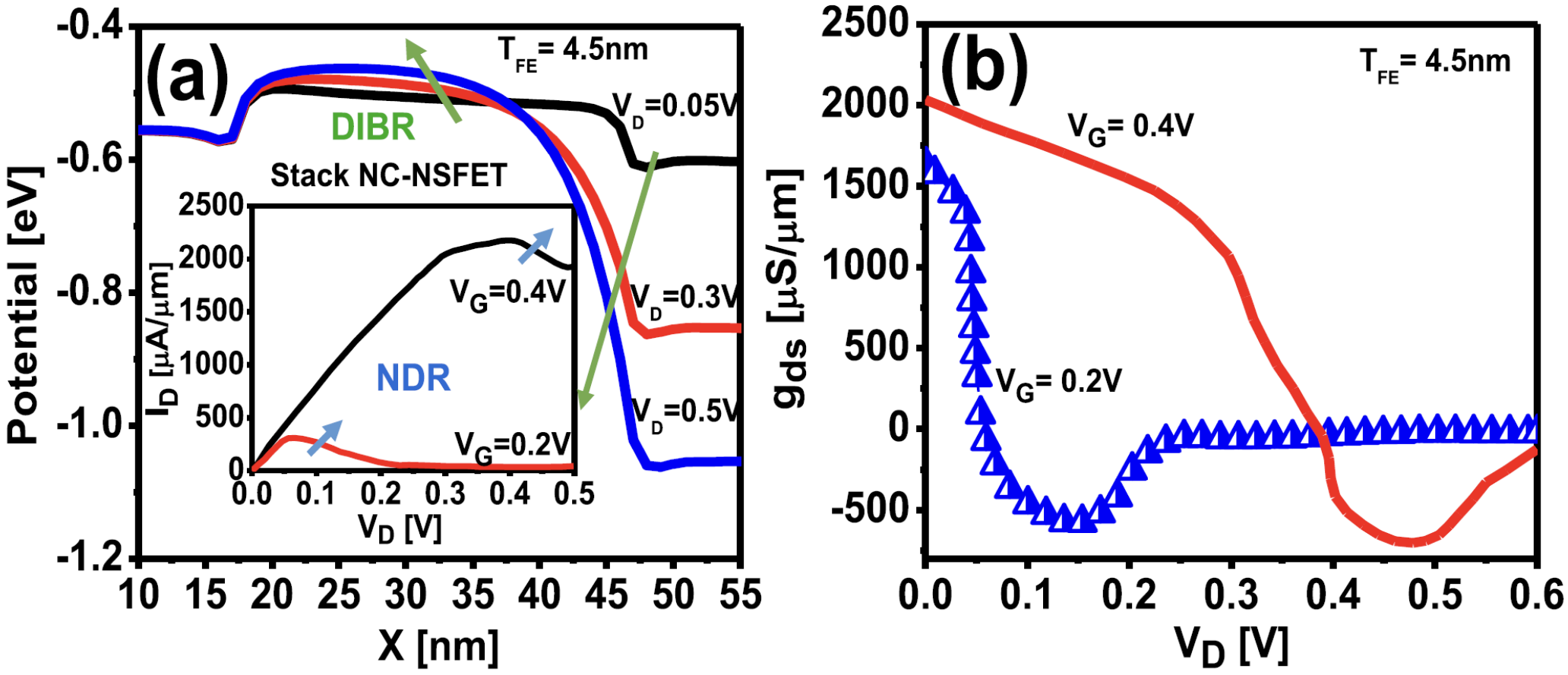


Fig. 5. (a) Potential profile at $V_G = 0.2$ V and $T_{FE} = 4.5$ nm for single stack NC-NSFET. Inset shows the output characteristics ($I_D - V_D$) of the same device showing NDR. (b) g_{ds} versus V_D at different gate bias.

DIBR and Negative Differential Resistance Characteristics

- **Phenomena in NCFETs**
- **Negative Drain-Induced Barrier Lowering (N-DIBL):**
  - Unlike conventional MOSFETs, the potential barrier rises with increasing V_D, leading to **Drain-Induced Barrier Rising (DIBR)** behavior.
  - This behavior reduces $I_D$with increasing V_D, causing **Negative Differential Resistance (NDR)**.
- **Negative Differential Resistance (NDR):**
  - $I_D$decreases with increasing V_D.
  - NDR is influenced by differential gain (A_v) and gate-drain coupling factor (η_xGD), which affect the internal node voltage (V_{int}).

Device Tuning

- **Impact of TFET_FE (T_FE):**
- **TFET_FE (T_FE) influences C_FE (C_FE), which directly affects DIBR and NDR.**
- **A thicker TFET_FE (T_FE):**
  - **Lowers subthreshold swing (SS).**
  - **Enhances NDR, potentially causing hysteresis.**
- **Output Conductance (g_ds):**
- **Defined as $g_{ds} = \Delta I_D / \Delta V_D$.**
- **g_ds depends on V_D, V_G, and TFET_FE (T_FE).**
  - **Negative g_ds: Indicates a strong NDR effect.**
  - **Positive g_ds: Achieved by engineering asymmetric source/drain parasitic capacitances.**

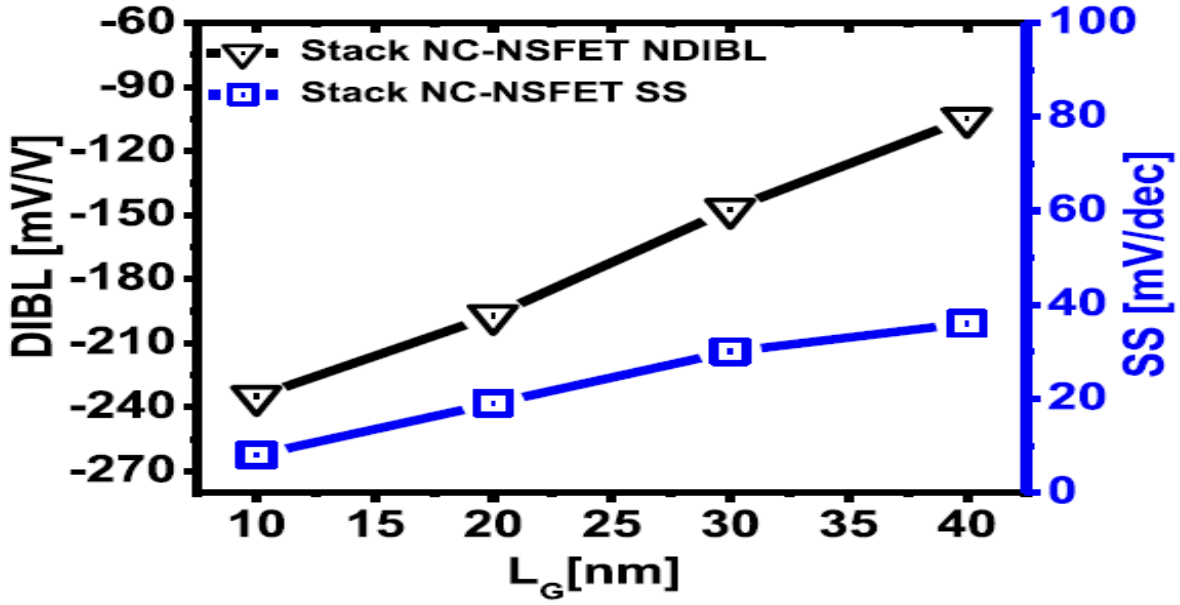
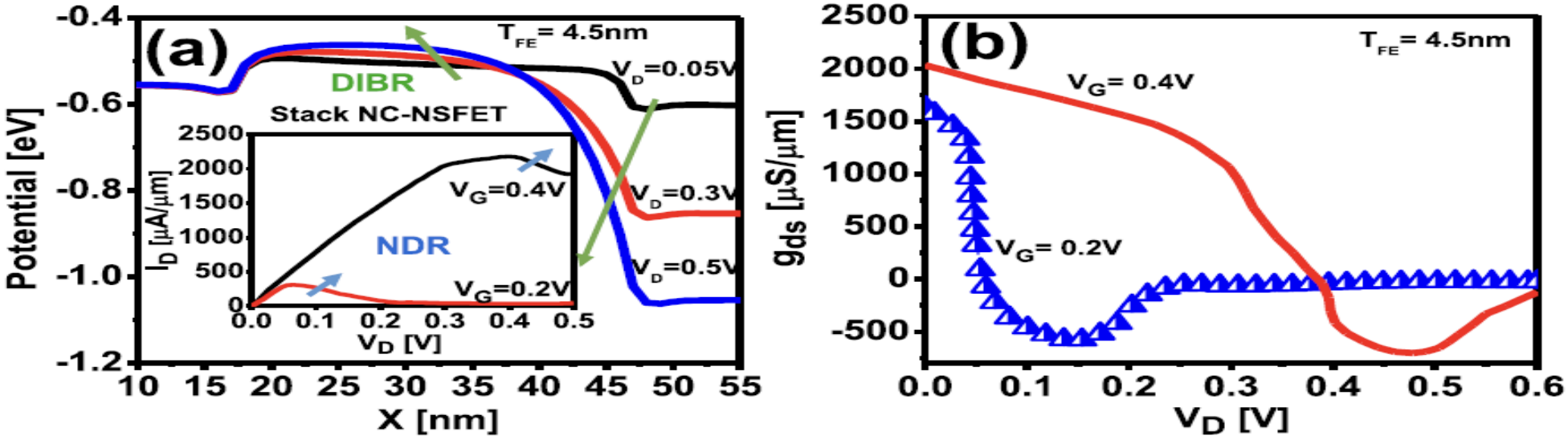


Fig. 6. Impact of channel length on SS and DIBL of single stack NC-NSFET.



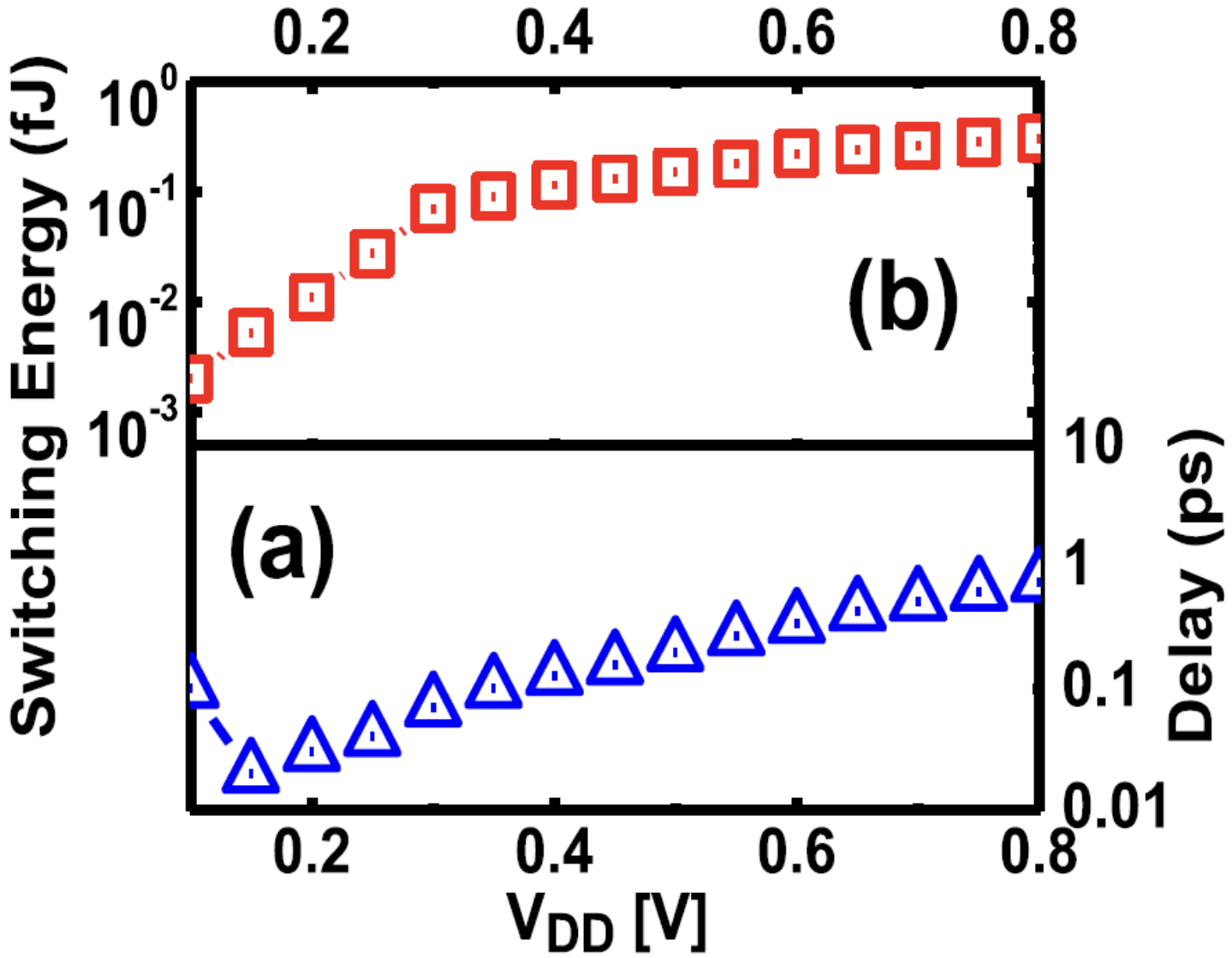


Fig. 7. (a) Switching delay and (b) switching energy versus operating voltage (V_{DD}) for single stack NC-NSFET.

Performance of NC-NSFETs Based on NS Dimensions

Key Parameters:

- Width (W_NS) and Thickness (T_NS) of the nanosheet (NS) significantly affect drive current and performance.

Transfer Characteristics (I_D-V_G):

- For thinner NS (T_NS decreases from 5 nm to 3 nm, W_NS = 20 nm):
  - Both I_on and I_off decrease.
  - Reasons:
    - Increased effective bandgap
    - Enhanced barrier height
    - Reduced density of states
    - Mobility degradation
    - Increased perpendicular electric field
  - Thinner NS requires a higher V_G for saturation current.
- Adding the FE layer compensates for the reduced I_on, improving the I_on/I_off ratio.

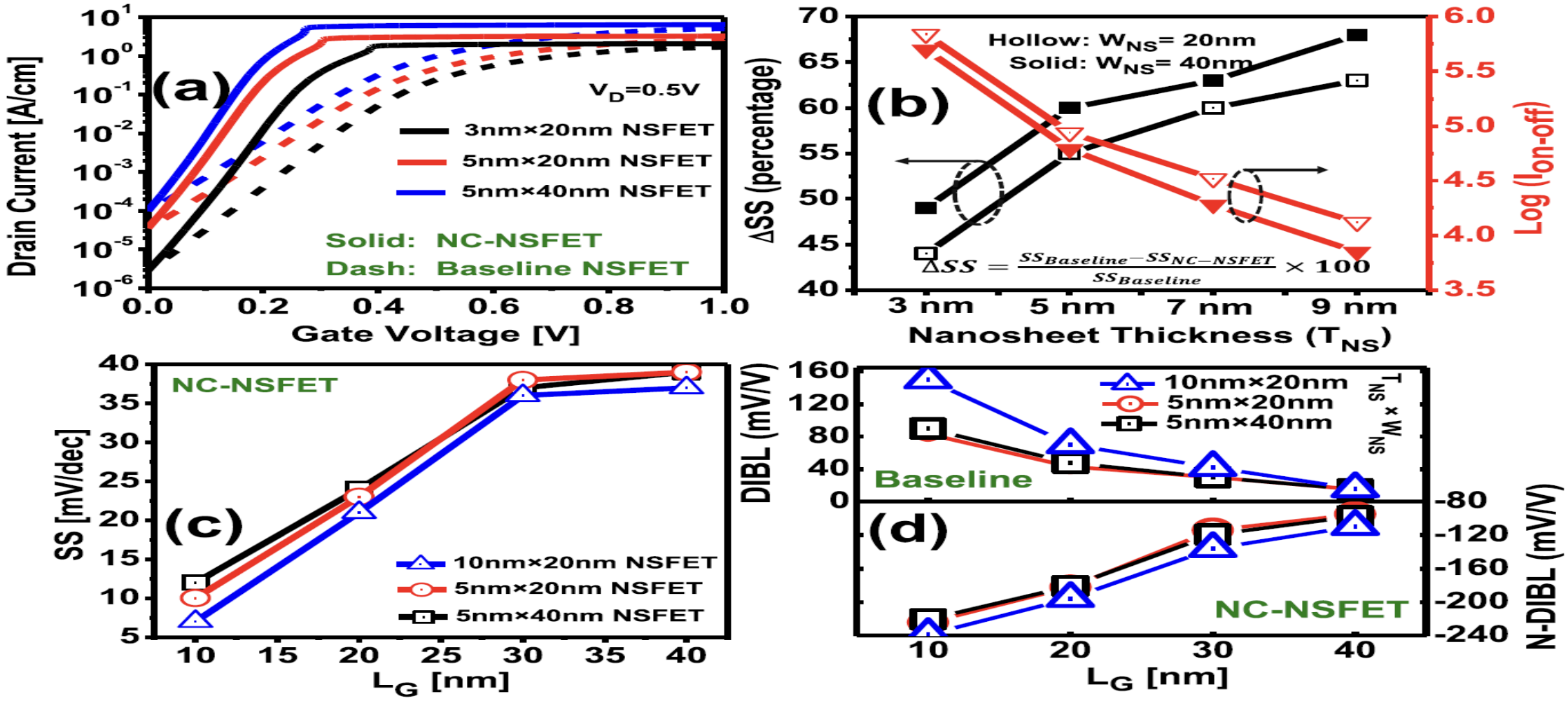
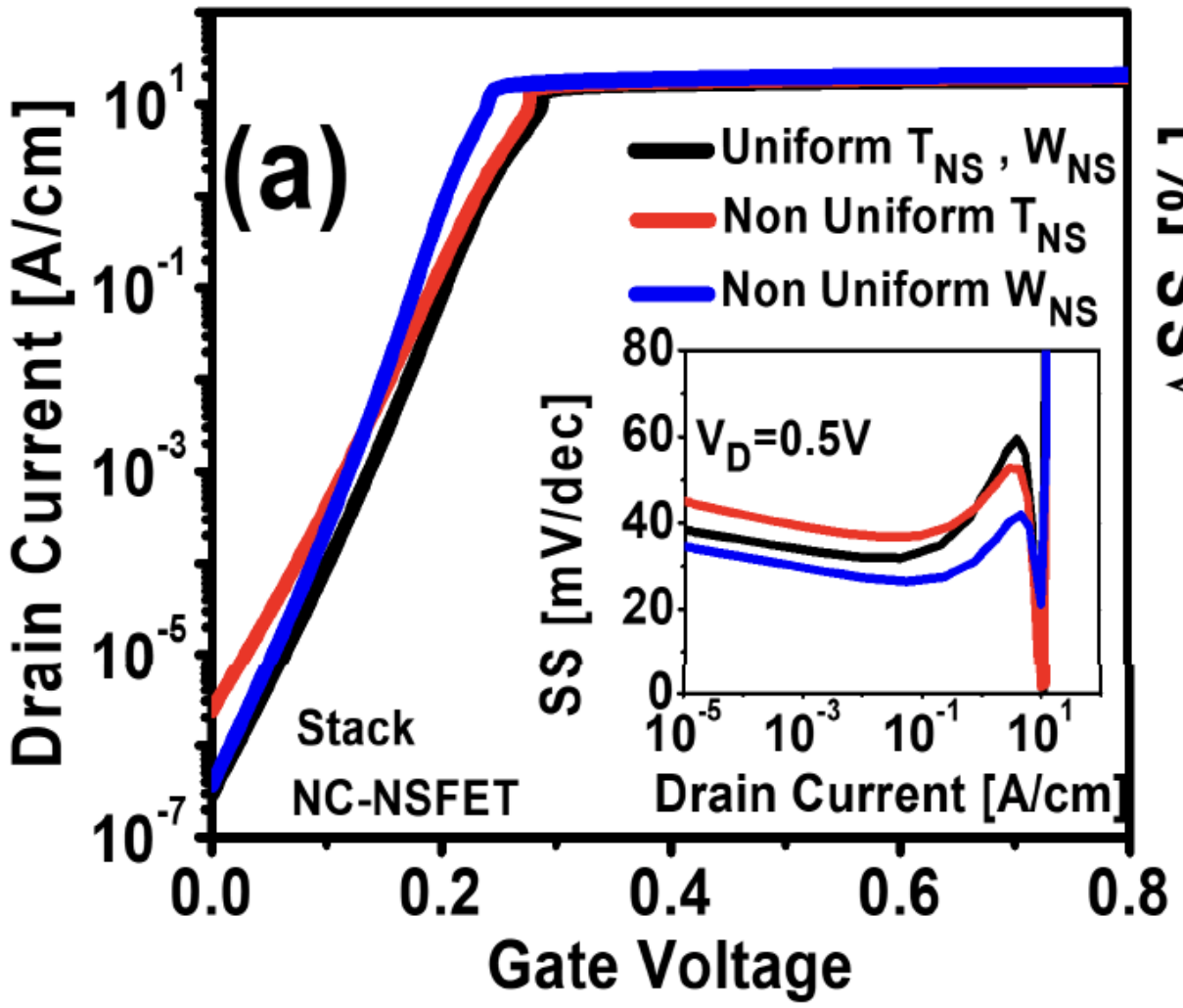
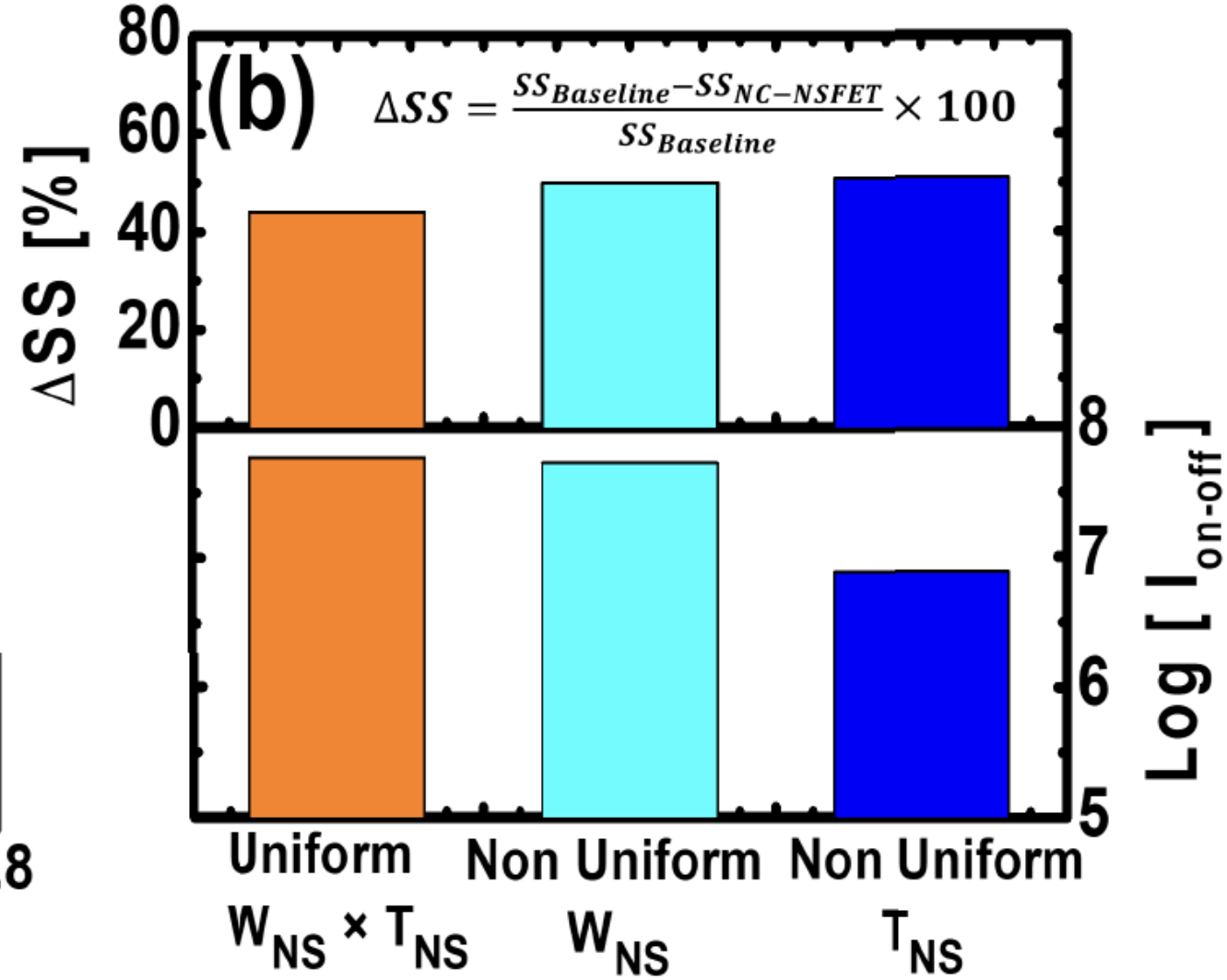


Fig. 8. (a) Transfer characteristics ($I_D - V_G$) of single channel baseline and NC-NSFETs at various NS cross sections ($T_{NS} \times W_{NS}$). (b) Percentage change in SS between baseline and NC-NSFET devices and I_{on}/I_{off} ratio at various T_{NS} for single channel NC-NSFET. (c) SS versus channel length, L_G of single channel NC-NSFETs at various NS cross sections. (d) DIBL and N-DIBL in single channel baseline and NC-NSFET, respectively, for different channel length, L_G and NS cross sections.

Nonuniformity in Stacked Nanosheets (NSs)





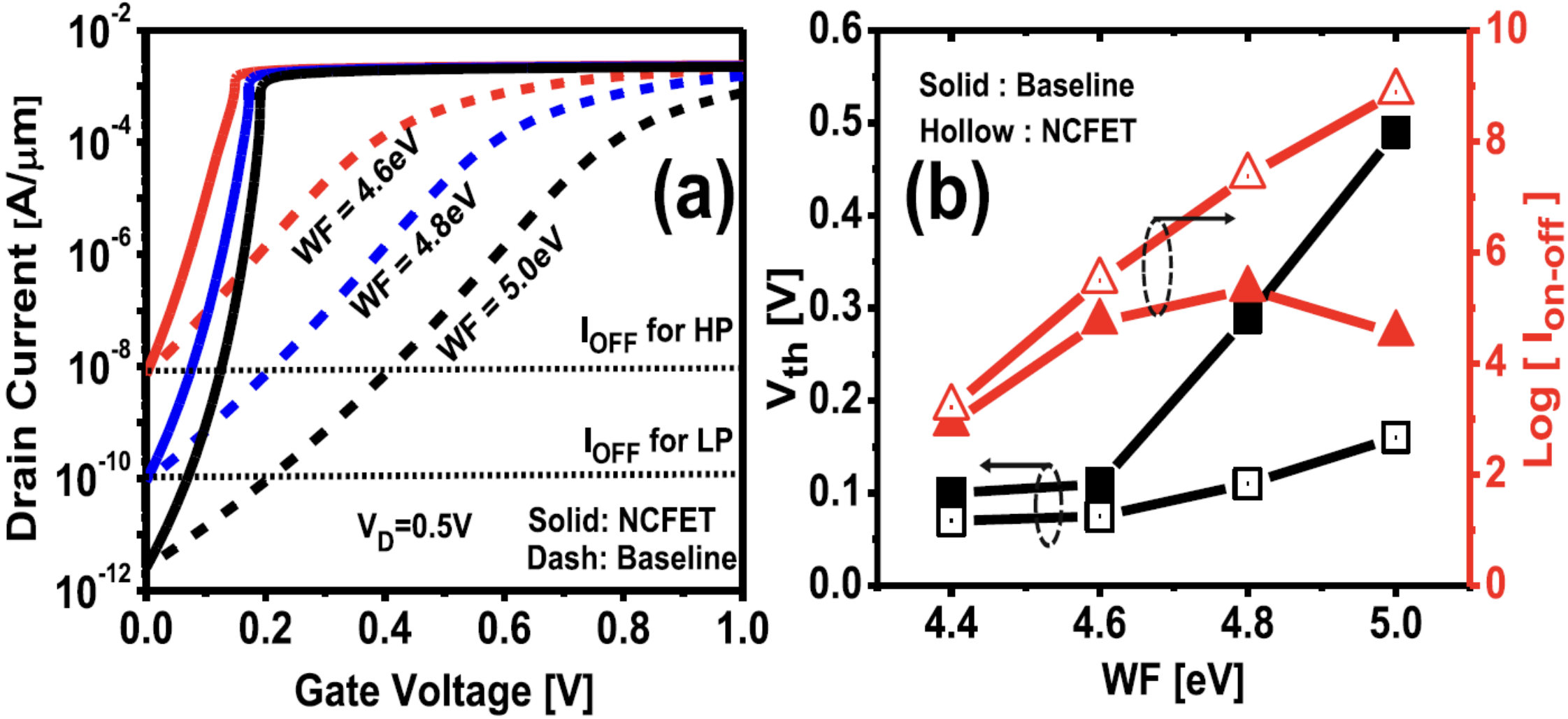


Fig. 10. (a) Transfer characteristics ($I_D - V_G$) of single stack baseline and NC-NSFET with varying metal WF. (b) V_{th} and I_{on}/I_{off} ratio changes with WF variation for both baseline and NC-NSFETs.

Sustainability & Ethical analysis

- Enables ultra-low power consumption, reducing energy demand.
- Supports device scaling, minimizing material usage.
- Extends device life, delaying electronic waste generation.
- Complex fabrication may increase resource and energy usage.
- High costs may exacerbate the digital divide.
- Manufacturing must minimize environmental harm and waste.
- Ensure transparency and collaboration in research.
- Prioritize worker safety in advanced fabrication processes.

Conclusion

- A comprehensive study of NC-NSFETs has been conducted using fully calibrated 3-D TCAD simulations.
- **Subthreshold Swing (SS):-** Single-channel NC-NSFETs demonstrate significantly lower SS (9% compared to NC-NWFET and 38% compared to NC-FinFET) for similar device dimensions.
- **Capacitance Matching:-** Effective matching between ferroelectric (FE) and MOS capacitances enables hysteresis-free operation, even with thinner FE layers, facilitating ultrascaling of NC-NSFETs.
- **Stack Performance:-** Single-stack NC-NSFETs outperform double-stack counterparts in terms of Ion, SS, and faster switching characteristics at low VDD.
- **N-DIBL and NDR:-** N-DIBL and associated negative differential resistance (NDR) behavior have been analyzed with varying gate lengths (L_G) in single-stack NC-NSFETs.
- **Impact of Key Design Parameters:**
  - Variations in NS dimensions T_{NS} and W_{NS} and metal work function (WF) influence device performance.
  - Thinner NSs yield superior performance, while W_{NS} must be optimized based on design requirements.
  - Tuning the metal WF significantly improves leakage current and Ion/Ioff ratio.

Future Works

- Explore **process variation mitigation techniques** to reduce nonuniformity in NS dimensions within stacks.
- Investigate **scaling opportunities for NC-NSFETs** beyond the 5-nm technology node.
- Optimize ferroelectric layer thickness for achieving hysteresis-free operation in multi-stack configurations.
- Extend studies on **negative capacitance effects** in different transistor architectures (e.g., gate-all-around devices).
- Develop models for **reliability analysis** under practical operating conditions, including thermal and electrical stress.
- Assess NC-NSFETs' suitability for **emerging low-power applications**, such as IoT and edge computing.
- Analyze the integration of NC-NSFETs with advanced materials, such as 2D semiconductors, for ultra-scaled devices.

References

- T. S. Perry, "The father of FinFets: Chenming Hu took transistors into the third dimension to save Moore's Law," in IEEE Spectrum, vol. 57, no. 5, pp. 46-51, May 2020, doi: 10.1109/MSPEC.2020.9078456.
- J. Singh et al., “14-nm FinFET technology for analog and RF applications,”IEEE Trans. Electron Devices, vol. 65, no. 1, pp. 31–37, Jan. 2018, doi: 10.1109/TED.2017.2776838.
- A. Razavieh, P. Zeitzoff, and E. J. Nowak, “Challenges and limitations of CMOS scaling for FinFET and beyond architectures,” IEEE Trans. Nanotechnol., vol. 18, no. 4, pp. 999–1004, Sep. 2019, doi: 10.1109/TNANO.2019.2942456.
- A. I. Rahman, A. S. Naqvi, A. A. Reza, and A. A. Farid, "Progress and Future Prospects of Negative Capacitance Devices," *Appl. Phys. Rev.*, vol. 9, no. 2, p. 020902, Feb. 2022.

- A. I. Rahman, A. S. Naqvi, A. A. Reza, and A. A. Farid, "Progress and Future Prospects of Negative Capacitance Devices," *Appl. Phys. Rev.*, vol. 9, no. 2, p. 020902, Feb. 2022.


Thank you