

FinFETs and Their Impact on Moore's Law

Name: Raahul L S
Roll No : CB.EN.U4ECE22143

Abstract:

The invention of **FinFET technology** by **Chenming Hu** and his team revolutionized the **semiconductor industry**, enabling a transition from **planar designs** to **three-dimensional structures**. This innovation addressed critical limitations of traditional **MOSFETs**, such as **poor electrostatic control** and **high leakage currents**, at **nanoscale dimensions**. By introducing a **vertical fin-like structure**, **FinFETs** offered **improved current flow control** and significantly **reduced power consumption**. These attributes established **FinFETs** as the cornerstone of advanced **CMOS technology**, extending the viability of **Moore's Law** by enabling the fabrication of **sub-10 nm nodes**. Over time, **FinFETs** have undergone substantial advancements, with their **three-dimensional architecture** allowing **gates to wrap around the channel**. This enhanced design has improved **efficiency**, minimized **short-channel effects**, and supported the development of **high-performance, energy-efficient chips**. However, as technology scales to **5 nm and beyond**, challenges such as **increased manufacturing complexity**, **higher costs**, and limitations in **short-channel effects** have surfaced, demanding innovative solutions.

To address these challenges, **Negative Capacitance FinFETs (NC-FinFETs)** have emerged as a transformative breakthrough. By integrating **ferroelectric materials** into the **gate stack**, **NC-FinFETs** leverage the **negative capacitance phenomenon** to achieve **sub-threshold swings** below the **60 mV/decade limit**, overcoming **Boltzmann's tyranny**. This capability enables **ultra-low-power operation** and significantly improves **energy efficiency**. **NC-FinFETs** also mitigate issues such as **hysteresis** and **scalability**, making them ideal for **high-performance IoT and AI applications**. Further advancements have integrated the principles of **negative capacitance** into **Gate-All-Around (GAA) nanosheet** and **nanowire transistors**, providing scalable alternatives beyond **FinFETs**. **GAA architectures** combined with **NC effects** offer **superior electrostatic control**, enhanced **current drive**, and **reduced power consumption**, making them critical for **next-generation semiconductor nodes**. Design optimization through **nanosheet dimensions**, **ferroelectric properties**, and **work function engineering** ensures their adaptability for **low-power** and **high-performance applications**.

This seminar explores the **evolution of FinFETs**, the innovations driving **NC-FinFETs**, and the prospects of **NC-GAA transistors**. It emphasizes their critical role in addressing the **scaling challenges of Moore's Law** and highlights their **transformative potential** to shape the future of **semiconductor technology** in the **post-Moore's Law era**.

References:

Base paper :

1. F. I. Sakib, M. A. Hasan, and M. Hossain, "Exploration of Negative Capacitance in Gate-All-Around Si Nanosheet Transistors," *IEEE Transactions on Electron Devices*, vol. 67, no. 11, pp. 5236–5242, Nov. 2020, doi: 10.1109/TED.2020.3025524.

Main References

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3. T. S. Perry, "The father of FinFets: Chenming Hu took transistors into the third dimension to save Moore's Law," *IEEE Spectrum*, vol. 57, no. 5, pp. 46–51, May 2020, doi: 10.1109/MSPEC.2020.9078456.